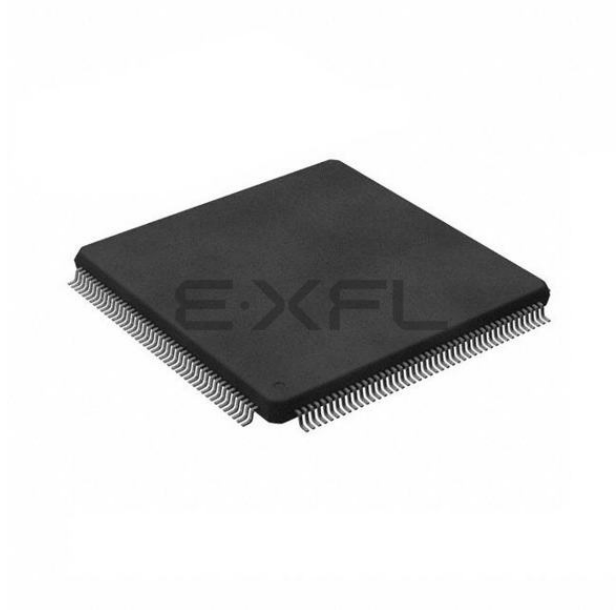


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2g28jhagv2000a

- LIN break delimiter generation (can change to 1- to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

- I²C
  - Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported
- I²S
  - Using CSIO (SPI) (ch 1 only) and I²S clock generator
  - Supports two transfer protocol: I²S and MSB-justified
  - Master mode only

DMA Controller (Eight Channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System Data Transfer Controller; 256 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 32 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Built-in three units
  - Conversion time: 0.5 µs at 5 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max 16 channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer
- Event counter mode (External clock mode)

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 121 high-speed general-purpose I/O ports in 144-pin package
- Some pins 5 V tolerant I/O.
  See 6. Pin Descriptions and 7. I/O Circuit Type for the corresponding pins.

Multi-function Timer (Max two units)

The multi-function timer is composed of the following blocks:
Minimum resolution: 5.56 ns

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 6 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC)

The real-time clock can count year, month, day, hour, minute, second, or day of the week from 00 to 99.

- Interrupt function with specifying date and time (year/month/day/hour/minute) is available. This function is also available by specifying only year, month, day, hour, or minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC; Max two channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. It is also possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the following for each channel:

- Free-running
- Periodic (= Reload)
- One shot

Watch Counter

The watch counter is used for wake up from low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock, or built-in low-speed CR clock as the clock source.

- Interval timer: up to 64 s (max) with a sub clock of 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 32 pins
  - Both edges(Rise edge and Fall edge) detect
- Include one non-maskable interrupt (NMI)

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs: a "hardware" watchdog and a "software" watchdog.

The hardware watchdog timer is clocked by low-speed internal CR oscillator. The hardware watchdog is thus active in any power saving mode except RTC mode and Stop mode.

Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator helps to verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7

SD Card Interface Available on S6E2GM, S6E2GH, and S6E2GK Devices Only

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

Ethernet-MAC Available on S6E2GM, S6E2GK, and S6E2G2 Devices only

- Compliant with IEEE802.3 specification
- 10 Mbps/100 Mbps data transfer rates supported
- MII/RMII for external PHY device supported.
- MII: Max one channel
- RMII: Max one channel
- Full-duplex and half-duplex mode supported.
- Wake-ON-LAN supported
- Built-in dedicated descriptor-system DMAC
- Built-in 2 Kbytes transmit FIFO and 2 Kbytes receive FIFO.
- Compliant IEEE1558-2008 (PTP)

Smartcard Interface (Max 2 channels)

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
  - Transmitter: 8E2, 8O2, 8N2
  - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
  - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

Clock and Reset

- Clocks

Five clock sources (two external oscillators, two internal CR oscillators, and Main PLL) that are dynamically selectable.

- Main clock: 4 MHz to 48 MHz
- Sub clock: 30 kHz to 100 kHz
- High-speed internal CR clock: 4 MHz
- Low-speed internal CR clock: 100 kHz
- Main PLL Clock

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
47	39	P41	G	I
		SOT7_1 (SDA7_1)		
		RTO11_0 (PPG11_0)		
		TIOA1_0		
		BIN0_0		
		MCSX6_0		
48	40	P42	G	I
		SCK7_1 (SCL7_1)		
		RTO12_0 (PPG12_0)		
		TIOA2_0		
		ZIN0_0		
		MCSX5_0		
49	41	P43	G	K
		SCS70_1		
		RTO13_0 (PPG13_0)		
		TIOA3_0		
		INT04_0		
		MCSX4_0		
50	42	P44	G	I
		SCS71_1		
		RTO14_0 (PPG14_0)		
		TIOA4_0		
		MCSX3_0		
51	43	P45	G	I
		SCS72_1		
		RTO15_0 (PPG15_0)		
		TIOA5_0		
		MCSX2_0		
52	44	C	-	-
53	45	VSS	-	-
54	46	VCC	-	-
55	47	P46	D	S
		X0A		
56	48	P47	D	T
		X1A		
57	49	INITX	B	C

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
98	82	P14 AN04 SOT9_1 (SDA9_1) TIOA2_2 IC1_DATA_0 TRACED0	F	N
99	83	P15 AN05 SCK9_1 (SCL9_1) TIOB2_2 IC1_CIN_0 TRACED1	F	N
100	84	P16 AN06 SIN6_1 RX0_0 INT09_0 TRACED2	F	O
101	85	P17 AN07 SOT6_1 (SDA6_1) TX0_0 TRACED3	F	N
102	-	PB0 AN16 SCK6_1 (SCL6_1) TIOA9_1 TRACED8	F	N
103	-	PB1 AN17 SCS60_1 TIOB9_1 AIN0_2 INT08_1 TRACED9	F	O
104	-	PB2 AN18 SCS61_1 TIOA10_1 BIN0_2 INT09_1 TRACED10	F	O

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
112	-	PB6	F	N
		AN22		
		SOT8_1 (SDA8_1)		
		TIOA12_1		
		BIN1_2		
		TRACED14		
113	-	PB7	F	N
		AN23		
		SCK8_1 (SCL8_1)		
		TIOB12_1		
		ZIN1_2		
		TRACED15		
114	90	P1C	F	N
		AN12		
		SCK0_1 (SCL0_1)		
		TIOA5_2		
		TRACECLK		
115	91	P1D	F	L
		AN13		
		SOT0_1 (SDA0_1)		
		TIOB5_2		
		MAD09_0		
116	92	P1E	F	M
		AN14		
		SIN0_1		
		TIOA8_1		
		INT26_1		
		MAD10_0		
117	93	P1F	F	M
		AN15		
		RTS5_0		
		TIOB8_1		
		INT27_1		
		MAD11_0		
118	94	P2A	F	M
		AN24		
		CTS5_0		
		INT08_2		
		MAD12_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
151	121	PC6 TIOA14_0 E_MDIO	K	V
152	122	PC7 INT13_0 E_MDC CROUT_1	E	W
153	123	PC8 E_RXCK_REFCK	K	V
154	124	PC9 TIOB15_0 E_COL	K	V
155	125	PCA TIOA15_0 E_CRS	K	V
156	126	ETHVCC	-	-
157	127	VSS	-	-
158	128	PCB INT28_0 E_COUT	L	W
159	129	PCC E_TCK	K	V
160	130	PCD SOT4_1 (SDA4_1) INT14_0 E_TXER	L	W
161	131	PCE SIN4_1 INT15_0 E_TX03	L	W
162	132	PCF RTS4_1 INT12_0 E_TX02	L	W
163	133	PD0 INT30_1 E_TX01	L	W
164	134	PD1 INT31_1 E_TX00	L	W
165	135	PD2 CTS4_1 E_TXEN	L	V

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 2	SIN2_0	Multi-function serial interface ch 2 input pin	106	86
	SIN2_1		38	33
	SOT2_0 (SDA2_0)	Multi-function serial interface ch 2 output pin This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I²C (operation mode 4).	107	87
	SOT2_1 (SDA2_1)		39	34
	SCK2_0 (SCL2_0)	Multi-function serial interface ch 2 clock I/O pin This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I²C (operation mode 4).	108	88
	SCK2_1 (SCL2_1)		40	35
Multi-Function Serial 3	SIN3_0	Multi-function serial interface ch 3 input pin	20	17
	SIN3_1		81	-
	SOT3_0 (SDA3_0)	Multi-function serial interface ch 3 output pin This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I²C (operation mode 4).	19	16
	SOT3_1 (SDA3_1)		82	-
	SCK3_0 (SCL3_0)	Multi-function serial interface ch 3 clock I/O pin This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I²C (operation mode 4).	18	15
	SCK3_1 (SCL3_1)		83	-
Multi-Function Serial 4	SIN4_0	Multi-function serial interface ch 4 input pin	172	140
	SIN4_1		161	131
	SOT4_0 (SDA4_0)	Multi-function serial interface ch 4 output pin This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I²C (operation mode 4).	171	139
	SOT4_1 (SDA4_1)		160	130
	SCK4_0 (SCL4_0)	Multi-function serial interface ch 4 clock I/O pin This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I²C (operation mode 4).	170	138
	SCK4_1 (SCL4_1)		166	136
	CTS4_0	Multi-function serial interface ch 4 CTS input pin	168	-
	CTS4_1		165	135
	RTS4_0	Multi-function serial interface ch 4 RTS output pin	169	137
	RTS4_1		162	132

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Timer 1	DTTI1X_0	Input signal controlling waveform generator outputs RTO10 to RTO15 of Multi-Function Timer 1.	60	50
	DTTI1X_1		78	-
	FRCK1_0	16-bit free-run timer ch 1 external clock input pin	65	55
	FRCK1_1		79	-
	IC10_0	16-bit input capture input pin of Multi-Function Timer 1. ICxx describes channel number.	61	51
	IC10_1		80	-
	IC11_0		62	52
	IC11_1		81	-
	IC12_0		63	53
	IC12_1		82	-
	IC13_0		64	54
	IC13_1		83	-
	RTO10_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	46	38
	RTO10_1 (PPG10_1)		139	-
	RTO11_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	47	39
	RTO11_1 (PPG10_1)		140	-
	RTO12_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	48	40
	RTO12_1 (PPG12_1)		141	-
	RTO13_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	49	41
	RTO13_1 (PPG12_1)		142	-
	RTO14_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	50	42
	RTO14_1 (PPG14_1)		143	-
	RTO15_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	51	43
	RTO15_1 (PPG14_1)		144	-

Latch-Up

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic pnpn junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

8.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of static electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive gases, dust, or oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, including cosmic radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

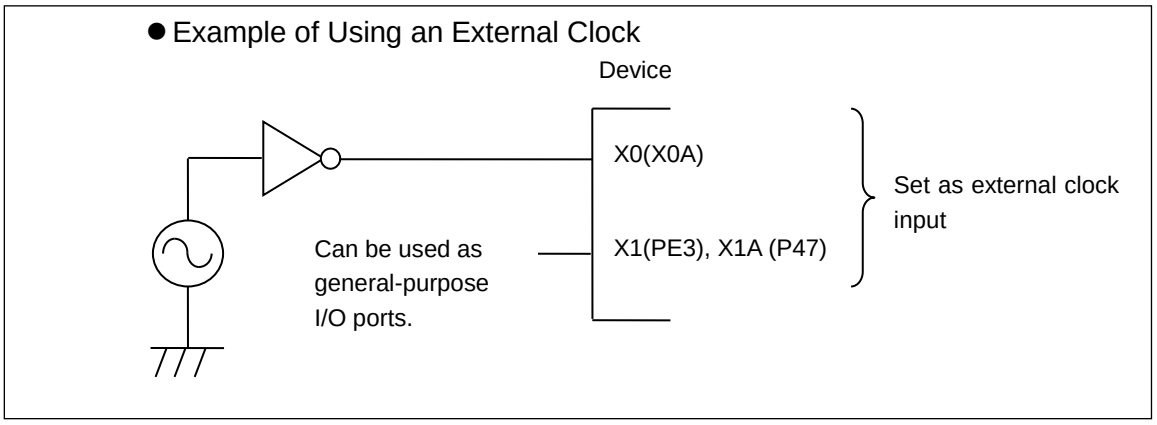
5. Smoke, flame

   CAUTION: Plastic molded devices are flammable and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

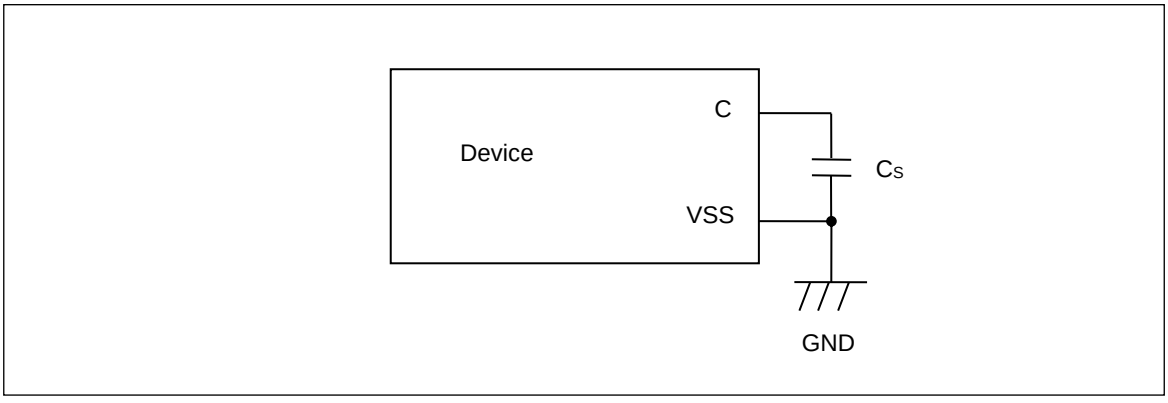


Handling When Using Multi-Function Serial Pin as I²C Pin

If the application uses the multi-function serial pin as an I²C pin, the P-channel transistor of the digital output must be disabled. I²C pins need to conform to electrical limitations like other pins, however, and avoid connecting to live external systems with the MCU power off.

C Pin

Devices in this series contain a regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. Some laminated ceramic capacitors have a large capacitance variation due to thermal fluctuation. Please select a capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of the device. A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, the distance between the mode pins and VCC pins or VSS pins is as short as possible, and the connection impedance is low when the pins are pulled up/down such as for switching the pin level and rewriting the flash memory data. This is important to prevent the device from erroneously switching to test mode as a result of noise.

Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	180 MHz	82	140	mA	*3 When all peripheral clocks are on
				*6	160 MHz	74	132	mA	
					144 MHz	68	126	mA	
					120 MHz	58	116	mA	
					100 MHz	49	107	mA	
					80 MHz	40	98	mA	
					60 MHz	31	89	mA	
					40 MHz	22	80	mA	
					20 MHz	13	71	mA	
					8 MHz	7.5	65	mA	
					4 MHz	5.6	63	mA	
				*5	180 MHz	48	106	mA	*3 When all peripheral clocks are off
				*6	160 MHz	44	102	mA	
					144 MHz	41	99	mA	
					120 MHz	35	93	mA	
					100 MHz	30	88	mA	
					80 MHz	25	83	mA	
					60 MHz	20	78	mA	
					40 MHz	14	72	mA	
					20 MHz	8.7	66	mA	
					8 MHz	5.6	63	mA	
					4 MHz	4.5	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

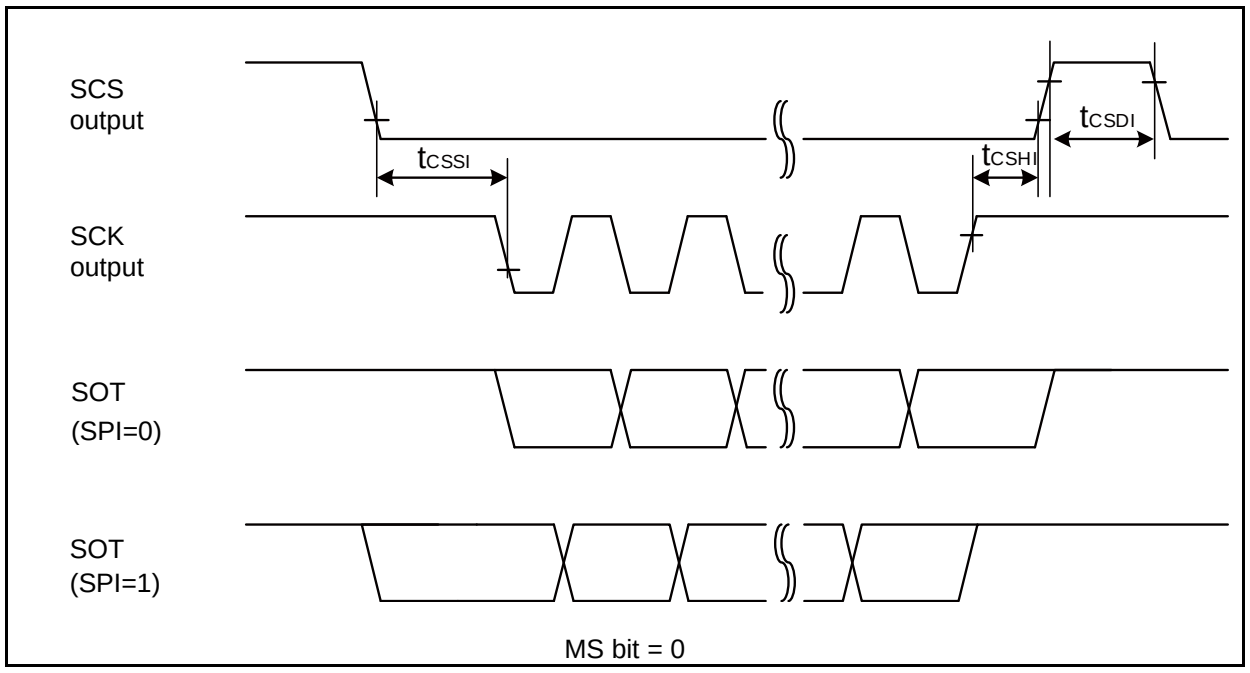
4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

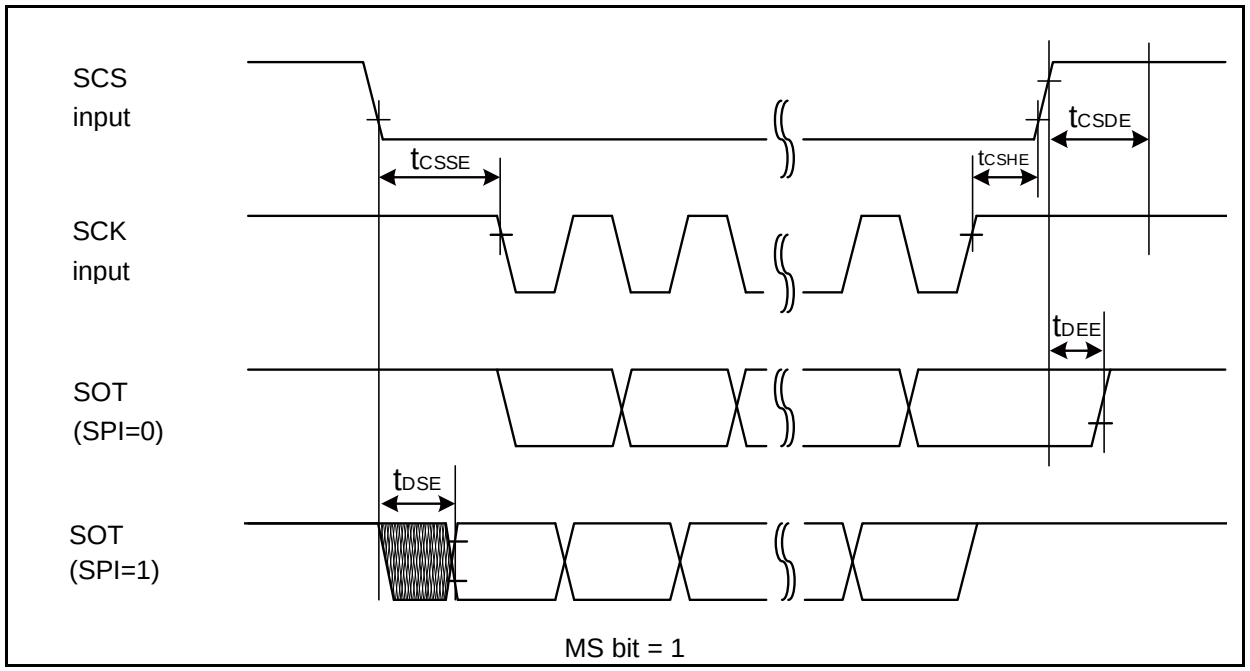
5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

7: With data access to a MainFlash memory.

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)


SCS
output
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSHI
tCSDI
MS bit = 0


SCS
input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSHE
tCSDE
tDEE
tDSE
MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

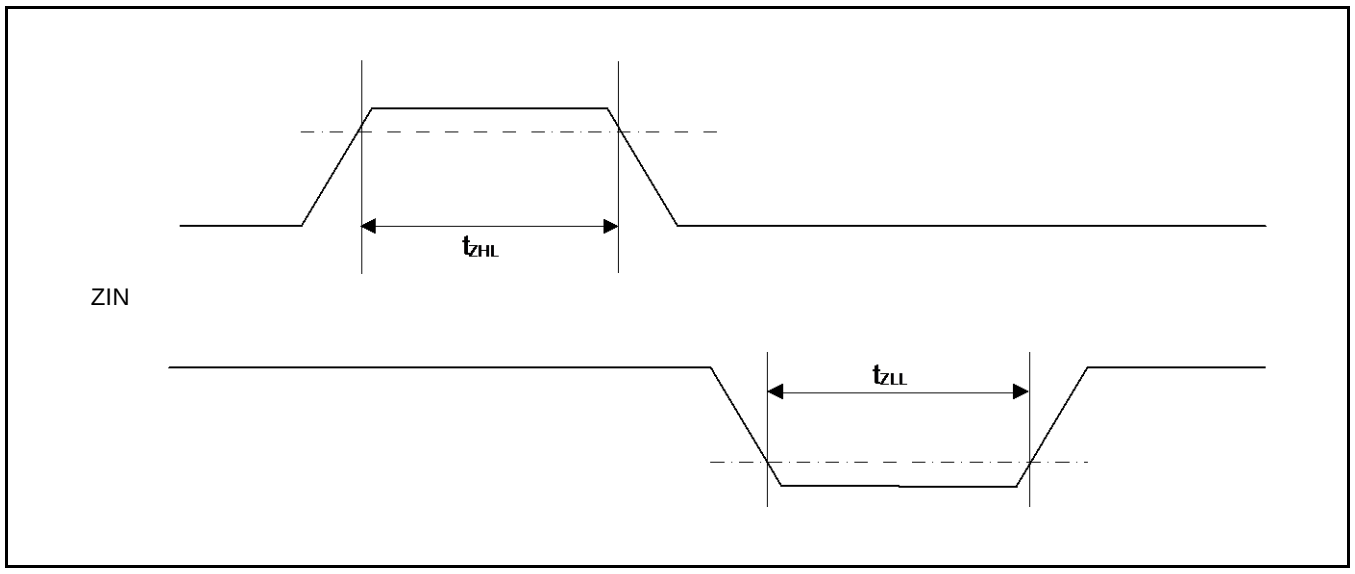
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

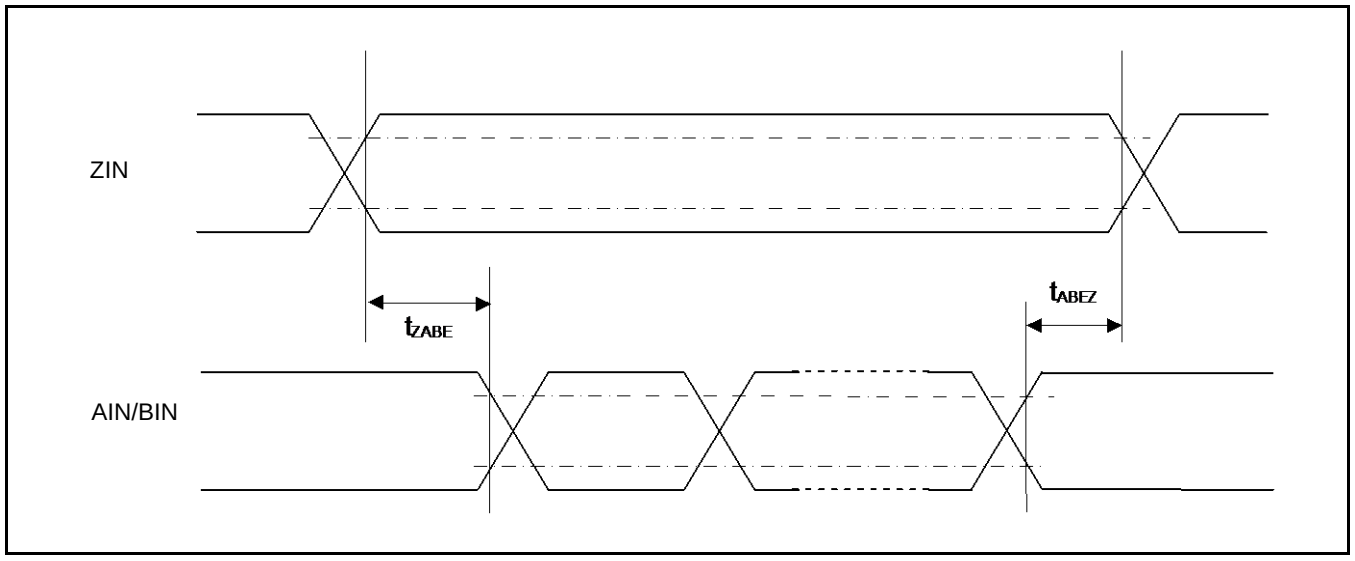
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

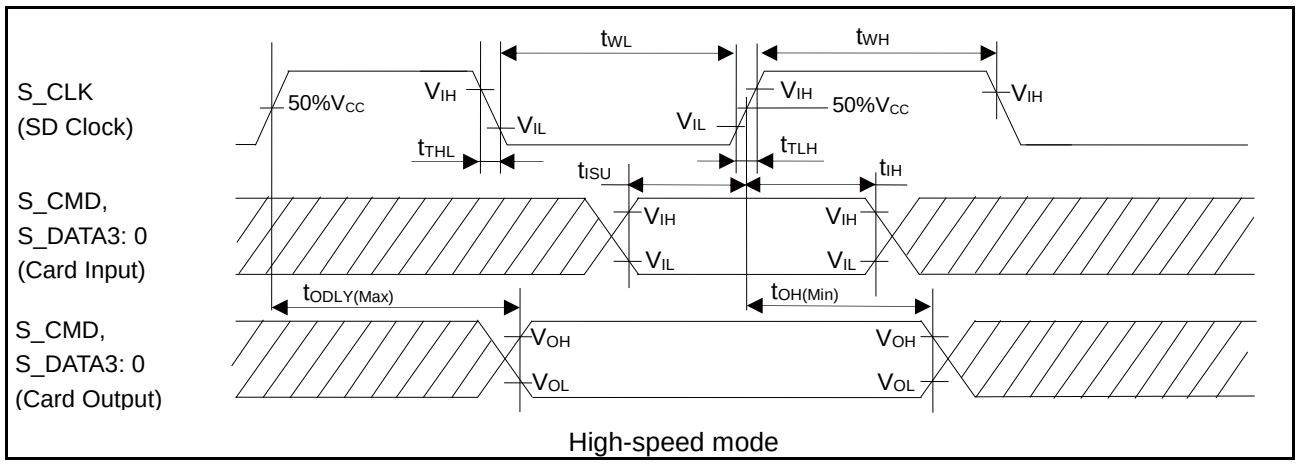
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*


ZIN
tZHL
tZLL


ZIN
tZABE
tABEZ
AIN/BIN



High-speed mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*

12.4.17 ETM/ HTM Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[15: 0]	V_{CC} ≥ 4.5 V	2	9	ns	
			V_{CC} <4.5 V	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	V_{CC} ≥ 4.5 V		50	MHz	
			V_{CC} <4.5 V		32	MHz	
TRACECLK clock cycle	t_{TRACE}		V_{CC} ≥ 4.5 V	20	-	ns	
			V_{CC} <4.5 V	31.25	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*

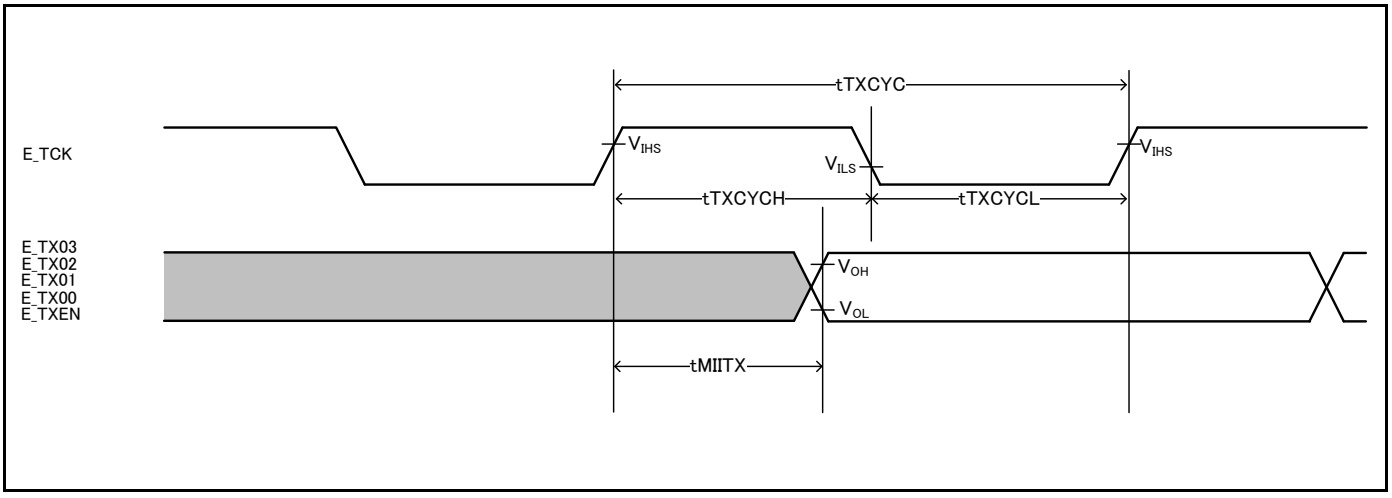
MII Transmission (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V[*1], V_{SS} = 0V, C_L = 25 pF)

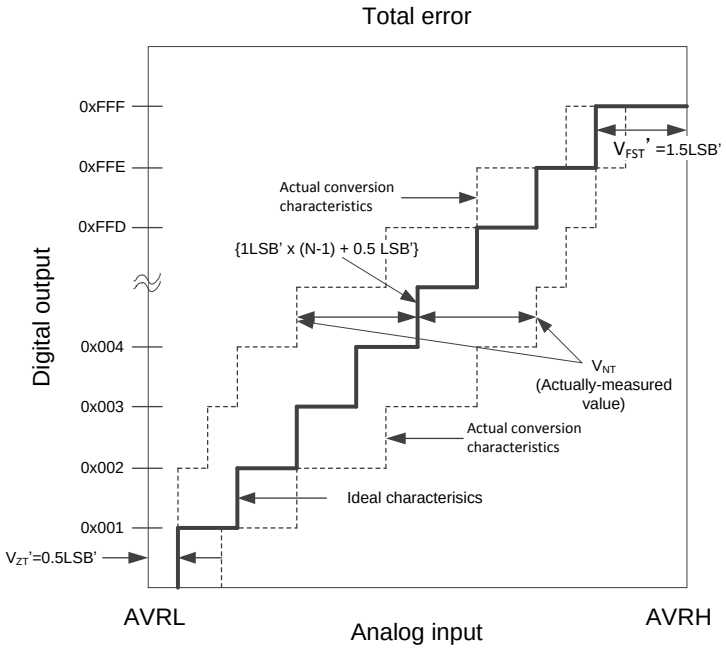
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Transmission clock Cycle time*2	t_{TXCYC}	E_TCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Transmission clock High-pulse-width duty cycle	t_{TXCYCH}	E_TCK	t_{TXCYCH}/t_{TXCYC}	35	65	%
Transmission clock Low-pulse-width duty cycle	t_{TXCYCL}	E_TCK	t_{TXCYCL}/t_{TXCYC}	35	65	%
TXCK ↑ → Transmitted data delay time	t_{MIITX}	E_TX03, E_TX02, E_TX01, E_TX00, E_TXEN	-	-	24	ns

1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

2: The transmission clock is fixed to 25 MHz or 2.5 MHz in the MII specifications. The clock accuracy should meet the PHY-device specifications.



■ Total error: A difference between actual value and theoretical value.
The overall error includes zero-transition voltage, full-scale transition voltage and linearity error.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N-1) + 0.5\ LSB'\}}{1\ LSB'} \quad [LSB]$$

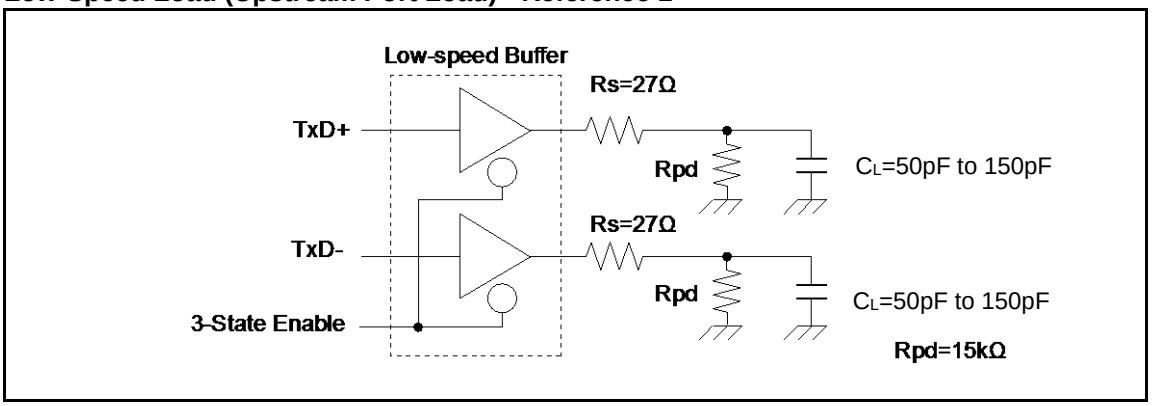
$$1\ LSB'\ (\text{ideal value}) = \frac{AVRH - AVRL}{4096} \quad [V]$$

V_{ZT}' (ideal value) = AVRL + 0.5 LSB' [V]

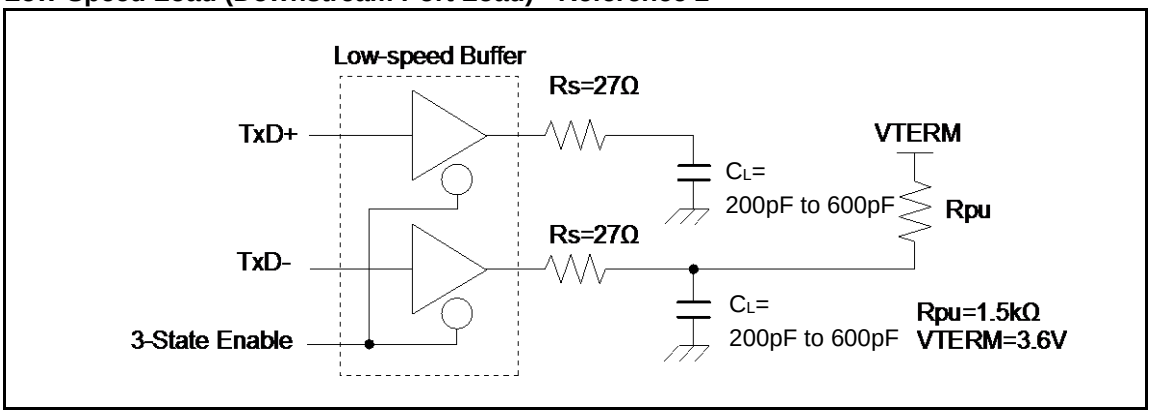
V_{FST}' (ideal value) = AVRH - 1.5 LSB' [V]

V_{NT}': A voltage for causing transition of digital output from (N-1) to N

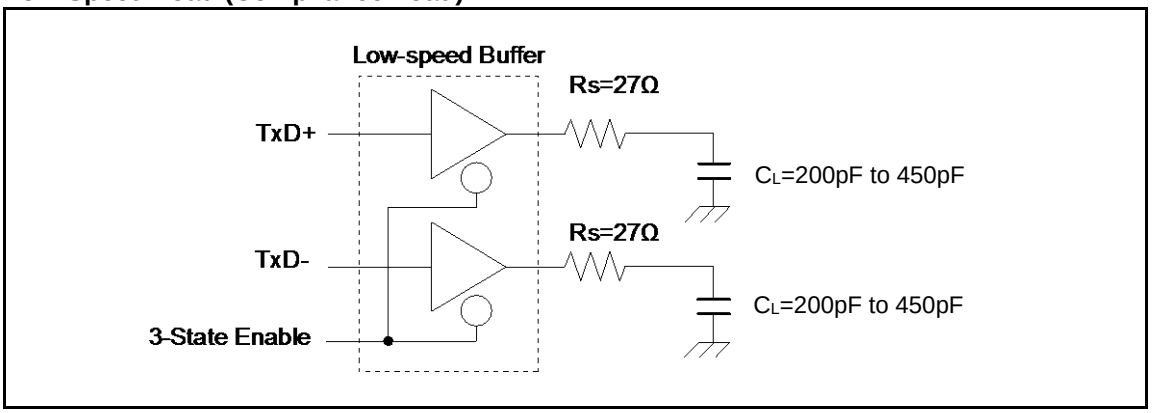
Low-Speed Load (Upstream Port Load) - Reference 1



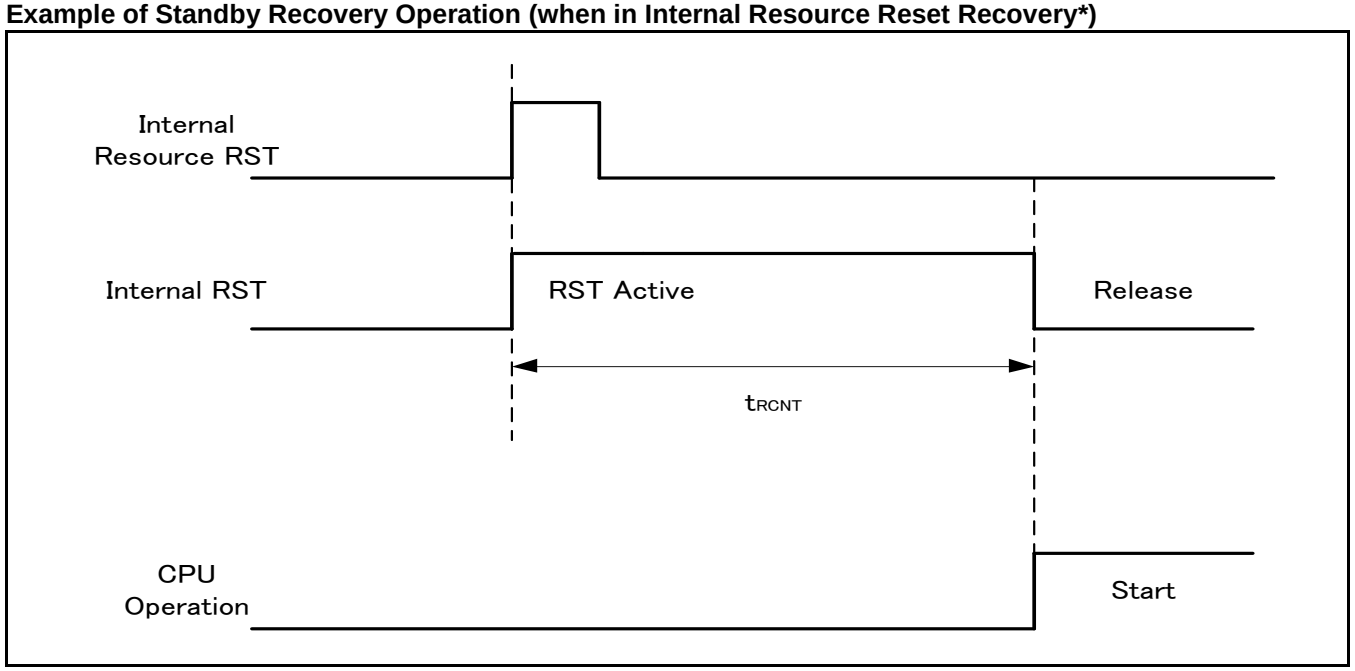
Low-Speed Load (Downstream Port Load) - Reference 2



Low-Speed Load (Compliance Load)



Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



*: Depending on the low-power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each low power consumption mode.*
  See Chapter 6: Low Power Consumption mode and Operations of Standby modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-On Reset Timing.*
- *In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.*
- *Internal resource reset indicates Watchdog reset and CSV reset.*