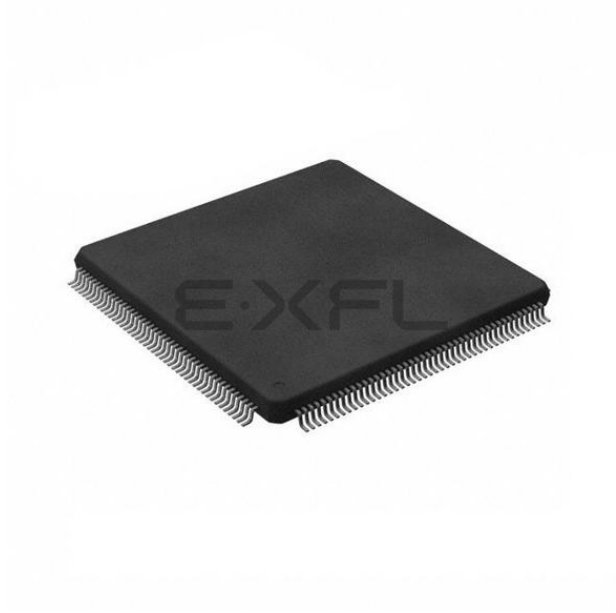


Welcome to E-XFL.COM

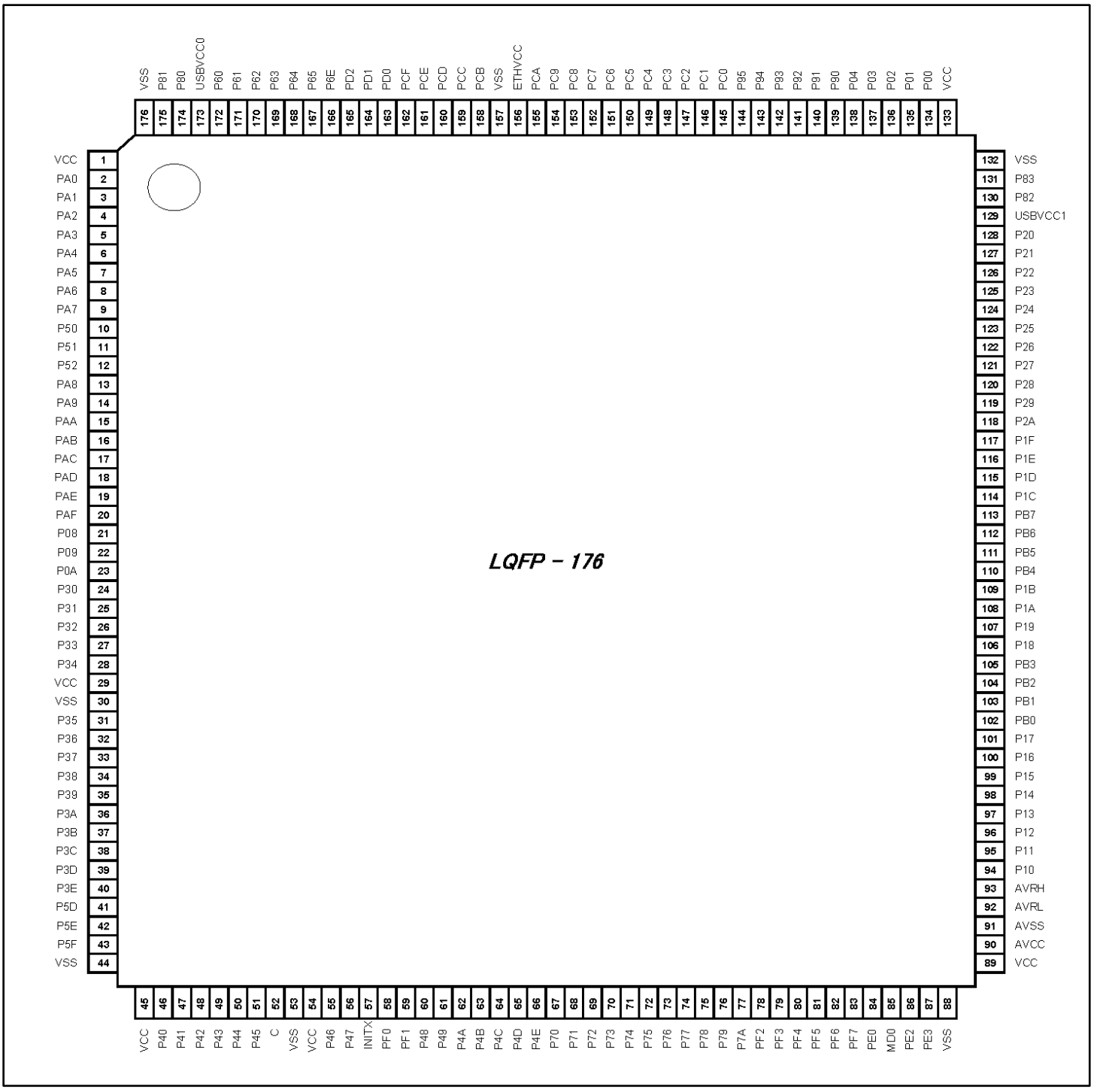
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2g36j0agv2000a

LQP176



Note:

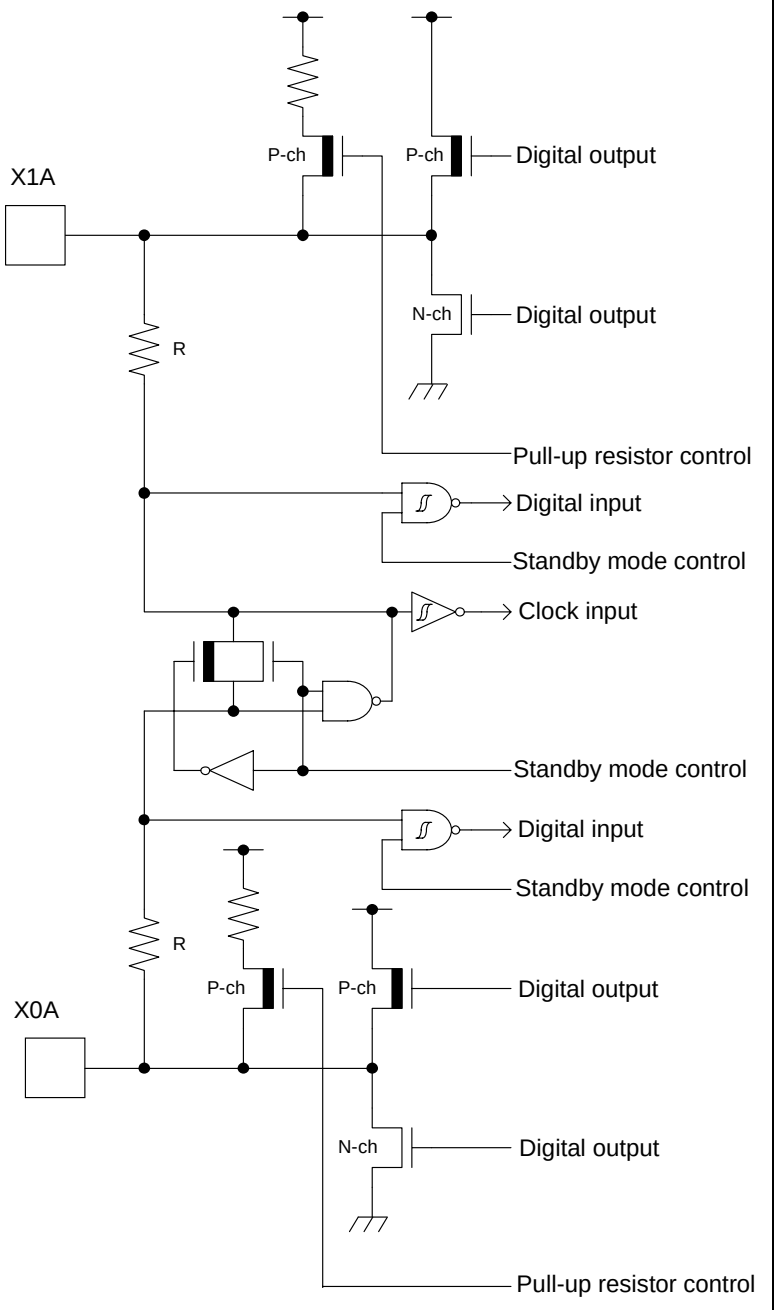
- *Only the GPIO function is shown on GPIO pins. See the table in Pin Descriptions for the full, multiplexed signal name.*

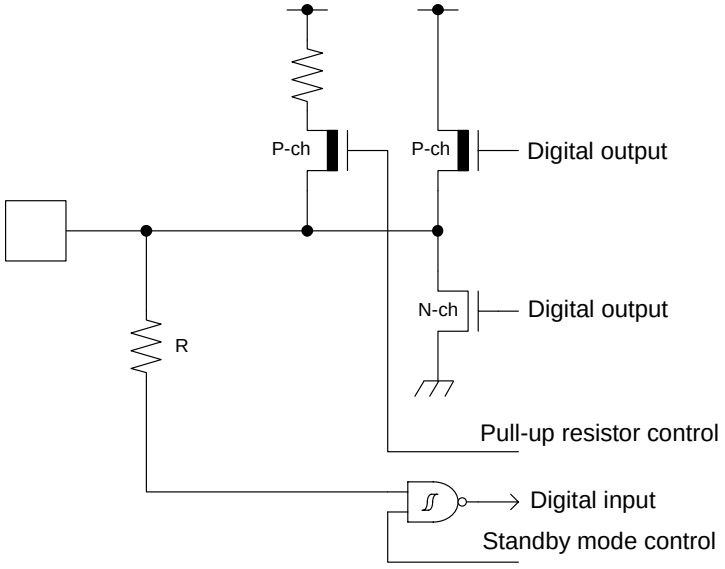
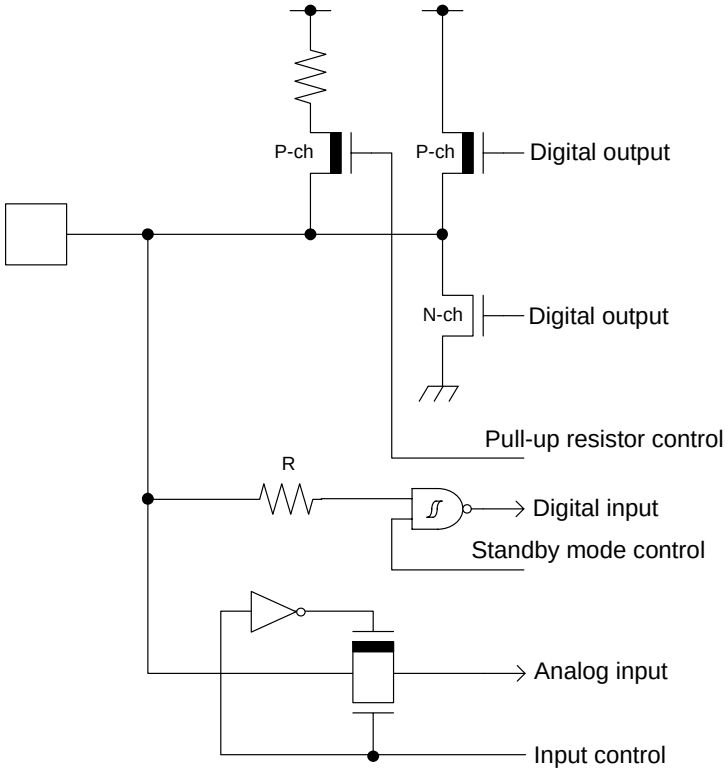
Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
151	121	PC6 TIOA14_0 E_MDIO	K	V
152	122	PC7 INT13_0 E_MDC CROUT_1	E	W
153	123	PC8 E_RXCK_REFCK	K	V
154	124	PC9 TIOB15_0 E_COL	K	V
155	125	PCA TIOA15_0 E_CRS	K	V
156	126	ETHVCC	-	-
157	127	VSS	-	-
158	128	PCB INT28_0 E_COUT	L	W
159	129	PCC E_TCK	K	V
160	130	PCD SOT4_1 (SDA4_1) INT14_0 E_TXER	L	W
161	131	PCE SIN4_1 INT15_0 E_TX03	L	W
162	132	PCF RTS4_1 INT12_0 E_TX02	L	W
163	133	PD0 INT30_1 E_TX01	L	W
164	134	PD1 INT31_1 E_TX00	L	W
165	135	PD2 CTS4_1 E_TXEN	L	V

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External interrupt	INT14_0	External interrupt request 14 input pin	160	130
	INT14_1		141	-
	INT15_0	External interrupt request 15 input pin	161	131
	INT15_1		142	-
	INT16_0	External interrupt request 16 input pin	20	17
	INT16_1		35	30
	INT17_0	External interrupt request 17 input pin	21	18
	INT17_1		36	31
	INT18_0	External interrupt request 18 input pin	22	19
	INT18_1		37	32
	INT19_0	External interrupt request 19 input pin	26	21
	INT19_1		38	33
	INT20_0	External interrupt request 20 input pin	70	60
	INT20_1		82	-
	INT21_0	External interrupt request 21 input pin	73	63
	INT21_1		83	-
	INT22_0	External interrupt request 22 input pin	76	66
	INT22_1		58	-
	INT23_0	External interrupt request 23 input pin	46	38
	INT23_1		59	-
	INT24_0	External interrupt request 24 input pin	121	97
	INT24_1		107	87
	INT25_0	External interrupt request 25 input pin	123	99
	INT25_1		97	81
	INT26_0	External interrupt request 26 input pin	126	102
	INT26_1		116	92
	INT27_0	External interrupt request 27 input pin	127	103
	INT27_1		117	93
	INT28_0	External interrupt request 28 input pin	158	128
	INT28_1		167	-
	INT29_0	External interrupt request 29 input pin	166	136
	INT29_1		168	-
	INT30_0	External interrupt request 30 input pin	169	137
	INT30_1		163	133
	INT31_0	External interrupt request 31 input pin	172	140
	INT31_1		164	134
	NMIX	Non-maskable interrupt input pin	128	104

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P30	General-purpose I/O port 3	24	-
	P31		25	-
	P32		26	21
	P33		27	22
	P34		28	23
	P35		31	26
	P36		32	27
	P37		33	28
	P38		34	29
	P39		35	30
	P3A		36	31
	P3B		37	32
	P3C		38	33
	P3D		39	34
	P3E		40	35
	P40	General-purpose I/O port 4	46	38
	P41		47	39
	P42		48	40
	P43		49	41
	P44		50	42
	P45		51	43
	P46		55	47
	P47		56	48
	P48		60	50
	P49		61	51
	P4A		62	52
	P4B		63	53
	P4C		64	54
	P4D		65	55
	P4E		66	56
	P50	General-purpose I/O port 5	10	-
	P51		11	-
	P52		12	-
	P5D		41	-
	P5E		42	-
	P5F		43	-
	P60	General-purpose I/O port 6	172	140
	P61		171	139
	P62		170	138
	P63		169	137
	P64		168	-
	P65		167	-
	P6E		166	136

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 2	SIN2_0	Multi-function serial interface ch 2 input pin	106	86
	SIN2_1		38	33
	SOT2_0 (SDA2_0)	Multi-function serial interface ch 2 output pin This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I²C (operation mode 4).	107	87
	SOT2_1 (SDA2_1)		39	34
	SCK2_0 (SCL2_0)	Multi-function serial interface ch 2 clock I/O pin This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I²C (operation mode 4).	108	88
	SCK2_1 (SCL2_1)		40	35
Multi-Function Serial 3	SIN3_0	Multi-function serial interface ch 3 input pin	20	17
	SIN3_1		81	-
	SOT3_0 (SDA3_0)	Multi-function serial interface ch 3 output pin This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I²C (operation mode 4).	19	16
	SOT3_1 (SDA3_1)		82	-
	SCK3_0 (SCL3_0)	Multi-function serial interface ch 3 clock I/O pin This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I²C (operation mode 4).	18	15
	SCK3_1 (SCL3_1)		83	-
Multi-Function Serial 4	SIN4_0	Multi-function serial interface ch 4 input pin	172	140
	SIN4_1		161	131
	SOT4_0 (SDA4_0)	Multi-function serial interface ch 4 output pin This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I²C (operation mode 4).	171	139
	SOT4_1 (SDA4_1)		160	130
	SCK4_0 (SCL4_0)	Multi-function serial interface ch 4 clock I/O pin This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I²C (operation mode 4).	170	138
	SCK4_1 (SCL4_1)		166	136
	CTS4_0	Multi-function serial interface ch 4 CTS input pin	168	-
	CTS4_1		165	135
	RTS4_0	Multi-function serial interface ch 4 RTS output pin	169	137
	RTS4_1		162	132

Type	Circuit	Remarks
D		It is possible to select the sub oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 5 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
F		• CMOS level output • CMOS level hysteresis input • Input control • Analog input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF		Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_C8FF		Reserved
0x4003_C900	0x4003_C9FF		I2S clock generator
0x4003_CA00	0x4003_CAFF		Smartcard Interface
0x4003_CB00	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface

Start Address	End Address	Bus	Peripherals
0x4004_0000	0x4004_FFFF	AHB	USB ch 0
0x4005_0000	0x4005_FFFF		USB ch 1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch 0
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x4006_5FFF		Ethernet-MAC ch 0
0x4006_6000	0x4006_6FFF		Ethernet-MAC setting register
0x4006_7000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x41FF_FFFF		Reserved

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
M	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
			$ETHV_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5$ V, I_{OL} = 2 mA					
		8 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 4 mA					
			$ETHV_{CC} \geq 4.5$ V, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5$ V, I_{OL} = 4 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5$ V, I_{OL} = 18.5 mA	V_{SS}	-	0.4	V	*1
			$USBV_{CC} < 4.5$ V, I_{OL} = 10.5 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5$ V, I_{OL} = 3 mA					
			$V_{CC} \leq 4.5$ V, I_{OL} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, USBVCC0, USBVCC1, ETHVCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

1: $USBV_{CC}0$ and $USBV_{CC}1$ are described as $USBV_{CC}$.

12.4 AC Characteristics

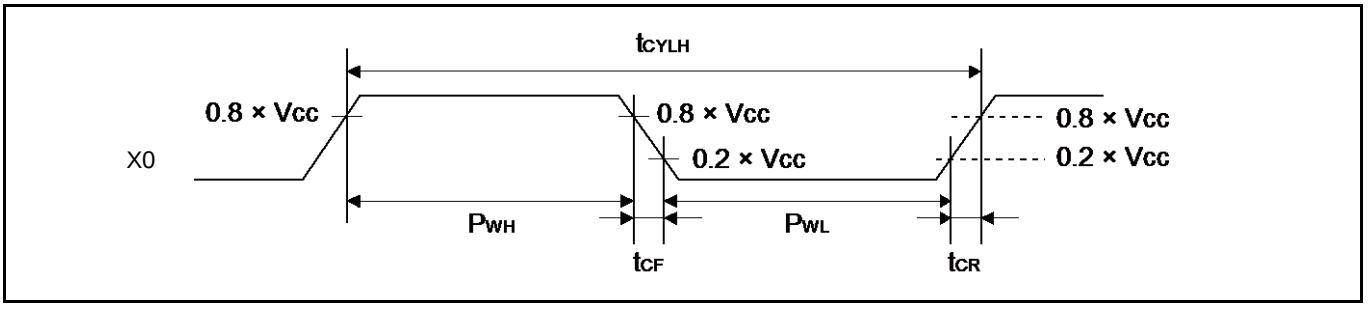
12.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥4.5 V	4	48	MHz	When crystal oscillator is connected
			V_{CC} < 4.5 V	4	20		
			V_{CC} ≥4.5 V	4	48	MHz	When using external clock
			V_{CC} < 4.5 V	4	20		
Input clock cycle	t_{CYLH}		V_{CC} ≥4.5 V	20.83	250	ns	When using external clock
			V_{CC} < 4.5 V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock *1 frequency	f_{CC}	-	-	-	180	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	90	MHz	APB0bus clock *2
	f_{CP1}	-	-	-	180	MHz	APB1bus clock *2
	f_{CP2}	-	-	-	90	MHz	APB2bus clock *2
Internal operating clock *1 cycle time	t_{CYCC}	-	-	5.56	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	11.1	-	ns	APB0bus clock *2
	t_{CYCP1}	-	-	5.56	-	ns	APB1bus clock *2
	t_{CYCP2}	-	-	11.1	-	ns	APB2bus clock *2

1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

2: For more about each APB bus to which each peripheral is connected, see 1. S6E2G Series Block Diagram in this data sheet.



12.4.6 Operating Conditions of Main PLL (in the Case of Using Built-in High-Speed CR Clock for Input Clock of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	50	-	95	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	190	-	400	MHz	
Main PLL clock frequency *2	f_{CLKPLL}	-	-	180	MHz	

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

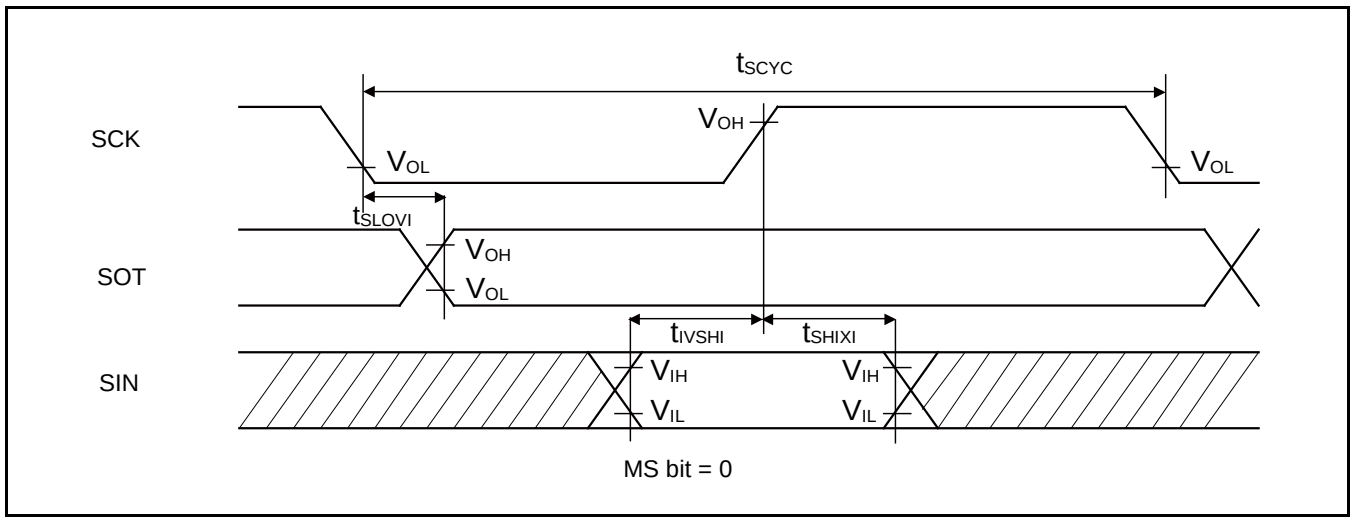
Note:

- *The High-speed CR clock (CLKHC) should be set with frequency/temperature trimming to act as the source clock of the Main PLL.*

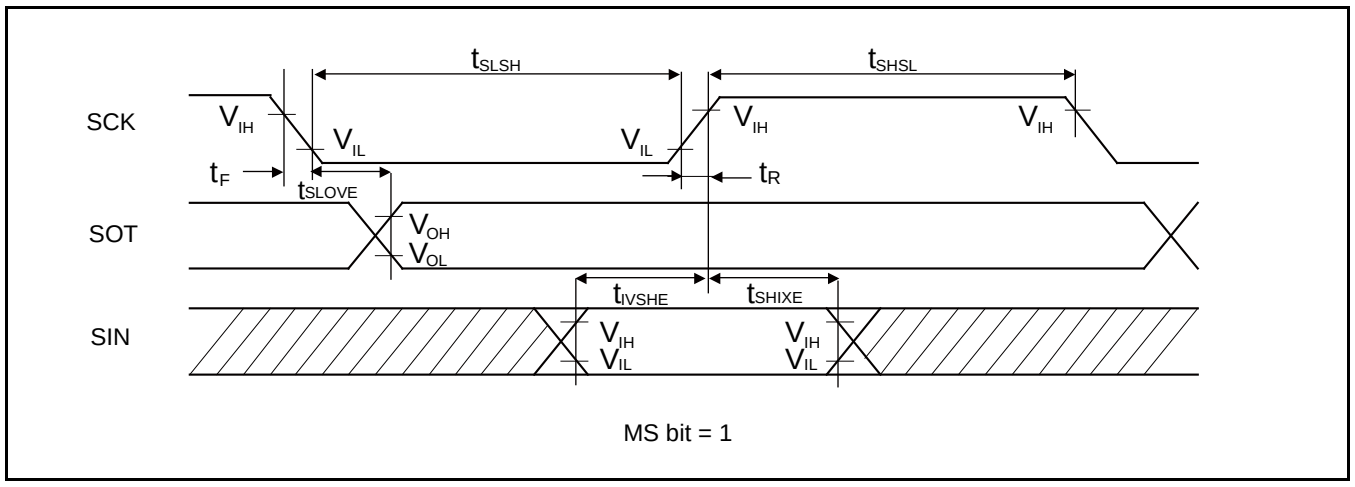
12.4.7 Reset Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	



MS bit = 0



MS bit = 1

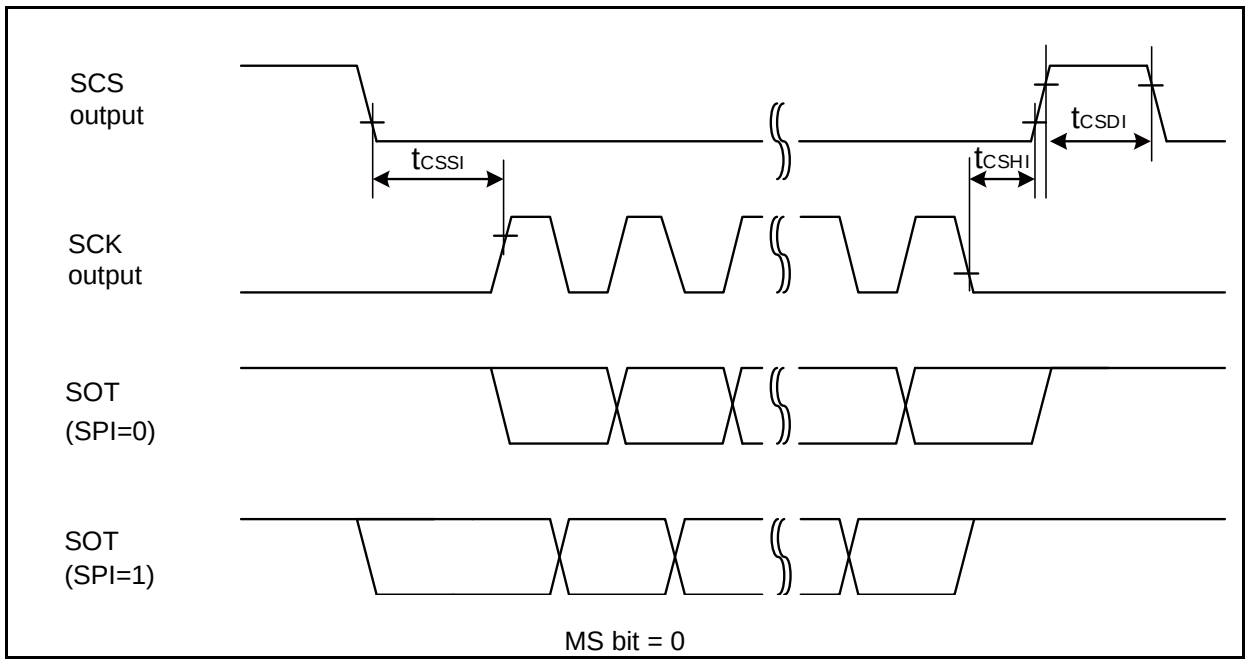
Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

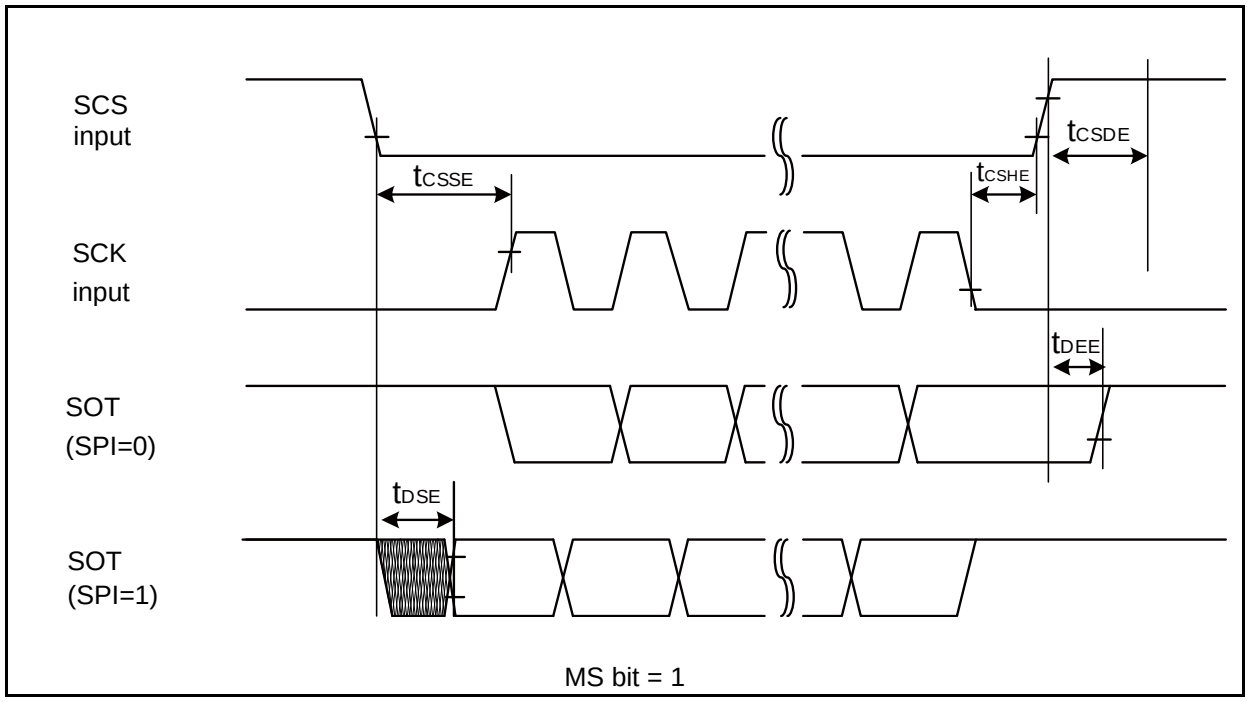
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

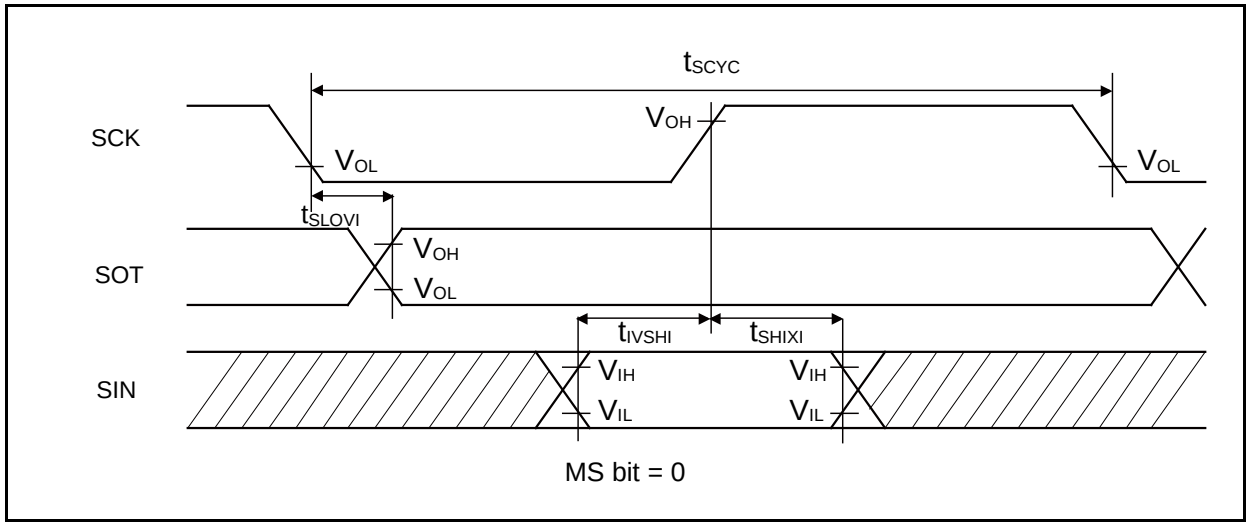
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

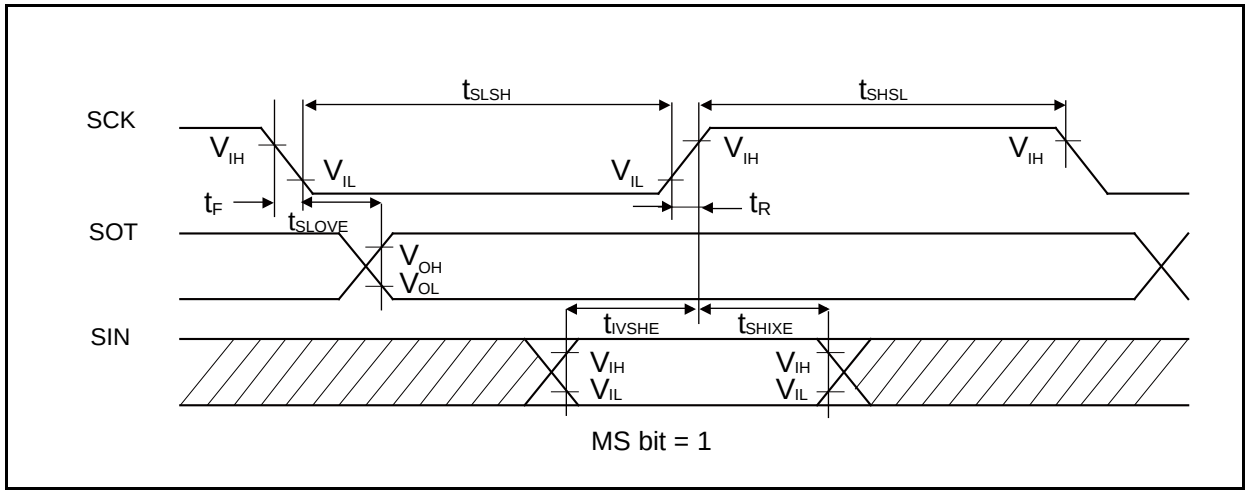
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

12.9.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

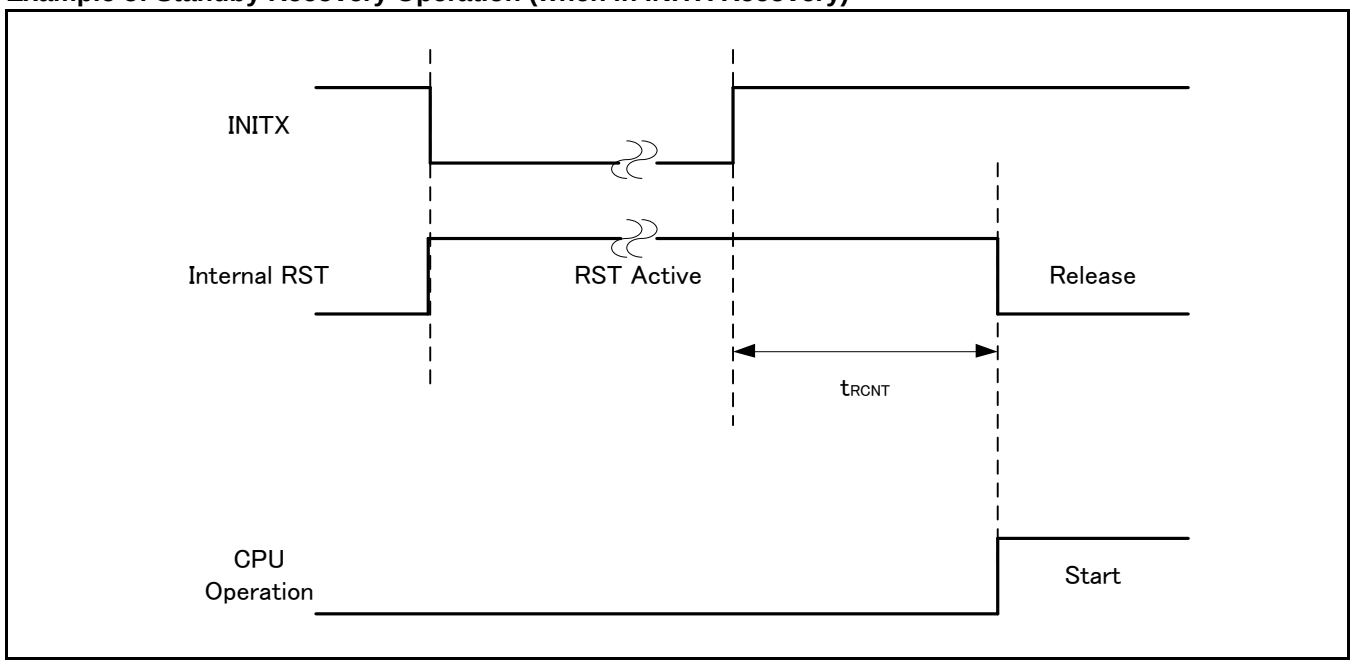
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR Timer mode		315	567	µs	
Sub Timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep Standby RTC mode with RAM retention		336	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		336	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support