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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2g38h0agv2000a

Quadrature Position/Revolution Counter (QPRC; Max two channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. It is also possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the following for each channel:

- Free-running
- Periodic (= Reload)
- One shot

Watch Counter

The watch counter is used for wake up from low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock, or built-in low-speed CR clock as the clock source.

- Interval timer: up to 64 s (max) with a sub clock of 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 32 pins
  - Both edges(Rise edge and Fall edge) detect
- Include one non-maskable interrupt (NMI)

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs: a "hardware" watchdog and a "software" watchdog.

The hardware watchdog timer is clocked by low-speed internal CR oscillator. The hardware watchdog is thus active in any power saving mode except RTC mode and Stop mode.

Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator helps to verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7

SD Card Interface Available on S6E2GM, S6E2GH, and S6E2GK Devices Only

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

Ethernet-MAC Available on S6E2GM, S6E2GK, and S6E2G2 Devices only

- Compliant with IEEE802.3 specification
- 10 Mbps/100 Mbps data transfer rates supported
- MII/RMII for external PHY device supported.
- MII: Max one channel
- RMII: Max one channel
- Full-duplex and half-duplex mode supported.
- Wake-ON-LAN supported
- Built-in dedicated descriptor-system DMAC
- Built-in 2 Kbytes transmit FIFO and 2 Kbytes receive FIFO.
- Compliant IEEE1558-2008 (PTP)

Smartcard Interface (Max 2 channels)

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
  - Transmitter: 8E2, 8O2, 8N2
  - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
  - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

Clock and Reset

- Clocks

Five clock sources (two external oscillators, two internal CR oscillators, and Main PLL) that are dynamically selectable.

- Main clock: 4 MHz to 48 MHz
- Sub clock: 30 kHz to 100 kHz
- High-speed internal CR clock: 4 MHz
- Low-speed internal CR clock: 100 kHz
- Main PLL Clock

6. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
1	1	VCC	-	-
2	2	PA0 RTO00_1 (PPG00_1) TIOA8_0 INT00_0 MADATA00_0 IC0_CIN_0	E	K
3	3	PA1 RTO01_1 (PPG01_1) TIOA9_0 MADATA01_0 IC0_DATA_0	E	I
4	4	PA2 RTO02_1 (PPG02_1) TIOA10_0 MADATA02_0 IC0_RST_0	E	I
5	5	PA3 RTO03_1 (PPG03_1) TIOA11_0 MADATA03_0 IC0_VPEN_0	E	I
6	6	PA4 RTO04_1 (PPG04_1) TIOA12_0 MADATA04_0 IC0_VCC_0	E	I
7	7	PA5 RTO05_1 (PPG05_1) TIOA13_0 INT01_0 MADATA05_0 IC0_CLK_0	E	K

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
28	23	P34 IC03_0 INT00_1 S_CLK_0	L	K
29	24	VCC	-	-
30	25	VSS	-	-
31	26	P35 IC02_0 INT01_1 S_CMD_0	L	K
32	27	P36 IC01_0 INT02_1 S_DATA3_0	L	K
33	28	P37 IC00_0 INT03_1 S_DATA2_0	L	K
34	29	P38 ADTG_2 DTTI0X_0 S_WP_0	E	I
35	30	P39 RTO00_0 (PPG00_0) TIOA0_1 AIN1_0 INT16_1 S_CD_0 MAD24_0	G	K
36	31	P3A RTO01_0 (PPG01_0) TIOA1_1 BIN1_0 INT17_1 MAD23_0	G	K
37	32	P3B RTO02_0 (PPG02_0) TIOA2_1 ZIN1_0 INT18_1 MAD22_0	G	K

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
75	65	P78	L	I
		SCK6_0 (SCL6_0)		
		AIN0_1		
		MAD06_0		
76	66	P79	E	K
		SCS60_0		
		BIN0_1		
		INT22_0		
		MAD07_0		
77	67	P7A	E	K
		SCS61_0		
		ZIN0_1		
		INT07_2		
		MAD08_0		
78	-	PF2	E	I
		SCS62_0		
		DTTI1X_1		
		TIOA6_1		
		IC1_CLK_1		
79	-	PF3	E	K
		SCS63_0		
		FRCK1_1		
		TIOB6_1		
		INT05_1		
		IC1_VCC_1		
80	-	PF4	E	K
		IC10_1		
		TIOA7_1		
		INT06_1		
		IC1_VPEN_1		
81	-	PF5	E	K
		SIN3_1		
		IC11_1		
		TIOB7_1		
		INT07_1		
		IC1_RST_1		
82	-	PF6	E	K
		SOT3_1 (SDA3_1)		
		IC12_1		
		TIOA14_1		
		INT20_1		
		IC1_DATA_1		

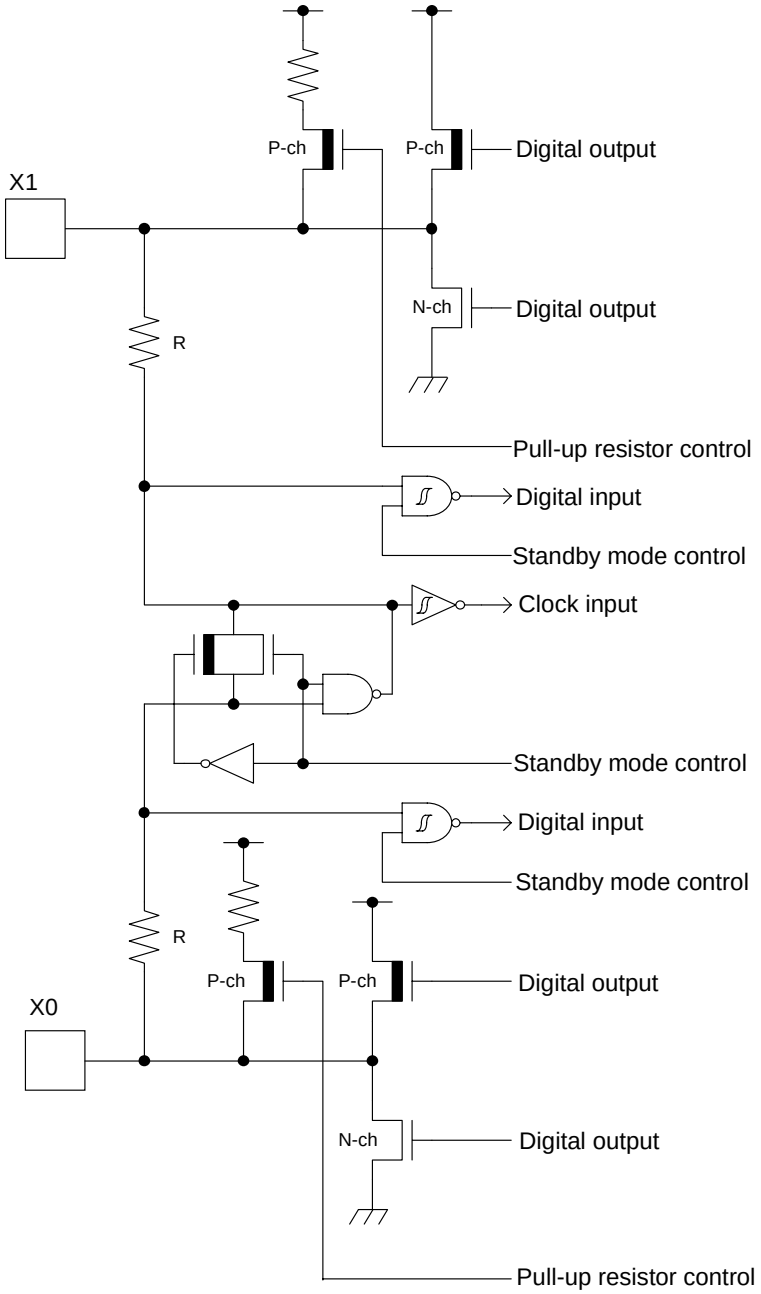
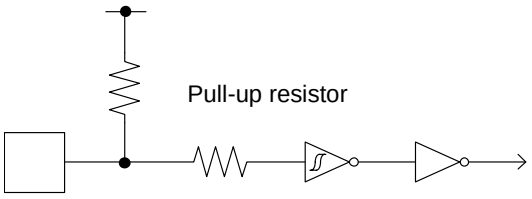
Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
112	-	PB6	F	N
		AN22		
		SOT8_1 (SDA8_1)		
		TIOA12_1		
		BIN1_2		
		TRACED14		
113	-	PB7	F	N
		AN23		
		SCK8_1 (SCL8_1)		
		TIOB12_1		
		ZIN1_2		
		TRACED15		
114	90	P1C	F	N
		AN12		
		SCK0_1 (SCL0_1)		
		TIOA5_2		
		TRACECLK		
115	91	P1D	F	L
		AN13		
		SOT0_1 (SDA0_1)		
		TIOB5_2		
		MAD09_0		
116	92	P1E	F	M
		AN14		
		SIN0_1		
		TIOA8_1		
		INT26_1		
		MAD10_0		
117	93	P1F	F	M
		AN15		
		RTS5_0		
		TIOB8_1		
		INT27_1		
		MAD11_0		
118	94	P2A	F	M
		AN24		
		CTS5_0		
		INT08_2		
		MAD12_0		

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	149	119
	TIOA7_1		80	-
	TIOA7_2		171	139
	TIOB7_0	Base Timer ch 7 TIOB pin	148	118
	TIOB7_1		81	-
	TIOB7_2		170	138
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2
	TIOA8_1		116	92
	TIOA8_2		10	-
	TIOB8_0	Base Timer ch 8 TIOB pin	17	14
	TIOB8_1		117	93
	TIOB8_2		11	-
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3
	TIOA9_1		102	-
	TIOA9_2		12	-
	TIOB9_0	Base Timer ch 9 TIOB pin	18	15
	TIOB9_1		103	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4
	TIOA10_1		104	-
	TIOB10_0	Base Timer ch 10 TIOB pin	19	16
	TIOB10_1		105	-
Base Timer 11	TIOA11_0	Base Timer ch 11 TIOA pin	5	5
	TIOA11_1		110	-
	TIOB11_0	Base Timer ch 11 TIOB pin	20	17
	TIOB11_1		111	-
	TIOB11_2		24	-
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6
	TIOA12_1		112	-
	TIOA12_2		25	-
	TIOB12_0	Base Timer ch 12 TIOB pin	21	18
	TIOB12_1		113	-
	TIOB12_2		41	-
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7
	TIOA13_1		124	100
	TIOA13_2		42	-
	TIOB13_0	Base Timer ch 13 TIOB pin	22	19
	TIOB13_1		125	101
	TIOB13_2		43	-
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	151	121
	TIOA14_1		82	-
	TIOB14_0	Base Timer ch 14 TIOB pin	150	120
	TIOB14_1		83	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External bus	MAD00_0	External bus interface address bus	69	59
	MAD01_0		70	60
	MAD02_0		71	61
	MAD03_0		72	62
	MAD04_0		73	63
	MAD05_0		74	64
	MAD06_0		75	65
	MAD07_0		76	66
	MAD08_0		77	67
	MAD09_0		115	91
	MAD10_0		116	92
	MAD11_0		117	93
	MAD12_0		118	94
	MAD13_0		119	95
	MAD14_0		120	96
	MAD15_0		121	97
	MAD16_0		122	98
	MAD17_0		123	99
	MAD18_0		124	100
	MAD19_0		40	35
	MAD20_0		39	34
	MAD21_0		38	33
	MAD22_0		37	32
	MAD23_0		36	31
	MAD24_0		35	30
	MCSX0_0	External bus interface chip select output pin	67	57
	MCSX1_0		66	56
	MCSX2_0		51	43
	MCSX3_0		50	42
	MCSX4_0		49	41
	MCSX5_0		48	40
	MCSX6_0		47	39
	MCSX7_0		46	38
	MCSX8_0		63	53

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External bus	MADATA00_0	External bus interface data bus (address/data multiplex bus)	2	2
	MADATA01_0		3	3
	MADATA02_0		4	4
	MADATA03_0		5	5
	MADATA04_0		6	6
	MADATA05_0		7	7
	MADATA06_0		8	8
	MADATA07_0		9	9
	MADATA08_0		13	10
	MADATA09_0		14	11
	MADATA10_0		15	12
	MADATA11_0		16	13
	MADATA12_0		17	14
	MADATA13_0		18	15
	MADATA14_0		19	16
	MADATA15_0		20	17
	MDQM0_0	External bus interface byte mask signal output pin	21	18
	MDQM1_0		22	19
	MALE_0	External bus interface address latch enable output signal for multiplex	171	139
	MRDY_0	External bus interface external RDY input signal	68	58
	MCLKOUT_0	External bus interface external clock output pin	23	20
	MNALE_0	External bus interface ALE signal to control NAND flash output pin	97	81
	MNCLE_0	External bus interface CLE signal to control NAND flash output pin	96	80
	MNREX_0	External bus interface read enable signal to control NAND flash	94	78
	MNWEX_0	External bus interface write enable signal to control NAND flash	95	79
	MOEX_0	External bus interface read enable signal for SRAM	169	137
	MWEX_0	External bus interface write enable signal for SRAM	170	138
	MSDCLK_0	SDRAM interface SDRAM clock output pin	65	55
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	64	54
	MRASX_0	SDRAM interface SDRAM row active strobe pin	60	50
	MCASX_0	SDRAM interface SDRAM column active strobe pin	61	51
	MSDWEX_0	SDRAM interface SDRAM write enable pin	62	52

7. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main Oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 1 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA
B		・ CMOS level hysteresis input ・ Pull-up resistor: approximately 50 kΩ

Latch-Up

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic pnpn junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected					Maintain previous state	Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

2: V_{CC} must not drop below V_{SS} - 0.5 V.

3: $USBV_{CC}0$, $USBV_{CC}1$ must not drop below V_{SS} - 0.5 V.

4: $ETHV_{CC}$ must not drop below V_{SS} - 0.5 V.

5: Ensure that the voltage does not exceed V_{CC} + 0.5V, for example, when the power is turned on.

6: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

7: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

8: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$$

- I_{OL}: L level output current
- I_{OH}: H level output current
- V_{OL}: L level output voltage
- V_{OH}: H level output voltage

I_{CC} is the current drawn by the device.
It can be analyzed as follows.

$$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$$

I_{CC} (INT): Current drawn by internal logic and memory, etc. through the regulator

ΣI_{CC} (IO): Sum of current (I/O switching current) drawn by the output pin

For I_{CC} (INT), it can be anticipated by "(1) Current Rating" in "12.3. DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For I_{CC} (IO), it depends on system used by customers.
The calculation formula is shown below.

$$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times f_{SW}$$

- C_{INT}: Pin internal load capacitance
- C_{EXT}: External load capacitance of output pin
- f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself:

Measure current value I_{CC} (Typ) at normal temperature (+25°C).

Add maximum leakage current value I_{CC} (leak_max) at operating on a value in (1).

$$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	I_{CC} (leak_max)	T_J = +125 °C	53.6 mA
		T_J = +105 °C	26.6 mA
		T_J = +85 °C	17.5 mA

12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	180 MHz	73	131	mA	*3 When all peripheral clocks are on
				*6	160 MHz	65	123	mA	
					144 MHz	59	117	mA	
					120 MHz	50	108	mA	
					100 MHz	43	101	mA	
					80 MHz	35	93	mA	
					60 MHz	27	85	mA	
					40 MHz	19	77	mA	
					20 MHz	11	69	mA	
					8 MHz	6.9	64	mA	
					4 MHz	5.3	63	mA	
				*5	180 MHz	44	102	mA	*3 When all peripheral clocks are off
				*6	160 MHz	40	98	mA	
					144 MHz	36	94	mA	
					120 MHz	31	89	mA	
					100 MHz	27	85	mA	
					80 MHz	22	80	mA	
					60 MHz	17	75	mA	
					40 MHz	13	71	mA	
					20 MHz	7.9	65	mA	
					8 MHz	5.2	63	mA	
					4 MHz	4.3	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

6: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory."

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

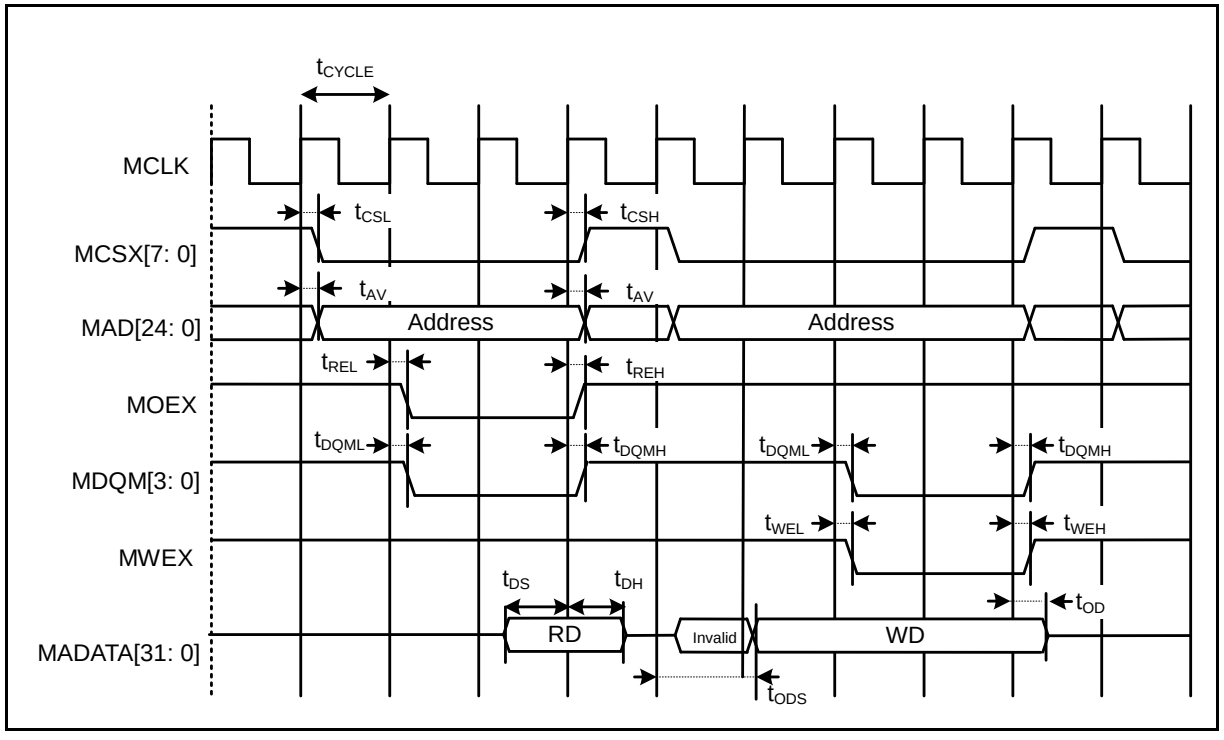
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX[7: 0]	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1: 0] delay time	t_{DQML}	MCLK, MDQM[3: 0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[31: 0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[31: 0]	-	1	18	ns	

Note:

- *When the external load capacitance C_L = 30 pF*



When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↓ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t_{DEE}		0	-	0	-	ns

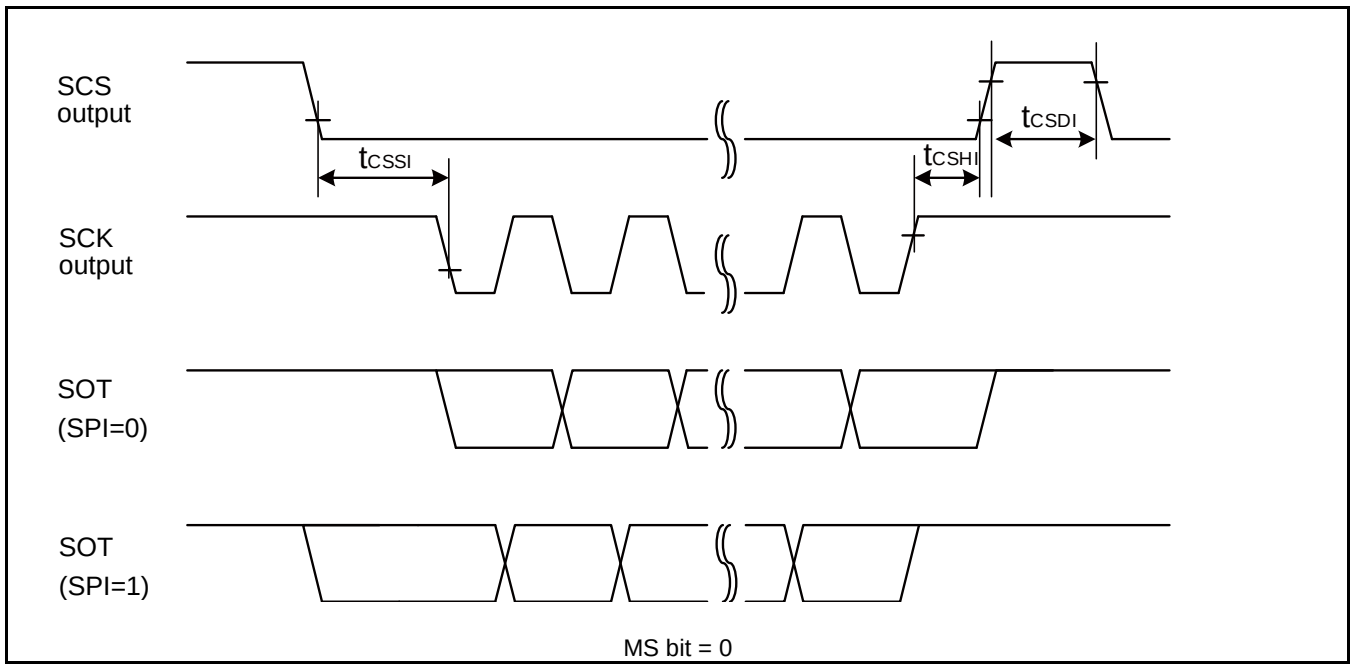
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

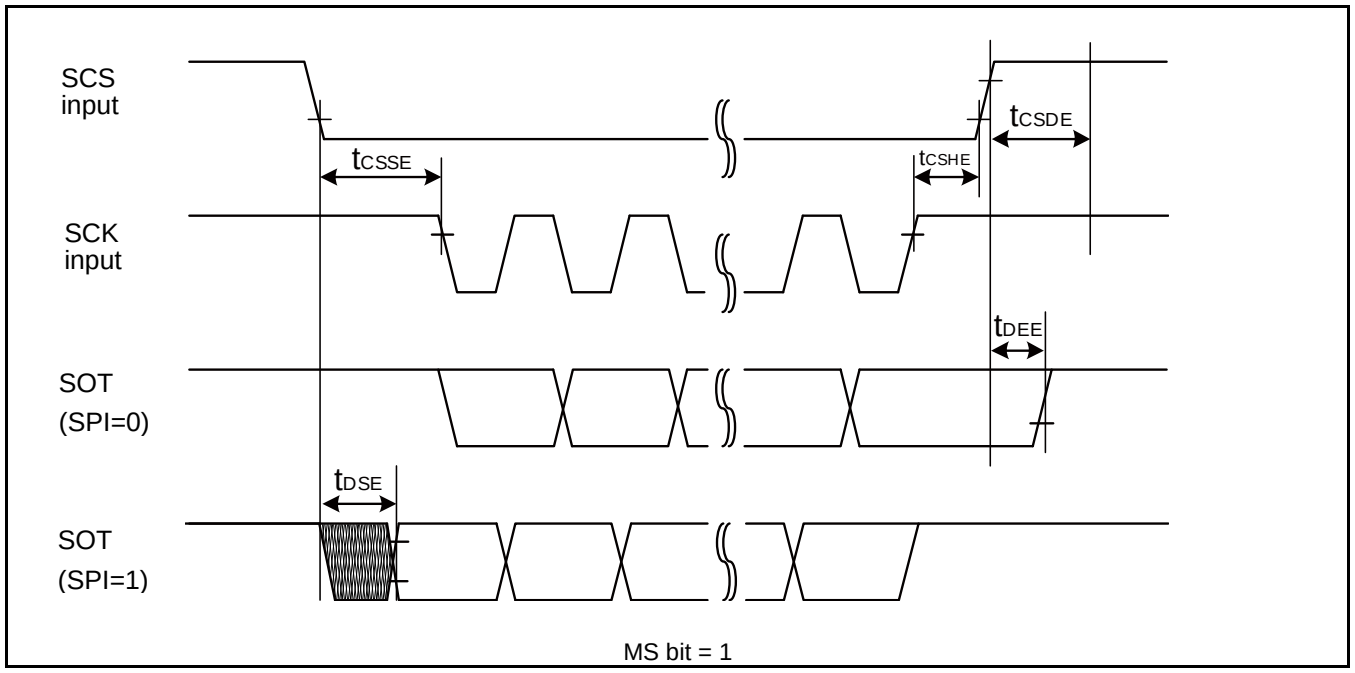
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

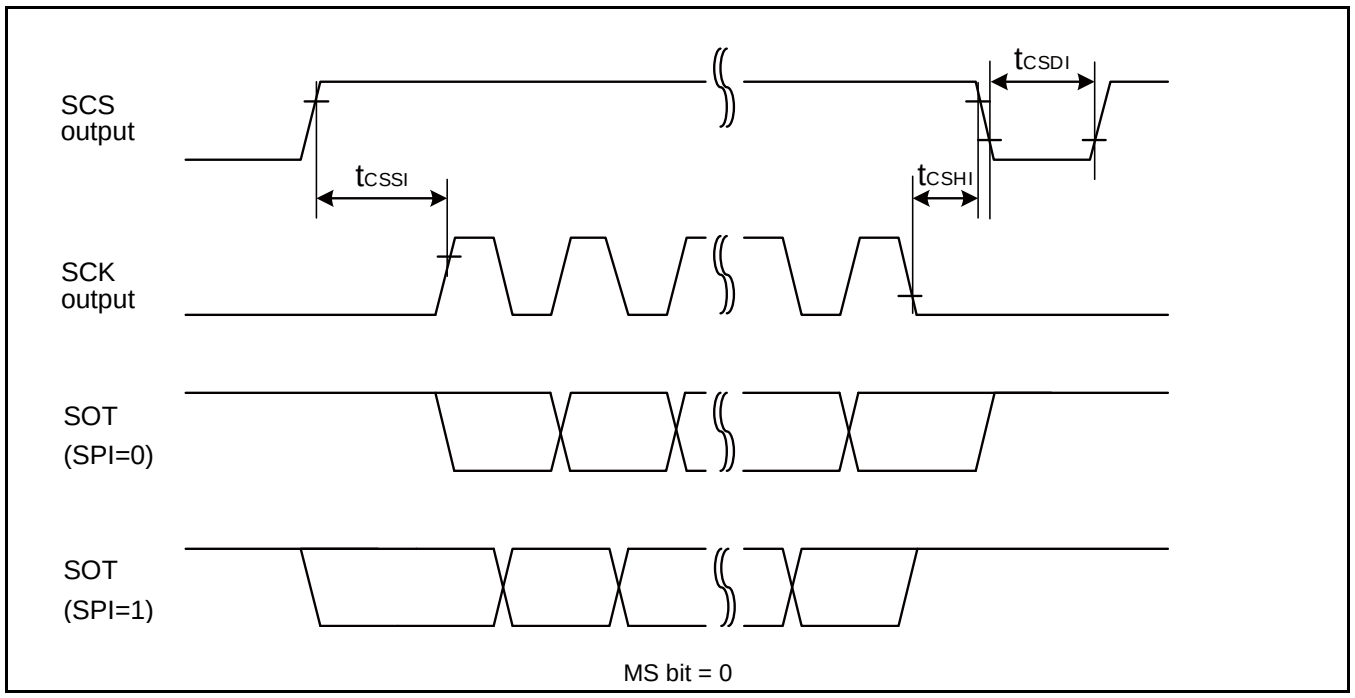
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



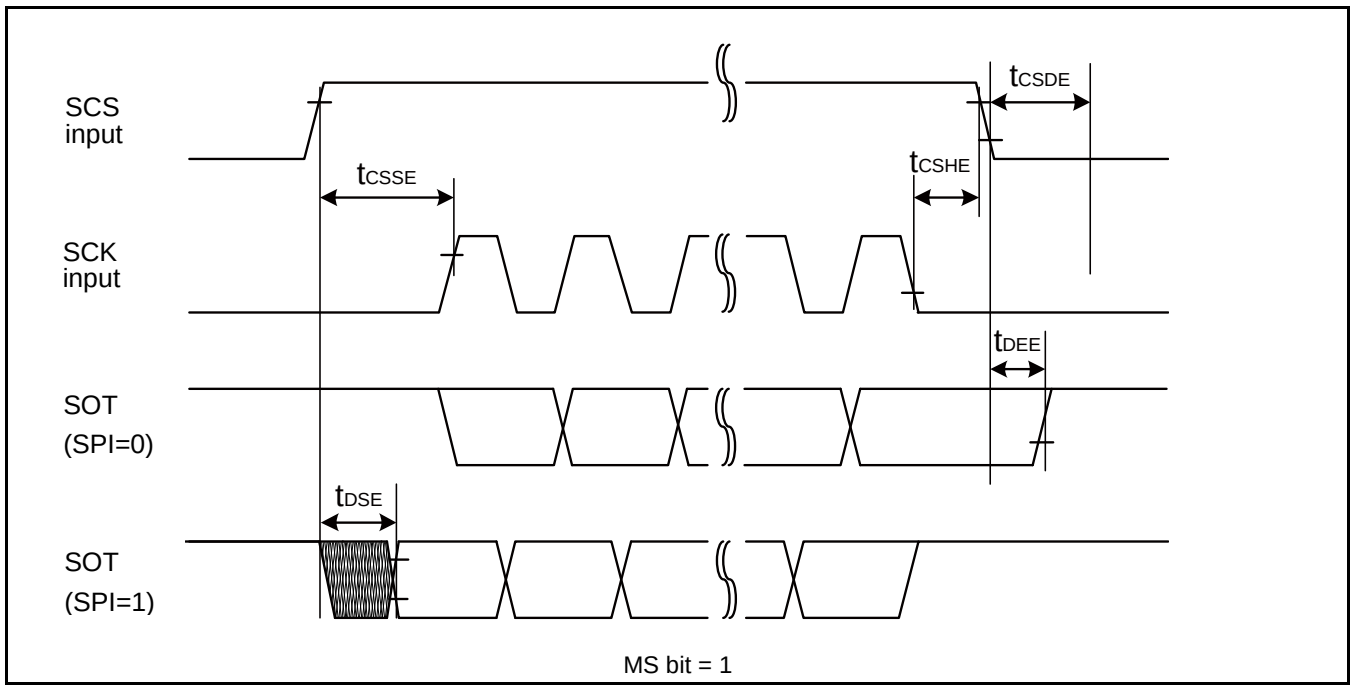
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

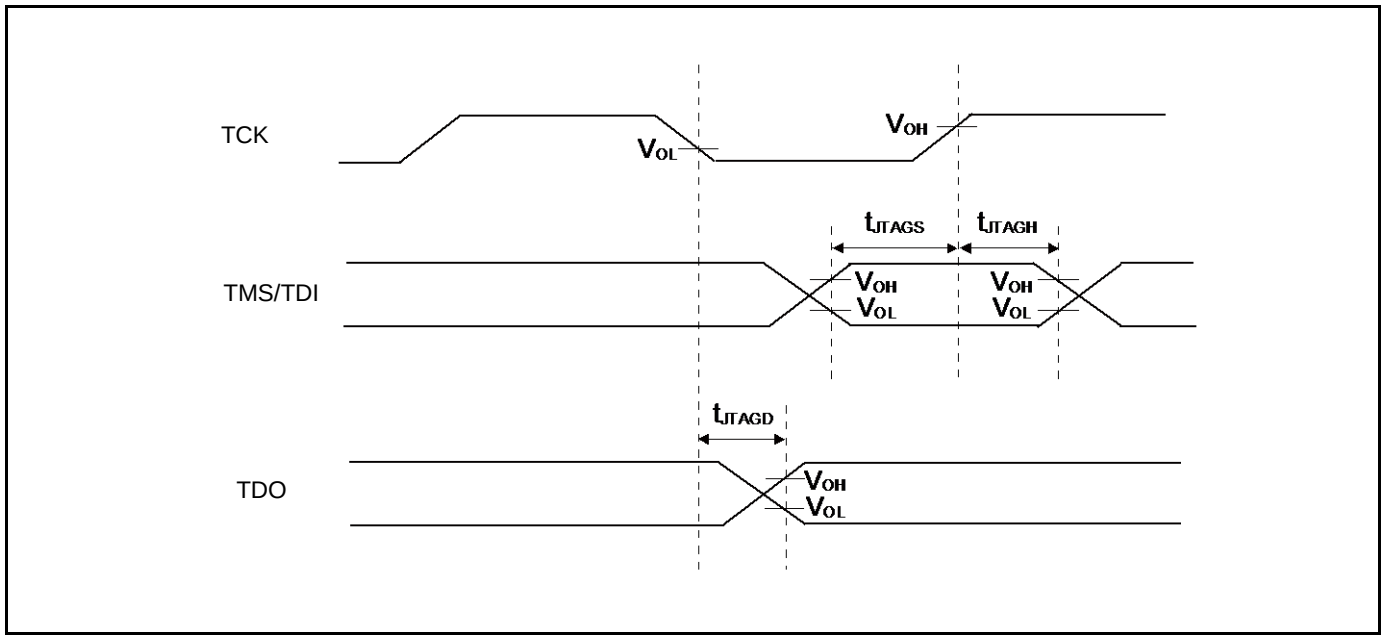
12.4.18 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

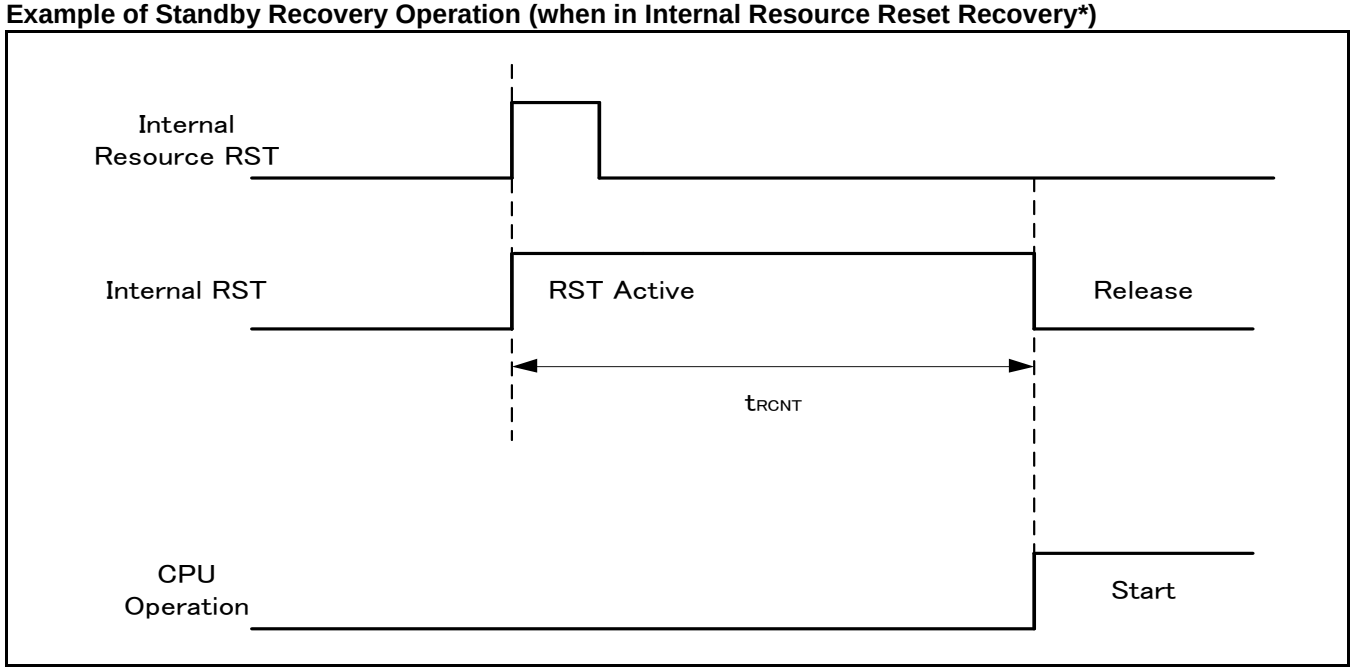
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

Note:

- *When the external load capacitance C_L = 30 pF.*



Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



*: Depending on the low-power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each low power consumption mode.*
  See Chapter 6: Low Power Consumption mode and Operations of Standby modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-On Reset Timing.*
- *In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.*
- *Internal resource reset indicates Watchdog reset and CSV reset.*