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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gh6h0agv2000a

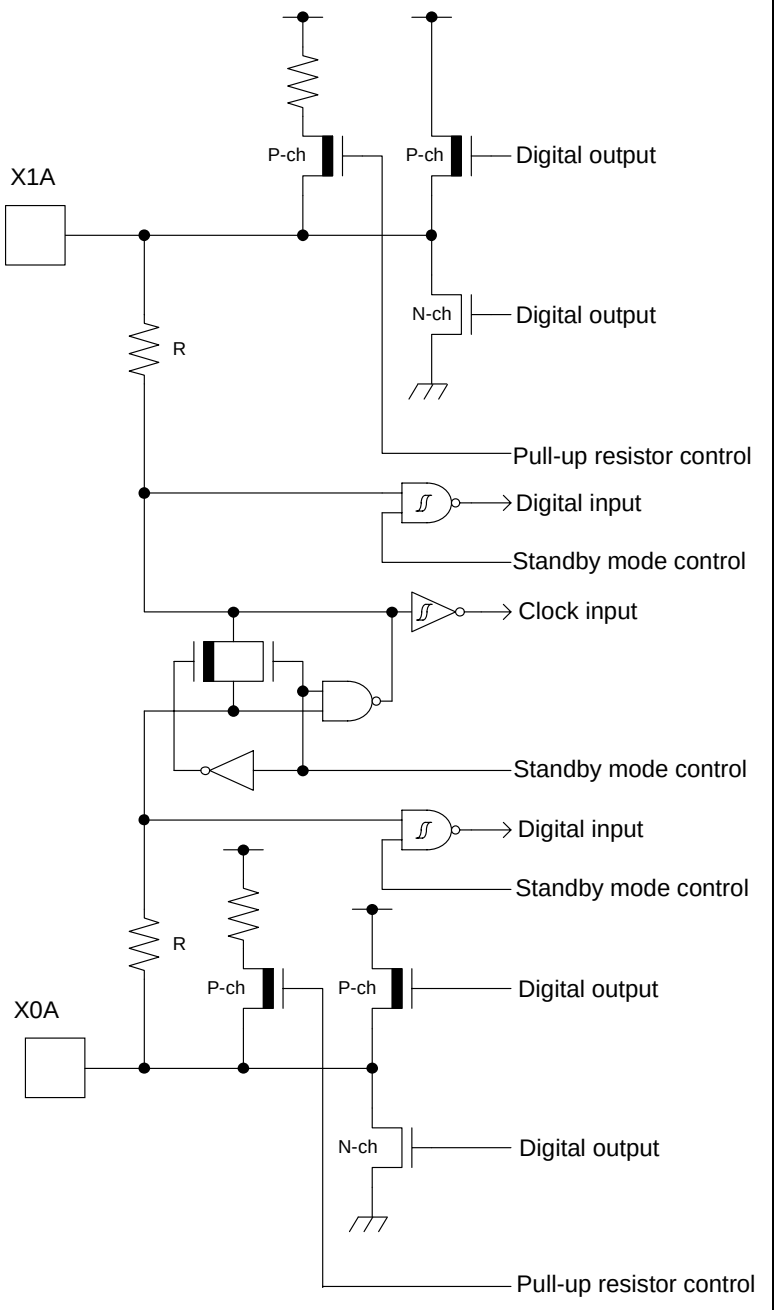
Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
58	-	PF0	E	K
		SCS73_1		
		RX0_2		
		TIOA15_1		
		INT22_1		
59	-	PF1	E	K
		TX0_2		
		TIOB15_1		
		INT23_1		
60	50	P48	L	K
		SIN1_0		
		MI2SDI1_0		
		DTTI1X_0		
		INT06_0		
		MRASX_0		
61	51	P49	L	I
		SOT1_0 (SDA1_0)		
		MI2SDO1_0		
		IC10_0		
		MCASX_0		
62	52	P4A	L	I
		SCK1_0 (SCL1_0)		
		MI2SCK1_0		
		IC11_0		
		MSDWEX_0		
63	53	P4B	L	K
		MI2SWS1_0		
		IC12_0		
		INT04_2		
		MCSX8_0		
64	54	P4C	L	K
		MI2SMCK1_0		
		IC13_0		
		INT05_2		
		MSDCKE_0		
65	55	P4D	L	K
		FRCK1_0		
		INT07_0		
		MSDCLK_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
119	95	P29 AN25 SCK5_0 (SCL5_0) INT09_2 MAD13_0	F	M
120	96	P28 AN26 SOT5_0 (SDA5_0) INT10_2 MAD14_0	F	M
121	97	P27 AN27 SIN5_0 INT24_0 MAD15_0	F	M
122	98	P26 ADTG_6 TIOA6_2 INT11_2 MAD16_0	E	M
123	99	P25 AN28 TIOB6_2 INT25_0 MAD17_0	F	M
124	100	P24 AN29 TIOA13_1 MAD18_0	F	L
125	101	P23 UHCONX1 AN30 SCK0_0 (SCL0_0) TIOB13_1	F	L
126	102	P22 AN31 SOT0_0 (SDA0_0) INT26_0	E	M

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
166	136	P6E ADTG_5 SCK4_1 (SCL4_1) INT29_0 E_PPS	E	W
167	-	P65 INT28_1	E	K
168	-	P64 CTS4_0 INT29_1	I	K
169	137	P63 ADTG_3 RTS4_0 INT30_0 MOEX_0	L	K
170	138	P62 SCK4_0 (SCL4_0) TIOB7_2 MWEX_0	L	I
171	139	P61 UHCONX0 SOT4_0 (SDA4_0) TIOA7_2 MALE_0 RTCCO_0 SUBOUT_0	L	I
172	140	P60 SIN4_0 INT31_0 WKUP3	I	Q
173	141	USBVCC0	-	-
174	142	P80 UDM0	H	R
175	143	P81 UDP0	H	R
176	144	VSS	-	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External interrupt	INT14_0	External interrupt request 14 input pin	160	130
	INT14_1		141	-
	INT15_0	External interrupt request 15 input pin	161	131
	INT15_1		142	-
	INT16_0	External interrupt request 16 input pin	20	17
	INT16_1		35	30
	INT17_0	External interrupt request 17 input pin	21	18
	INT17_1		36	31
	INT18_0	External interrupt request 18 input pin	22	19
	INT18_1		37	32
	INT19_0	External interrupt request 19 input pin	26	21
	INT19_1		38	33
	INT20_0	External interrupt request 20 input pin	70	60
	INT20_1		82	-
	INT21_0	External interrupt request 21 input pin	73	63
	INT21_1		83	-
	INT22_0	External interrupt request 22 input pin	76	66
	INT22_1		58	-
	INT23_0	External interrupt request 23 input pin	46	38
	INT23_1		59	-
	INT24_0	External interrupt request 24 input pin	121	97
	INT24_1		107	87
	INT25_0	External interrupt request 25 input pin	123	99
	INT25_1		97	81
	INT26_0	External interrupt request 26 input pin	126	102
	INT26_1		116	92
	INT27_0	External interrupt request 27 input pin	127	103
	INT27_1		117	93
	INT28_0	External interrupt request 28 input pin	158	128
	INT28_1		167	-
	INT29_0	External interrupt request 29 input pin	166	136
	INT29_1		168	-
	INT30_0	External interrupt request 30 input pin	169	137
	INT30_1		163	133
	INT31_0	External interrupt request 31 input pin	172	140
	INT31_1		164	134
	NMIX	Non-maskable interrupt input pin	128	104

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 0	SIN0_0	Multi-function serial interface ch 0 input pin	127	103
	SIN0_1		116	92
	SOT0_0 (SDA0_0)	Multi-function serial interface ch 0 output pin This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	126	102
	SOT0_1 (SDA0_1)		115	91
	SCK0_0 (SCL0_0)	Multi-function serial interface ch 0 clock I/O pin This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I^2C (operation mode 4)	125	101
	SCK0_1 (SCL0_1)		114	90
Multi-Function Serial 1	SIN1_0 (MI2SDI1_0)	Multi-function serial interface ch 1 input pin. SIN1 pin operates as MI2SDI1 when used as an I^2S pin (operation mode 2).	60	50
	SIN1_1 (MI2SDI1_1)		41	-
	SOT1_0 (SDA1_0) (MI2SDO1_0)	Multi-function serial interface ch 1 output pin This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4). SOT1 pin operates as MI2SDO1 when used as an I^2S pin (operation mode 2).	61	51
	SOT1_1 (SDA1_1) (MI2SDO1_1)		42	-
	SCK1_0 (SCL1_0) (MI2SCK1_0)	Multi-function serial interface ch 1 clock I/O pin This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I^2C (operation mode 4). SCK1 pin operates as MI2SCK1 when used as an I^2S pin (operation mode 2).	62	52
	SCK1_1 (SCL1_1) (MI2SCK1_1)		43	-
	MI2SWS1_0	I^2S word select (WS) output pin	63	53
	MI2SWS1_1		24	-
	MI2SMCK1_0	I^2S master clock I/O pin	64	54
	MI2SMCK1_1		25	-

Type	Circuit	Remarks
D		It is possible to select the sub oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 5 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA

List of Pin Behavior by Mode State

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Main crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enabled	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops*[1], it will be Hi-Z/ Internal input fixed at 0					
C	INITX input pin	Pull-up/ input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ input enabled	GPIO selected	Hi-Z/ input enabled	GPIO selected

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
O	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected						Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									

Current Explanation Diagram

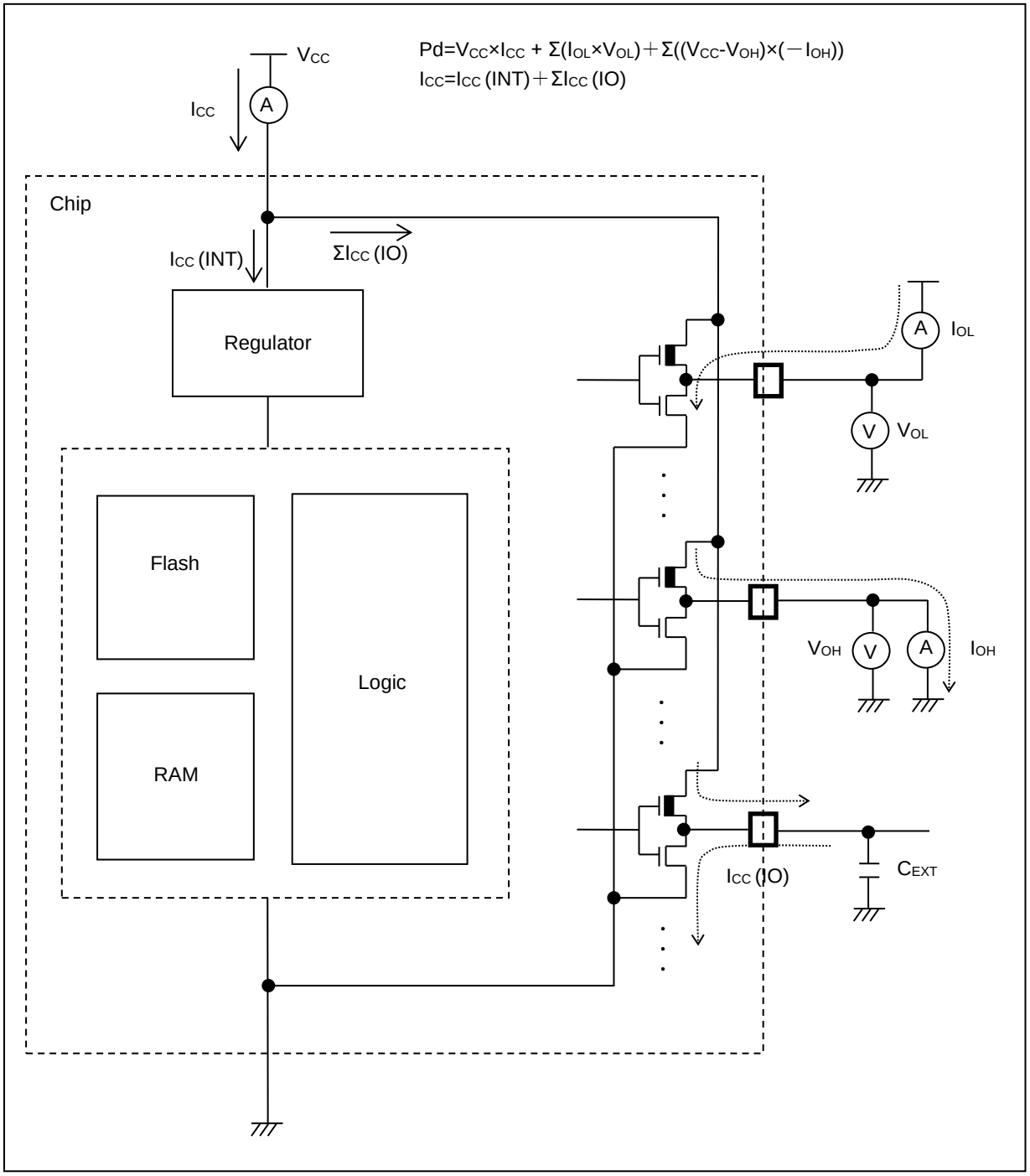


Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	180 MHz	82	140	mA	*3 When all peripheral clocks are on
				*6	160 MHz	74	132	mA	
					144 MHz	68	126	mA	
					120 MHz	58	116	mA	
					100 MHz	49	107	mA	
					80 MHz	40	98	mA	
					60 MHz	31	89	mA	
					40 MHz	22	80	mA	
					20 MHz	13	71	mA	
					8 MHz	7.5	65	mA	
					4 MHz	5.6	63	mA	
				*5	180 MHz	48	106	mA	*3 When all peripheral clocks are off
				*6	160 MHz	44	102	mA	
					144 MHz	41	99	mA	
					120 MHz	35	93	mA	
					100 MHz	30	88	mA	
					80 MHz	25	83	mA	
					60 MHz	20	78	mA	
					40 MHz	14	72	mA	
					20 MHz	8.7	66	mA	
					8 MHz	5.6	63	mA	
					4 MHz	4.5	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

7: With data access to a MainFlash memory.

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	180	MHz	

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

12.4.5 Operating Conditions of USB/Ethernet PLL (in the Case of Using Main Clock for Input Clock of PLL)

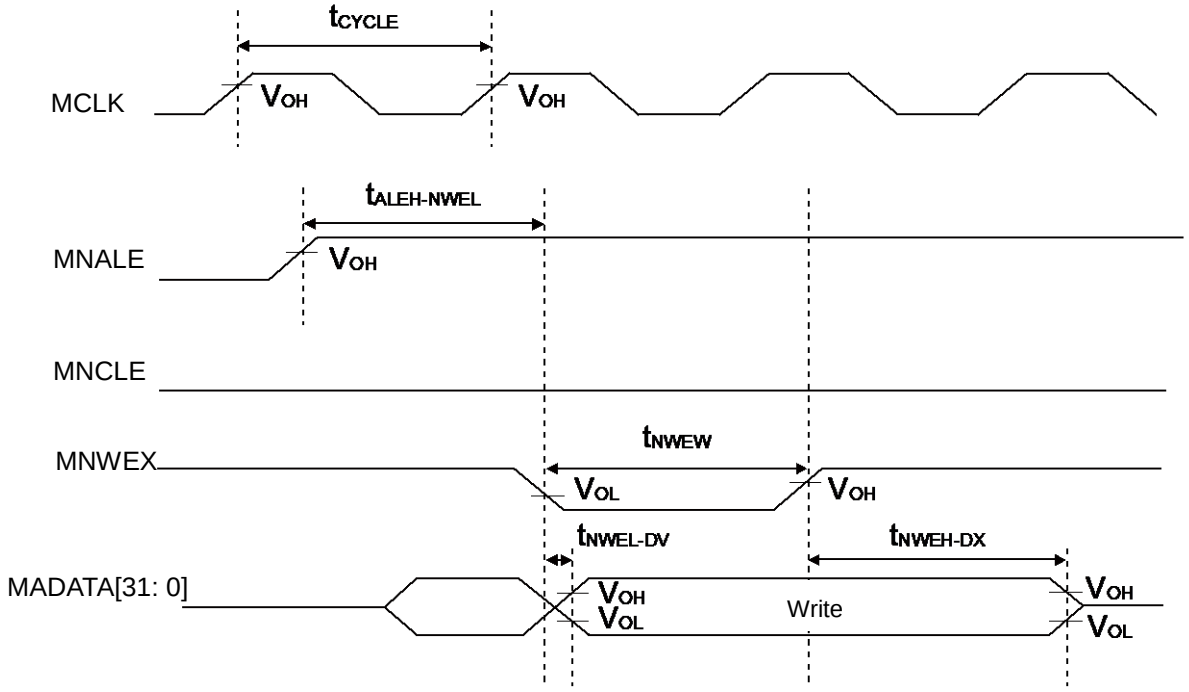
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB/Ethernet
USB/Ethernet clock frequency *2	f_{CLKPLL}	-	-	50	MHz	After the M frequency division

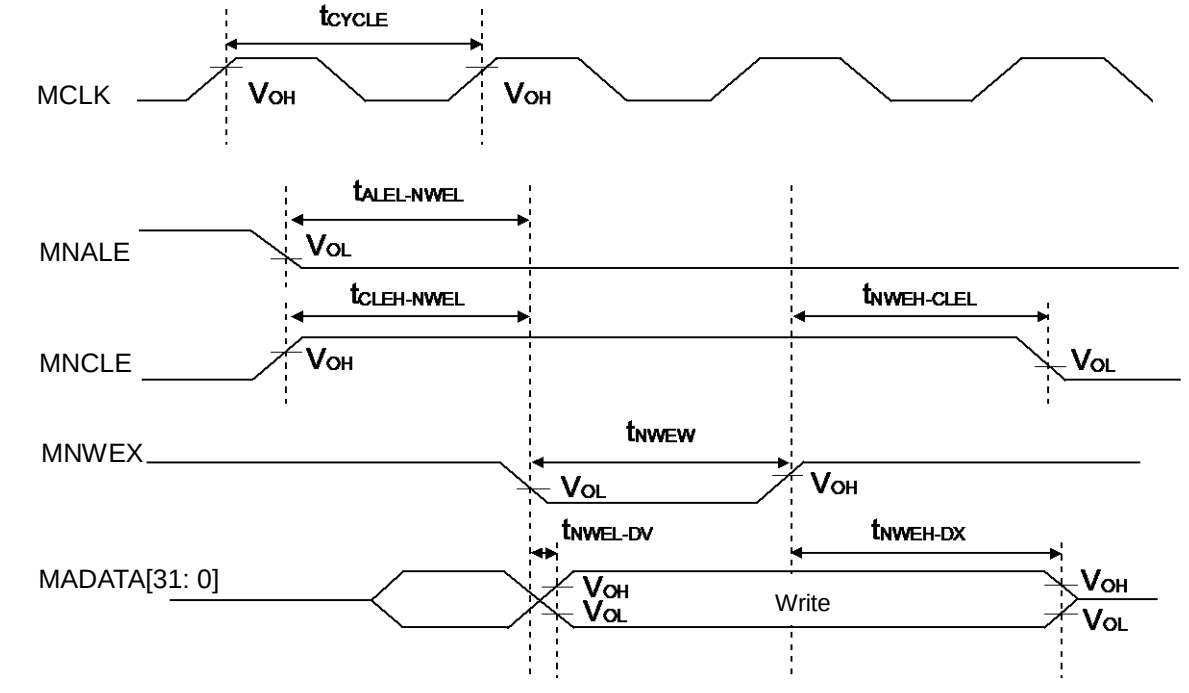
1: Time from when the PLL starts operating until the oscillation stabilizes

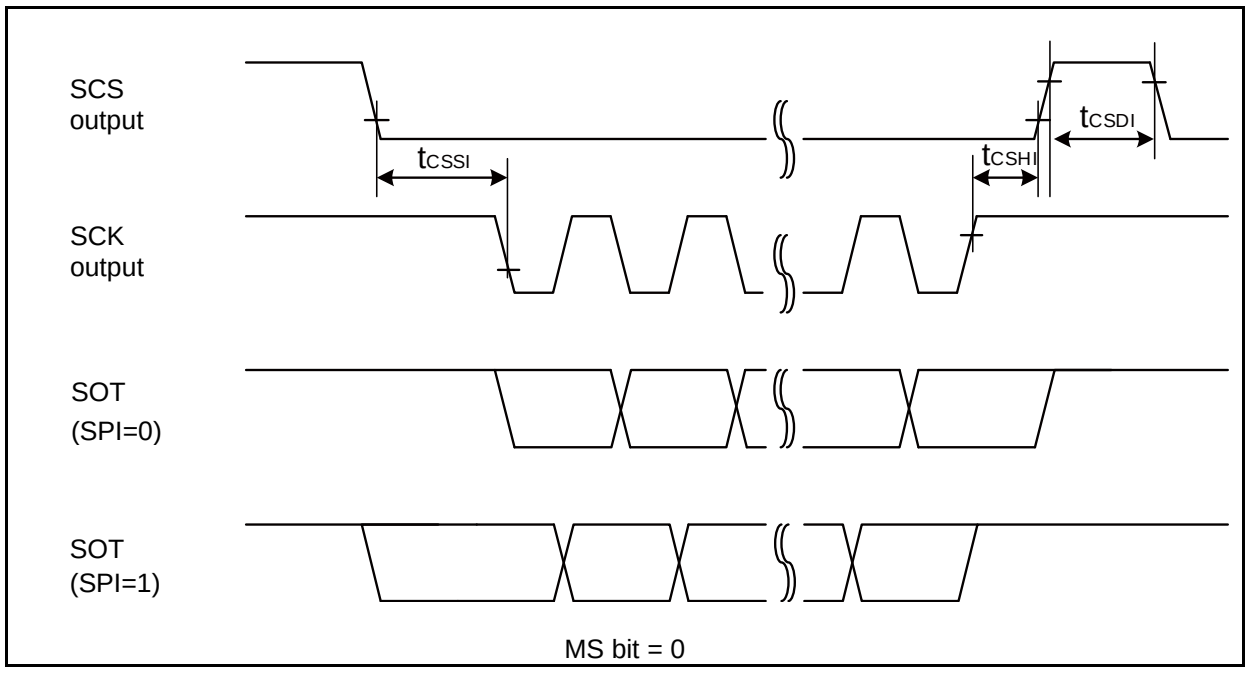
2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

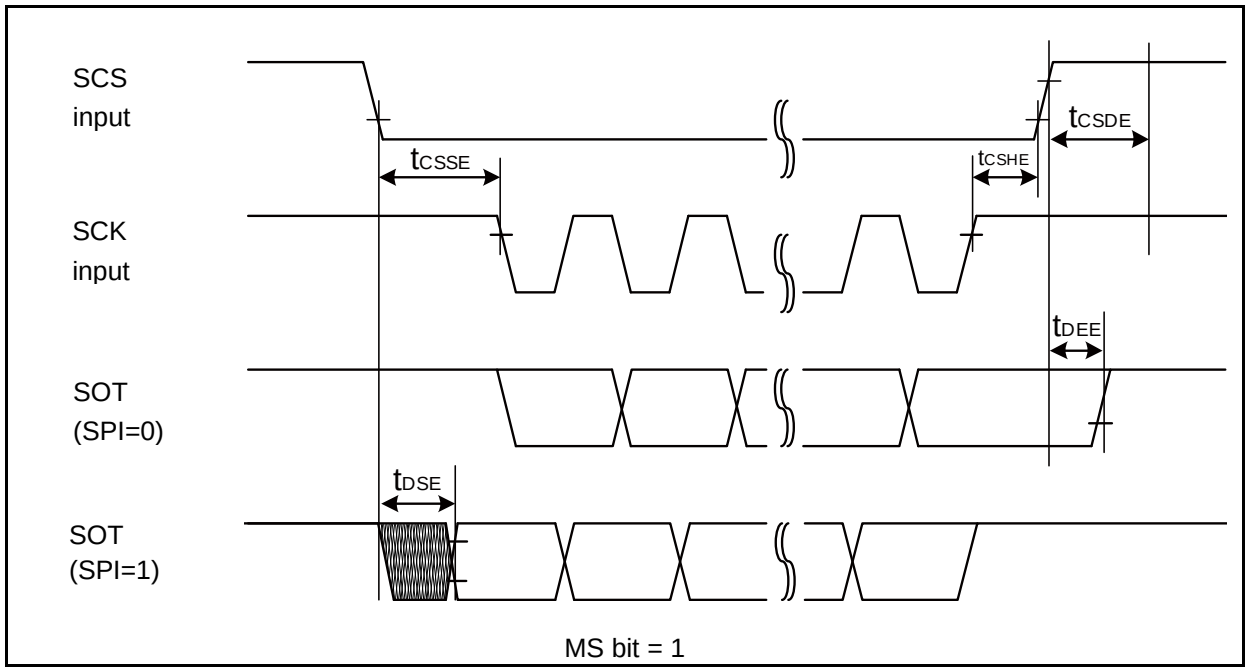
NAND Flash Address Write

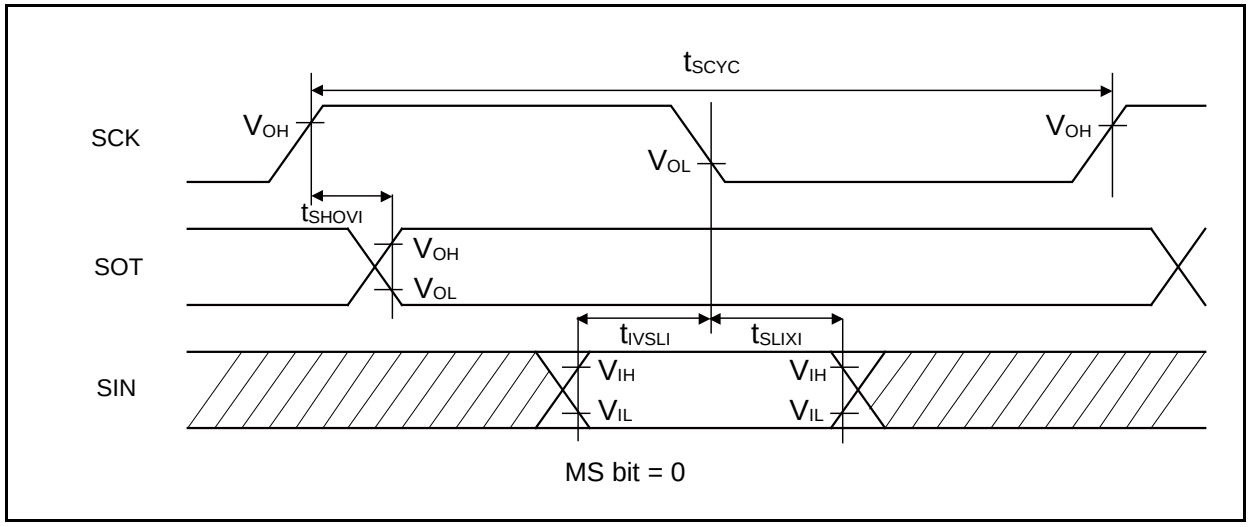


NAND Flash Command Write

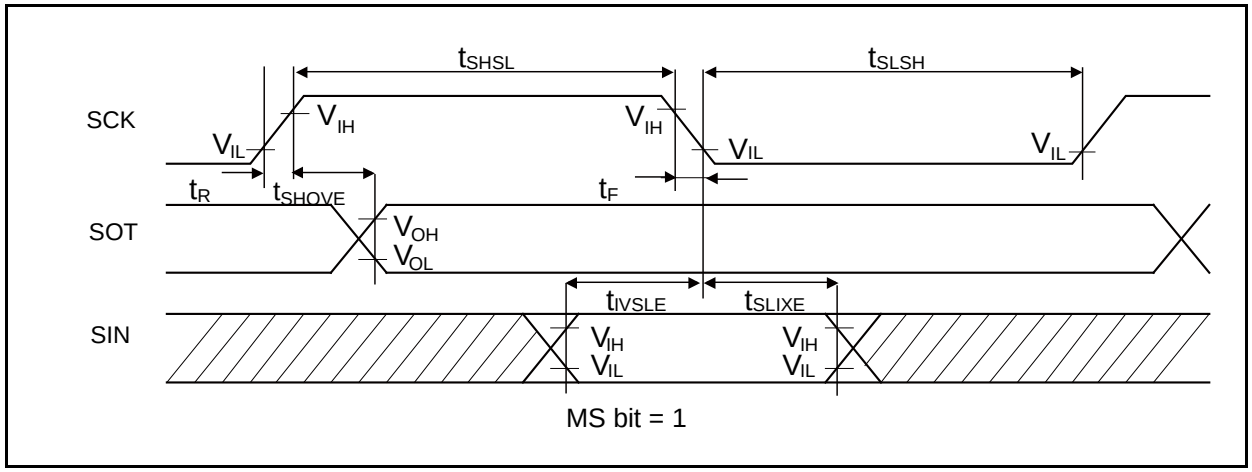



SCS
output
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSHI
tCSDI
MS bit = 0

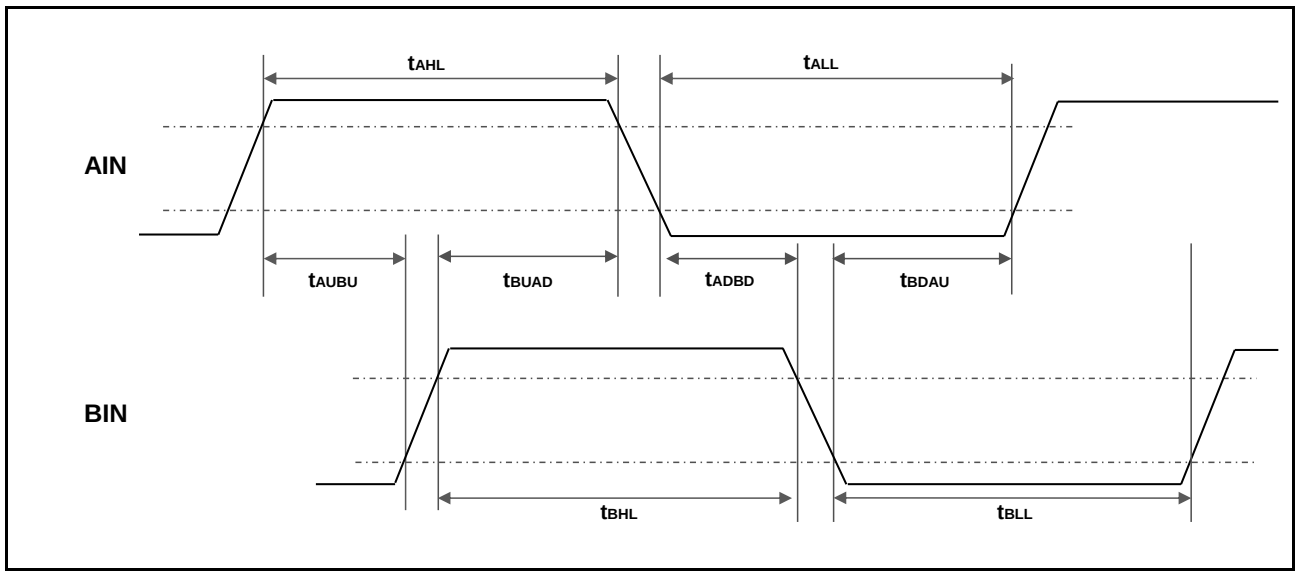

SCS
input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSHE
tCSDE
tDEE
tDSE
MS bit = 1

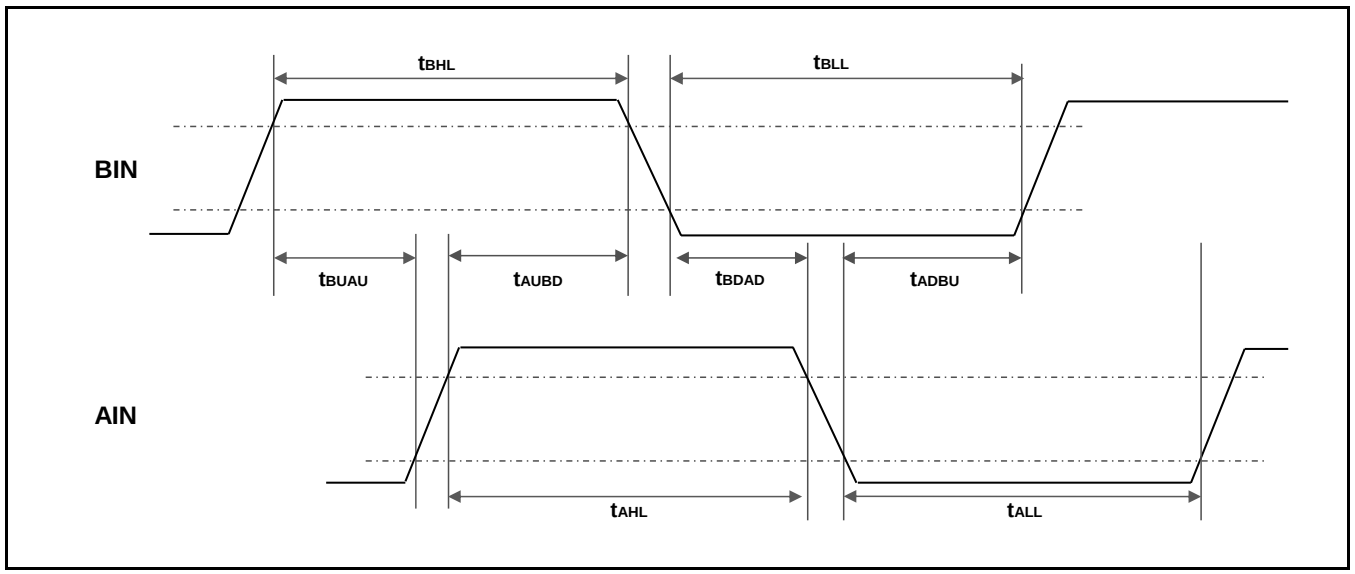


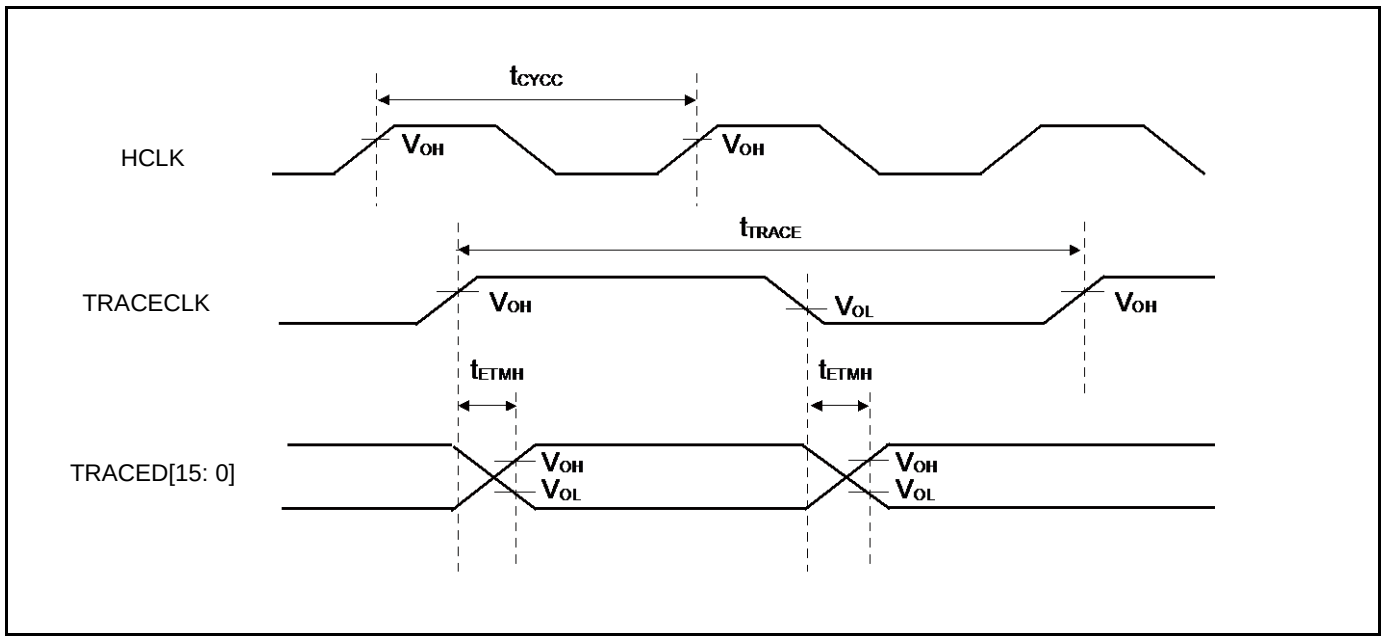
MS bit = 0



MS bit = 1

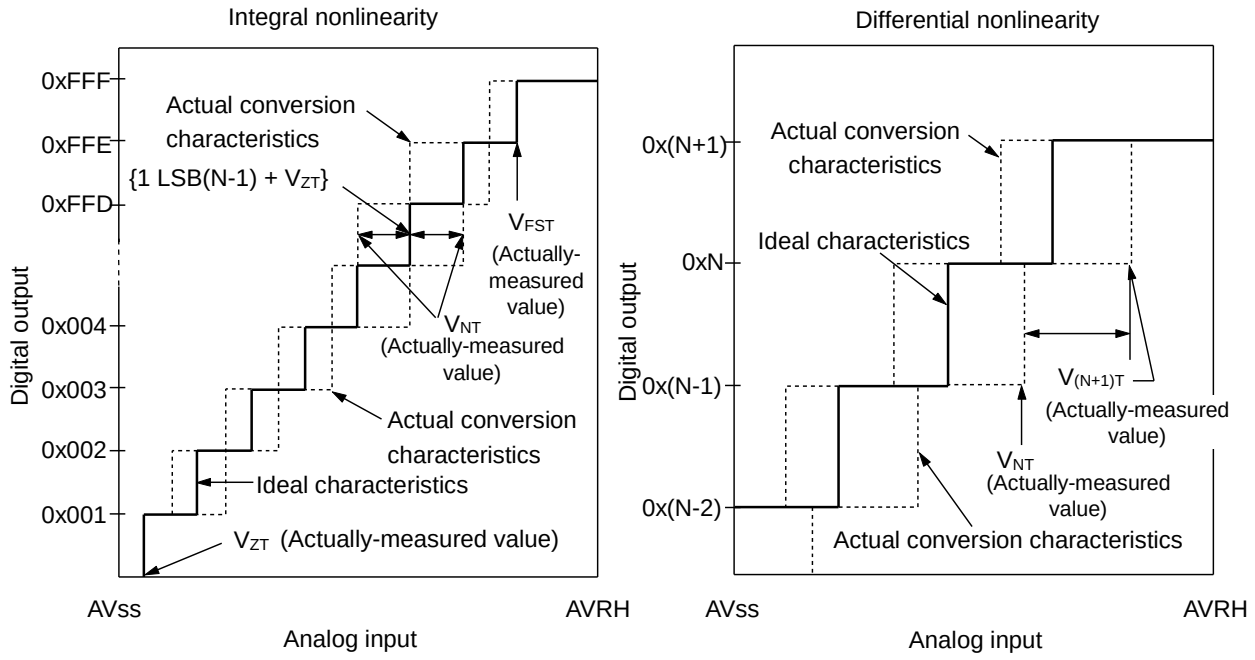

AIN
BIN
tAHL
tALL
tAUBU
tBUAD
tADBD
tBDAU
tBHL
tBLL


BIN
AIN
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tAHL
tALL


tCYCC
HCLK
VOH
VOH
tTRACE
TRACECLK
VOH
VOL
VOH
tETMH
tETMH
TRACED[15: 0]
VOH
VOL
VOH
VOL

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



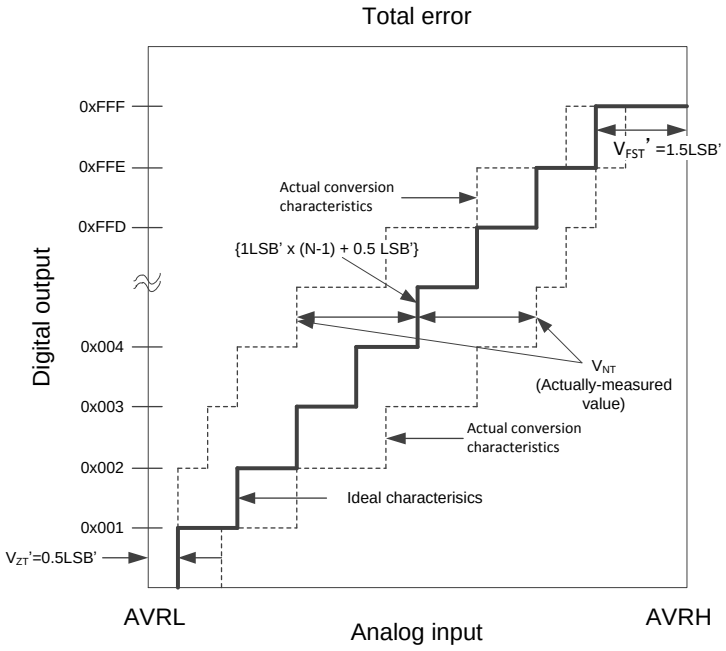
$$\text{Integral nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

■ Total error: A difference between actual value and theoretical value.
The overall error includes zero-transition voltage, full-scale transition voltage and linearity error.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N-1) + 0.5\ LSB'\}}{1\ LSB'} \quad [LSB]$$

$$1\ LSB'\ (\text{ideal value}) = \frac{AVRH - AVRL}{4096} \quad [V]$$

V_{ZT}' (ideal value) = AVRL + 0.5 LSB' [V]

V_{FST}' (ideal value) = AVRH - 1.5 LSB' [V]

V_{NT}': A voltage for causing transition of digital output from (N-1) to N

12.6 USB Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, $USBV_{CC}0$ = $USBV_{CC}1$ = 3.0V to 3.6V, V_{SS} = AV_{SS} = 0V)

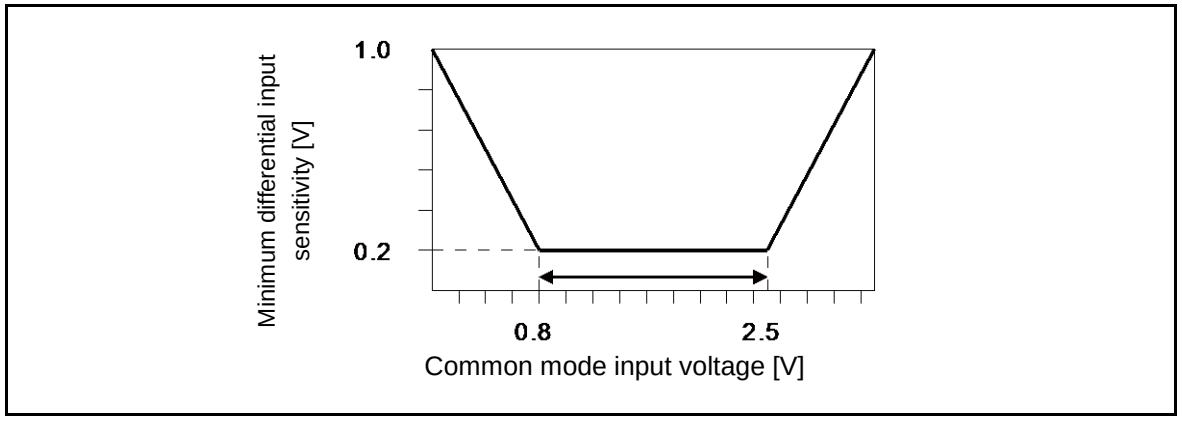
Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0/ UDM0, UDP1/ UDM1	-	2.0	$USBV_{CC}$ + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rise time	t_{FR}		Full-Speed	4	20	ns	*5
	Fall time	t_{FF}		Full-Speed	4	20	ns	*5
	Rise/fall time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rise time	t_{LR}		Low-Speed	75	300	ns	*7
	Fall time	t_{LF}		Low-Speed	75	300	ns	*7
	Rise/fall time matching	t_{LRFM}		Low-Speed	80	125	%	*7

1: The switching threshold voltage of the single-end-receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).

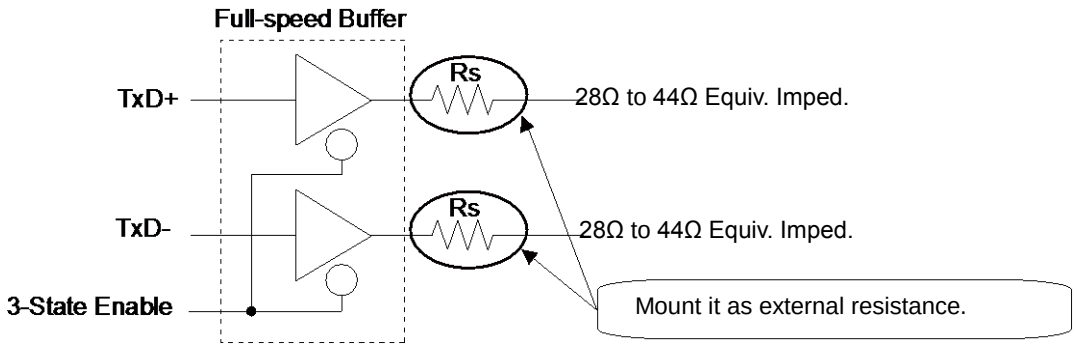
There is some hysteresis applied to lower noise sensitivity.

2: Use differential-receiver to receive USB differential data signal. Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

Above voltage range is the common mode input voltage range.

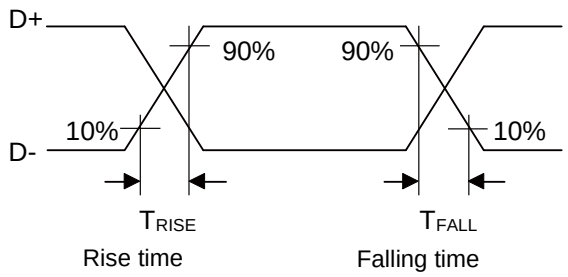


6: USB Full-speed connection is performed via twisted-pair cable shield with 90Ω ± 15% characteristic impedance (differential mode).
USB standard defines that the output impedance of the USB driver must be in the range from 28 Ω to 44 Ω. So, a discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommended value 27 Ω) series resistor Rs.



Rs series resistor 25Ω to 30Ω
Series resistor of 27Ω (recommendation value) must be added.
And, use "resistance with an uncertainty of 5% by E24 sequence."

7: They indicate rise time (t_{RISE}) and fall time (t_{FALL}) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.



Note:

- *See Low-Speed Load (Compliance Load) for conditions of external load.*