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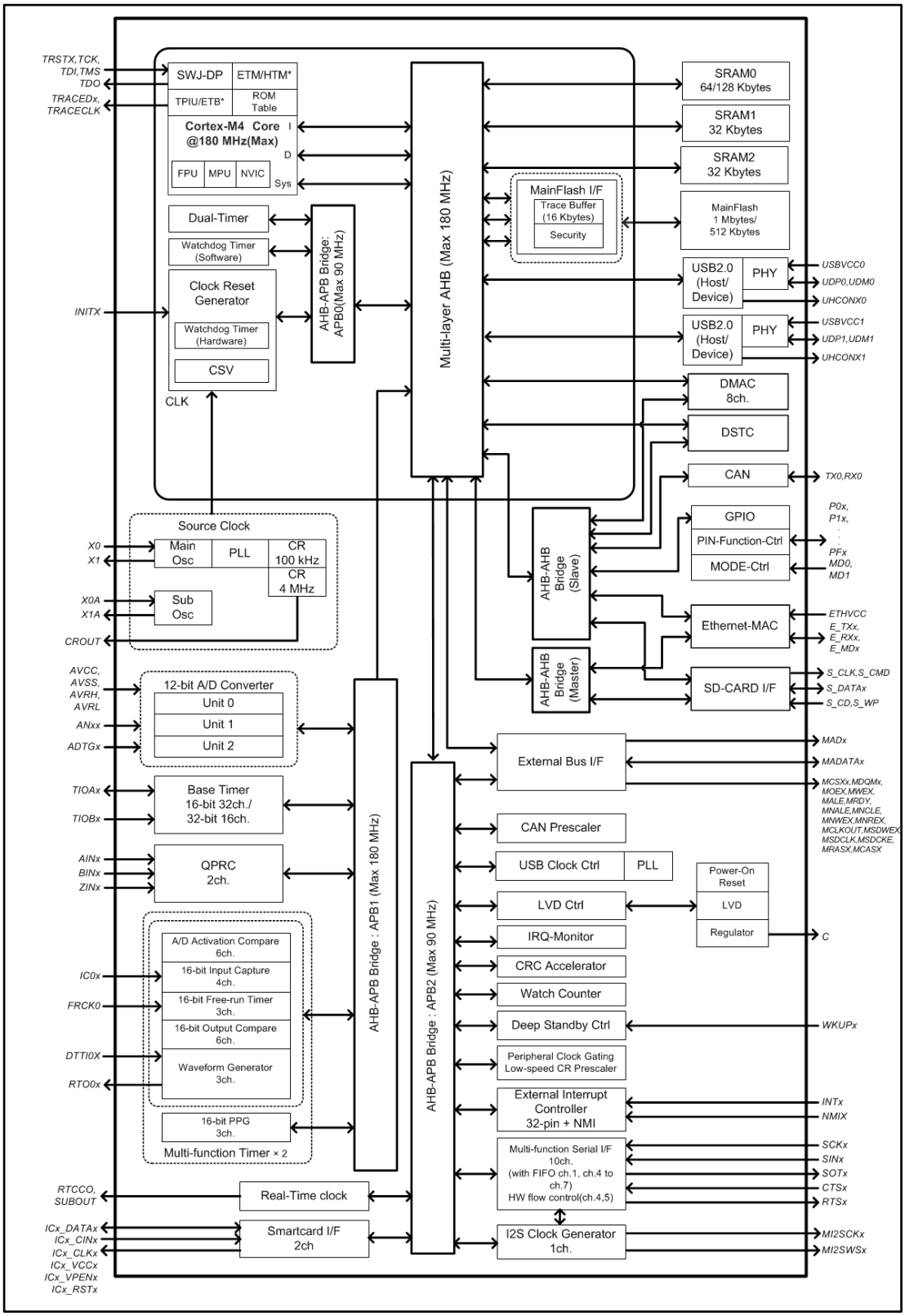
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

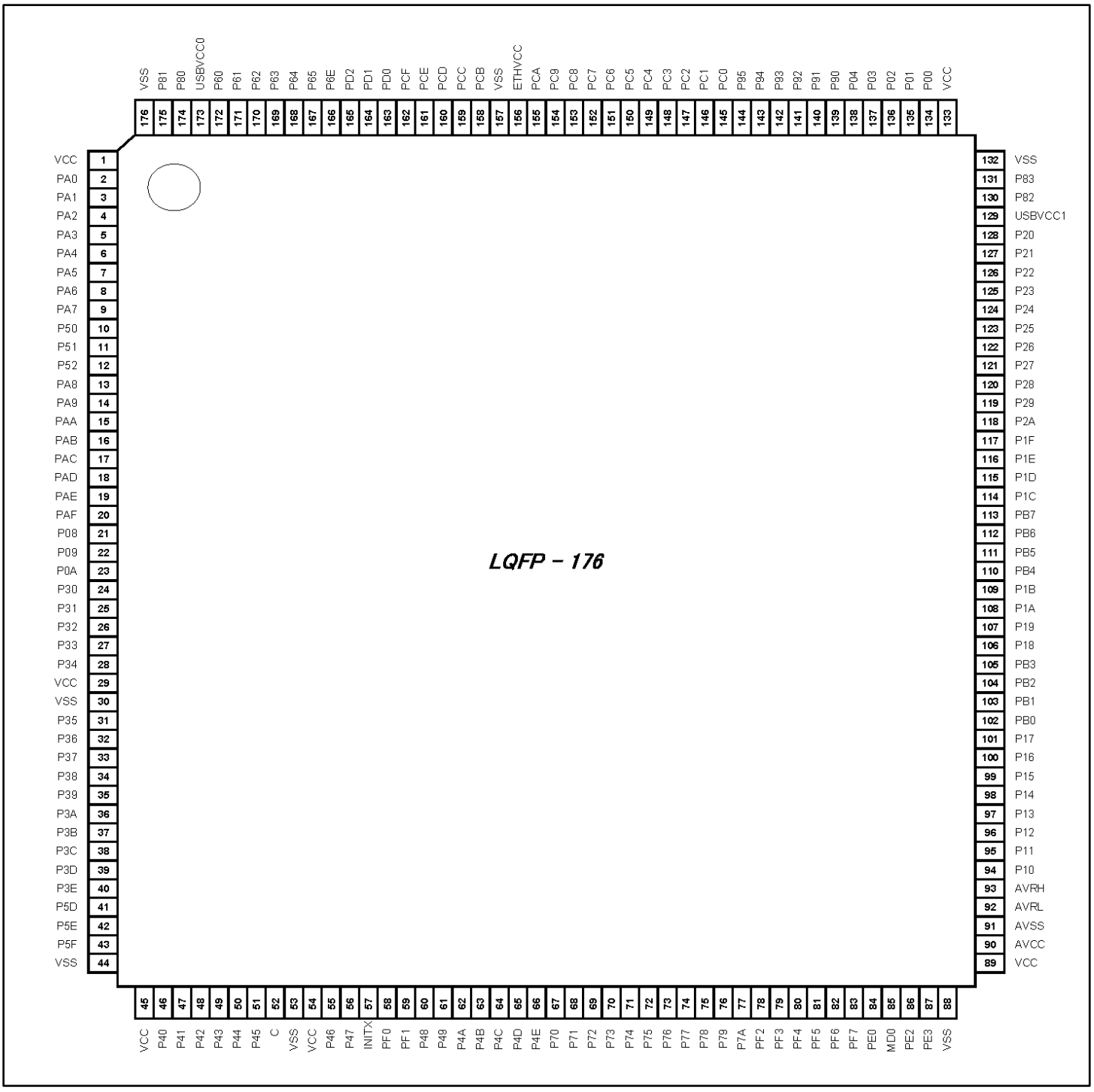
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gh8h0agv2000a

1. S6E2G Series Block Diagram



LQP176



Note:

- *Only the GPIO function is shown on GPIO pins. See the table in Pin Descriptions for the full, multiplexed signal name.*

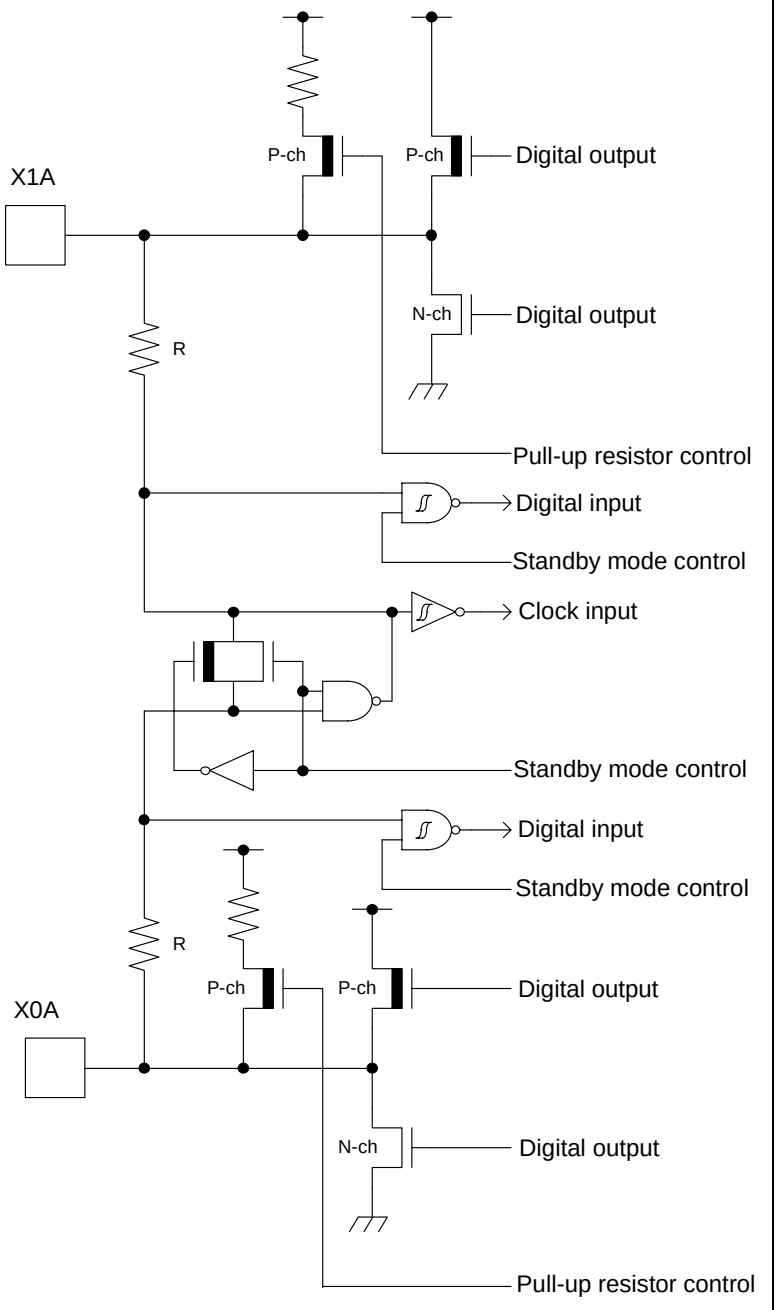
Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
166	136	P6E ADTG_5 SCK4_1 (SCL4_1) INT29_0 E_PPS	E	W
167	-	P65 INT28_1	E	K
168	-	P64 CTS4_0 INT29_1	I	K
169	137	P63 ADTG_3 RTS4_0 INT30_0 MOEX_0	L	K
170	138	P62 SCK4_0 (SCL4_0) TIOB7_2 MWEX_0	L	I
171	139	P61 UHCONX0 SOT4_0 (SDA4_0) TIOA7_2 MALE_0 RTCCO_0 SUBOUT_0	L	I
172	140	P60 SIN4_0 INT31_0 WKUP3	I	Q
173	141	USBVCC0	-	-
174	142	P80 UDM0	H	R
175	143	P81 UDP0	H	R
176	144	VSS	-	-

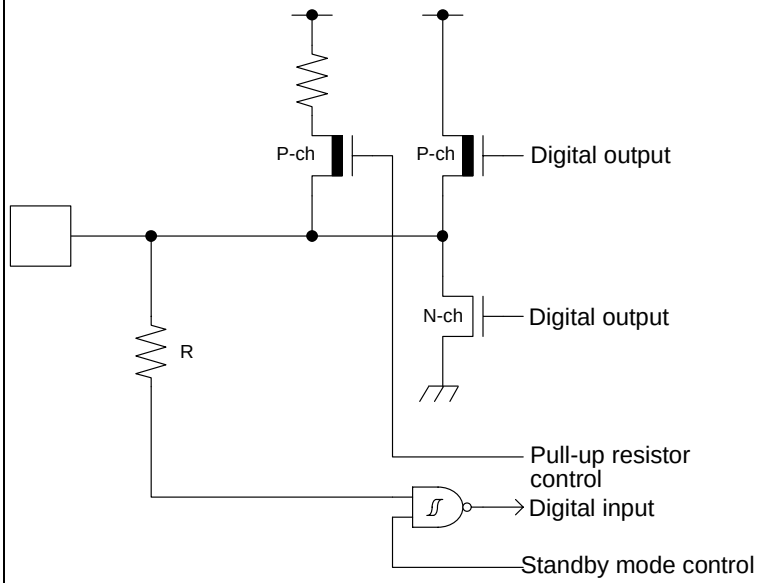
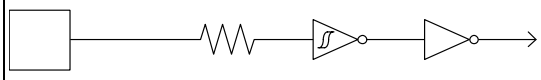
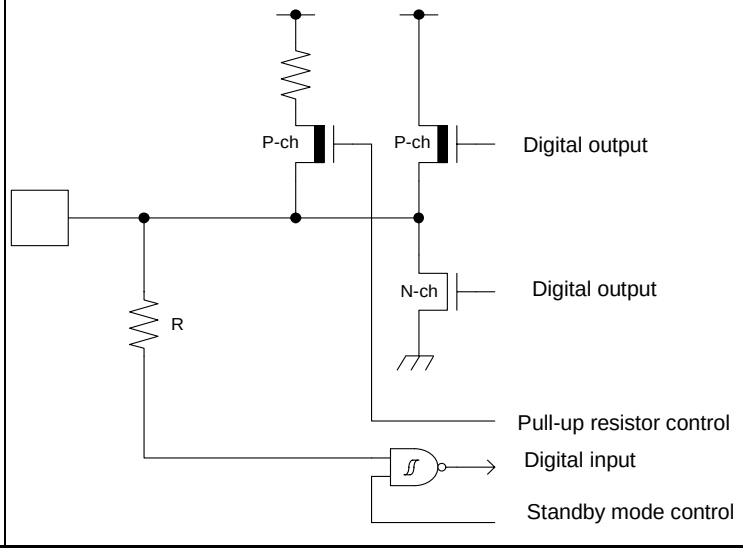
Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Base Timer 0	TIOA0_0	Base Timer ch 0 TIOA pin	46	38
	TIOA0_1		35	30
	TIOA0_2		94	78
	TIOB0_0	Base Timer ch 0 TIOB pin	69	59
	TIOB0_1		139	-
	TIOB0_2		95	79
Base Timer 1	TIOA1_0	Base Timer ch 1 TIOA pin	47	39
	TIOA1_1		36	31
	TIOA1_2		96	80
	TIOB1_0	Base Timer ch 1 TIOB pin	70	60
	TIOB1_1		140	-
	TIOB1_2		97	81
Base Timer 2	TIOA2_0	Base Timer ch 2 TIOA pin	48	40
	TIOA2_1		37	32
	TIOA2_2		98	82
	TIOB2_0	Base Timer ch 2 TIOB pin	71	61
	TIOB2_1		141	-
	TIOB2_2		99	83
Base Timer 3	TIOA3_0	Base Timer ch 3 TIOA pin	49	41
	TIOA3_1		38	33
	TIOA3_2		106	86
	TIOB3_0	Base Timer ch 3 TIOB pin	72	62
	TIOB3_1		142	-
	TIOB3_2		107	87
Base Timer 4	TIOA4_0	Base Timer ch 4 TIOA pin	50	42
	TIOA4_1		39	34
	TIOA4_2		108	88
	TIOB4_0	Base Timer ch 4 TIOB pin	73	63
	TIOB4_1		143	-
	TIOB4_2		109	89
Base Timer 5	TIOA5_0	Base Timer ch 5 TIOA pin	51	43
	TIOA5_1		40	35
	TIOA5_2		114	90
	TIOB5_0	Base Timer ch 5 TIOB pin	74	64
	TIOB5_1		144	-
	TIOB5_2		115	91
Base Timer 6	TIOA6_0	Base Timer ch 6 TIOA pin	147	117
	TIOA6_1		78	-
	TIOA6_2		122	98
	TIOB6_0	Base Timer ch 6 TIOB pin	146	116
	TIOB6_1		79	-
	TIOB6_2		123	99

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External interrupt	INT00_0	External interrupt request 00 input pin	2	2
	INT00_1		28	23
	INT00_2		8	8
	INT01_0	External interrupt request 01 input pin	7	7
	INT01_1		31	26
	INT01_2		24	-
	INT02_0	External interrupt request 02 input pin	13	10
	INT02_1		32	27
	INT02_2		9	9
	INT03_0	External interrupt request 03 input pin	16	13
	INT03_1		33	28
	INT03_2		41	-
	INT04_0	External interrupt request 04 input pin	49	41
	INT04_1		68	58
	INT04_2		63	53
	INT05_0	External interrupt request 05 input pin	66	56
	INT05_1		79	-
	INT05_2		64	54
	INT06_0	External interrupt request 06 input pin	60	50
	INT06_1		80	-
	INT06_2		69	59
	INT07_0	External interrupt request 07 input pin	65	55
	INT07_1		81	-
	INT07_2		77	67
	INT08_0	External interrupt request 08 input pin	94	78
	INT08_1		103	-
	INT08_2		118	94
	INT09_0	External interrupt request 09 input pin	100	84
	INT09_1		104	-
	INT09_2		119	95
	INT10_0	External interrupt request 10 input pin	106	86
	INT10_1		110	-
	INT10_2		120	96
	INT11_0	External interrupt request 11 input pin	109	89
	INT11_1		111	-
	INT11_2		122	98
	INT12_0	External interrupt request 12 input pin	162	132
	INT12_1		139	-
	INT13_0	External interrupt request 13 input pin	152	122
	INT13_1		140	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P00	General-purpose I/O port 0	134	110
	P01		135	111
	P02		136	112
	P03		137	113
	P04		138	114
	P08		21	18
	P09		22	19
	P0A		23	20
	P10	General-purpose I/O port 1	94	78
	P11		95	79
	P12		96	80
	P13		97	81
	P14		98	82
	P15		99	83
	P16		100	84
	P17		101	85
	P18		106	86
	P19		107	87
	P1A		108	88
	P1B		109	89
	P1C		114	90
	P1D		115	91
	P1E		116	92
	P1F		117	93
	P20	General-purpose I/O port 2	128	104
	P21		127	103
	P22		126	102
	P23		125	101
	P24		124	100
	P25		123	99
	P26		122	98
	P27		121	97
	P28		120	96
	P29		119	95
	P2A		118	94

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	121	97
	SIN5_1		140	-
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I²C (operation mode 4).	120	96
	SOT5_1 (SDA5_1)		141	-
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I²C (operation mode 4).	119	95
	SCK5_1 (SCL5_1)		142	-
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	118	94
	CTS5_1		143	-
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	117	93
	RTS5_1		144	-
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	73	63
	SIN6_1		100	84
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I²C (operation mode 4).	74	64
	SOT6_1 (SDA6_1)		101	85
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I²C (operation mode 4).	75	65
	SCK6_1 (SCL6_1)		102	-
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	76	66
	SCS60_1		103	-
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	77	67
	SCS61_1		104	-
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	78	-
	SCS62_1		105	-
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	79	-
	SCS63_1		110	-

Type	Circuit	Remarks
D		It is possible to select the sub oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 5 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA

Type	Circuit	Remarks
I		・ CMOS level output ・ CMOS level hysteresis input ・ 5 V tolerant ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA ・ Available to control of PZR registers (pseudo-open drain control) ・ For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856).
J		CMOS level hysteresis input
K		・ CMOS level output ・ TTL level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA

Latch-Up

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic pnpn junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

10. Memory Map

Memory Map (1)

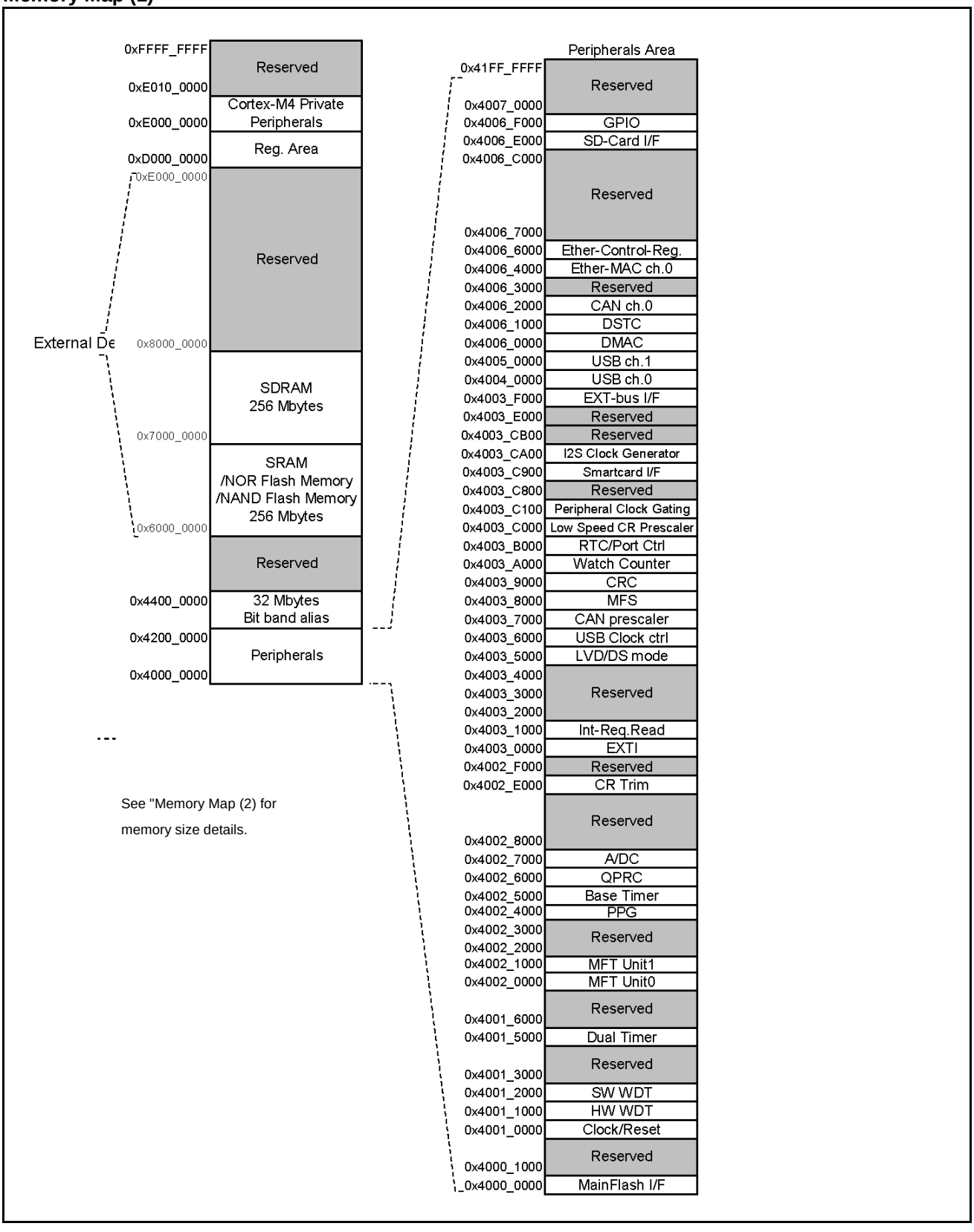


Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7 (PLL)	*5	72 MHz	54	112	mA	*3 When all peripheral clocks are on
					60 MHz	47	105	mA	
					48 MHz	39	97	mA	
					36 MHz	31	89	mA	
					24 MHz	23	81	mA	
					12 MHz	14	72	mA	
					8 MHz	11	69	mA	
					4 MHz	7.2	65	mA	
				*5	72 MHz	37	95	mA	*3 When all peripheral clocks are off
					60 MHz	33	91	mA	
					48 MHz	28	86	mA	
					36 MHz	23	81	mA	
					24 MHz	17	75	mA	
					12 MHz	11	69	mA	
					8 MHz	8.3	66	mA	
					4 MHz	5.9	63	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

6: With data access to a MainFlash memory.

7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	180	MHz	

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

12.4.5 Operating Conditions of USB/Ethernet PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB/Ethernet
USB/Ethernet clock frequency *2	f_{CLKPLL}	-	-	50	MHz	After the M frequency division

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↓ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t_{DEE}		0	-	0	-	ns

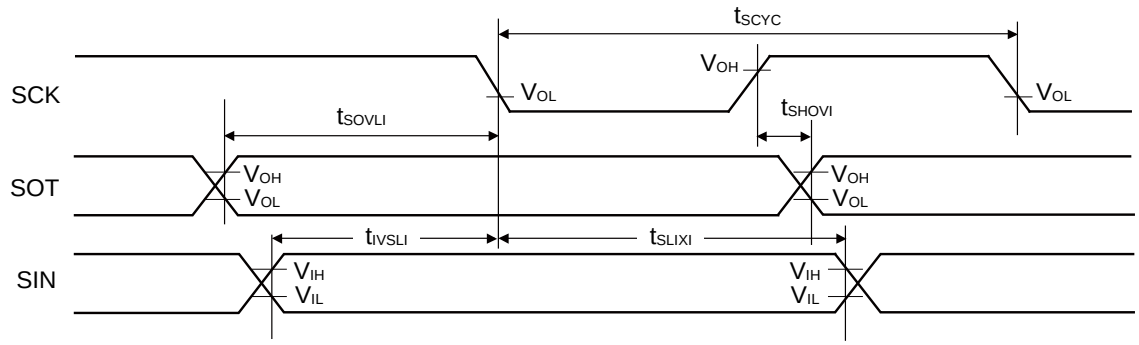
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

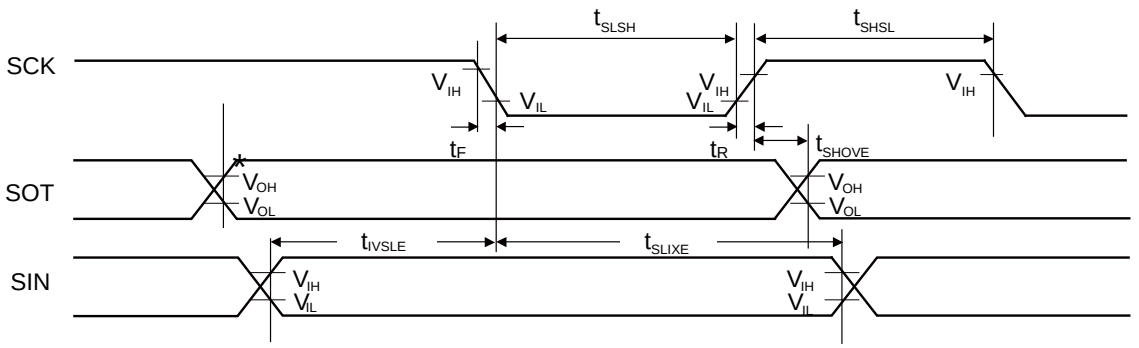
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

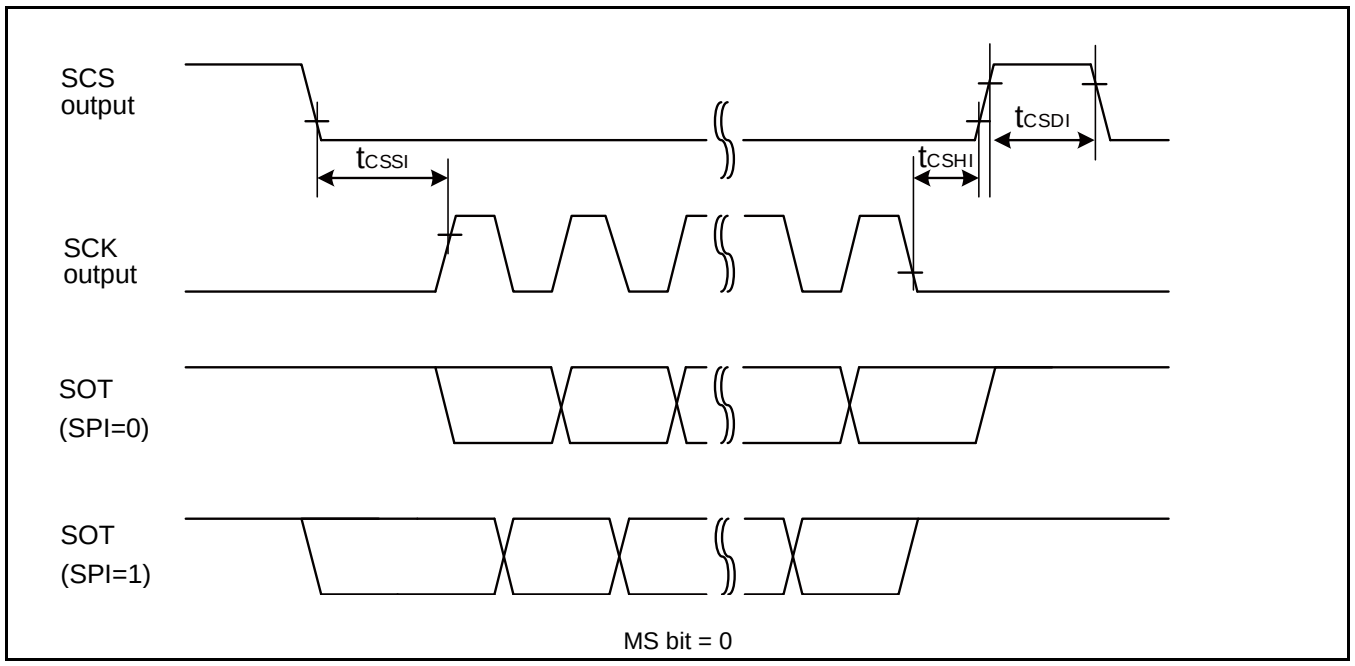


MS bit = 0

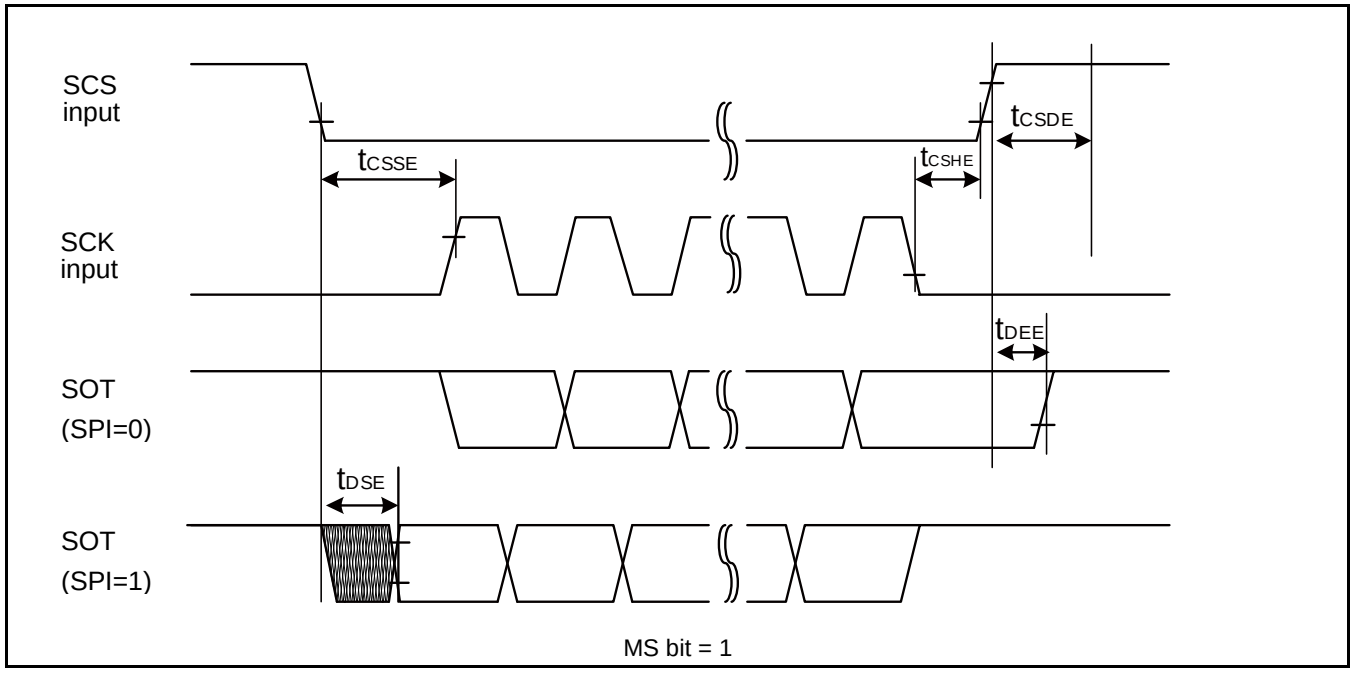


MS bit = 1

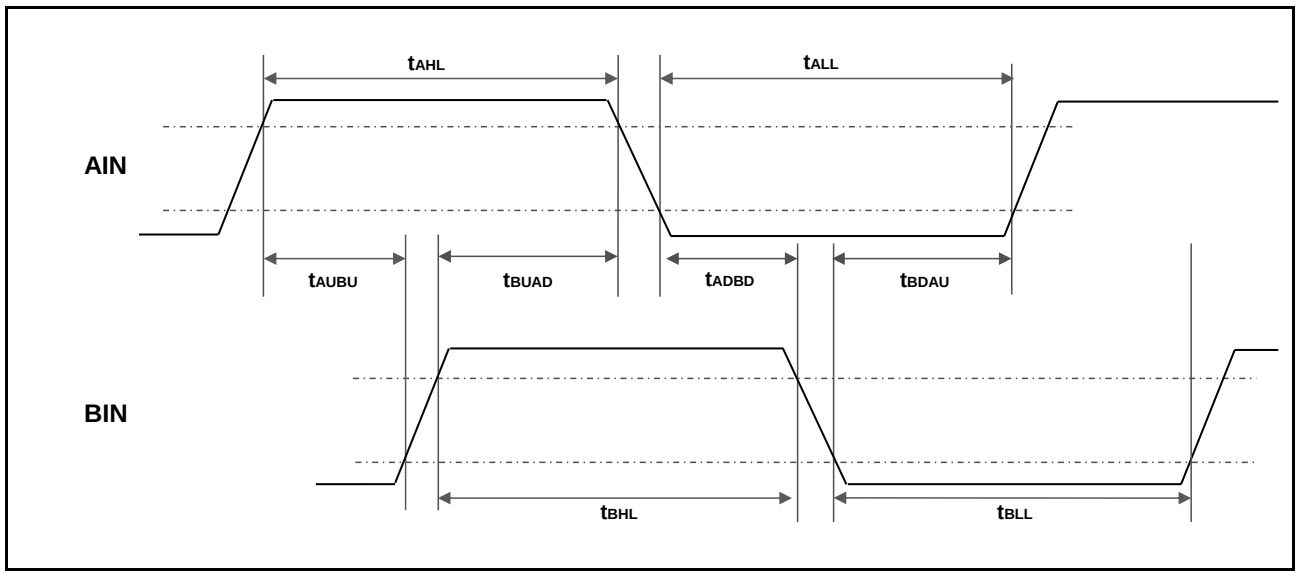
*: Changes when writing to TDR register

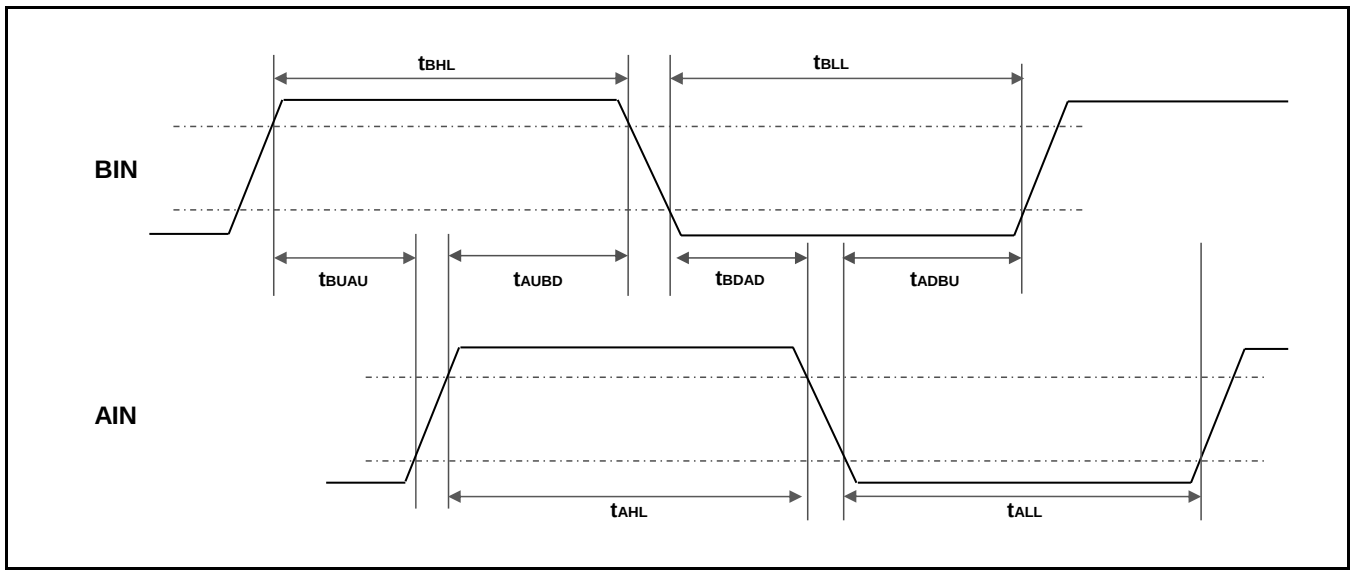


MS bit = 0



MS bit = 1


AIN
BIN
tAHL
tALL
tAUBU
tBUAD
tADBD
tBDAU
tBHL
tBLL

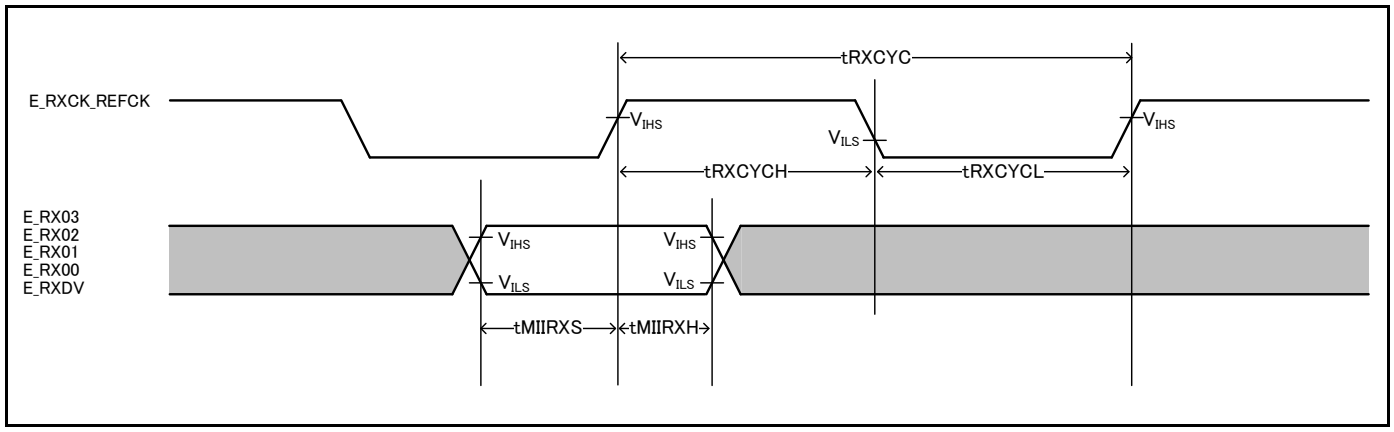

BIN
AIN
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tAHL
tALL

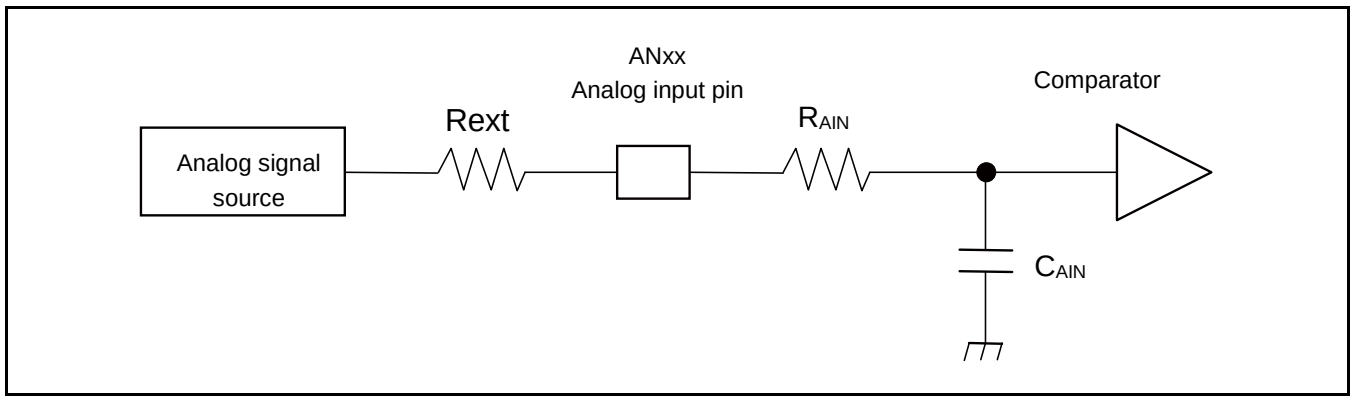
MII Receiving (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Receiving clock cycle time*	t_{RXCYC}	E_RXCK_REFCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Receiving clock High pulse width duty cycle	t_{RXCYCH}	E_RXCK_REFCK	t_{RXCYCH}/t_{RXCYC}	35	65	%
Receiving clock Low pulse width duty cycle	t_{RXCYCL}	E_RXCK_REFCK	t_{RXCYCL}/t_{RXCYC}	35	65	%
Received data → REFCK ↑Setup time	t_{MIIRXS}	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	5	-	ns
REFCK ↑ → Received data Hold time	t_{MIIRXH}	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	2	-	ns

*: The receiving clock 100Mbps is fixed to 25MHz or 2.5MHz in the MII specifications.
The clock accuracy should meet the PHY-device specifications.





(Equation 1) $t_S \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.2 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V

Input resistance of A/D = 1.8 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 12.05 pF at 2.7 V ≤ AV_{CC} ≤ 5.5 V

Rext: Output impedance of external circuit

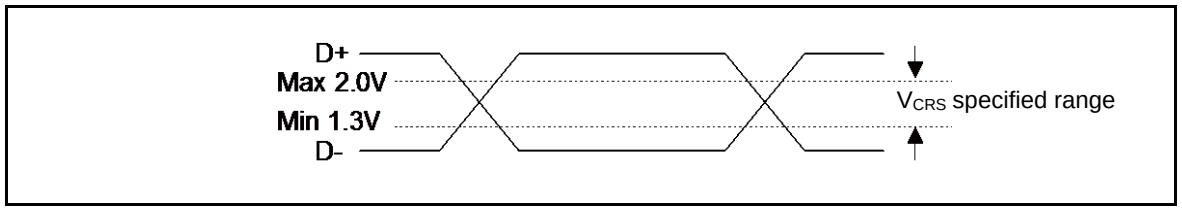
(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

3: The output drive capability of the driver is below 0.3 V at low state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the VSS and 1.5 kΩ load) at high state (V_{OH}).

4: The cross voltage of the external differential output signal (D +/D −) of USB I/O buffer is within 1.3 V to 2.0 V.



5: They indicate rise time (t_{RISE}) and fall time (t_{FALL}) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, t_R/t_F ratio is regulated as within ± 10% to minimize RFI emission.