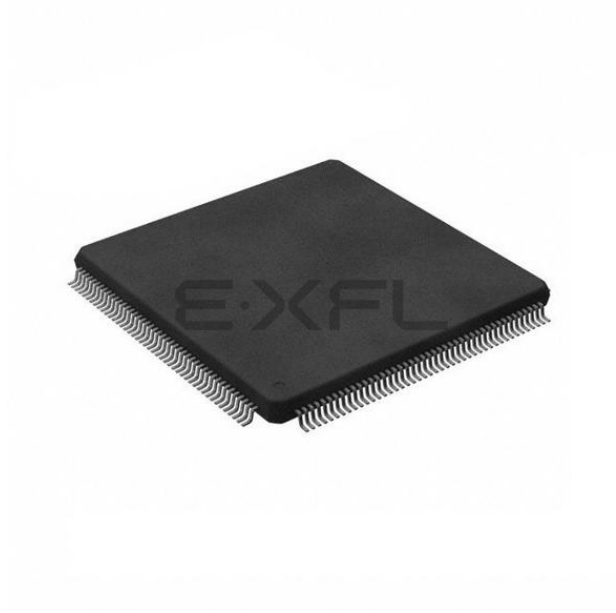

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gk6j0agv2000a

4. Product Features in Detail

32-bit ARM Cortex-M4F Core

- Up to 180 MHz frequency operation
- FPU built-in
- Support DSP instructions
- Memory protection unit (MPU): improves the reliability of an embedded system
- Integrated nested vectored interrupt controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit system timer (Sys Tick): system timer for OS task management

On-chip Memories

- Flash memory

This series is on-chip flash memories.

  - Up to 1024 Kbytes
  - Built-in flash accelerator for zero wait state
  - Security function for code protection

- SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to the I-code bus and D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to system bus of Cortex-M4F core.

  - SRAM0: up to 128 Kbytes
  - SRAM1: 32 Kbytes
  - SRAM2: 32 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-/32-bit data width
- Up to 25-bit address bus
- Supports address/data multiplexing
- Supports external RDY function
- Supports scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key
  - **Note:** It is necessary to use the Cypress provided software library to use the scramble function.

USB Interface (Max two channels)

The USB interface is composed of a Device and a Host.

- USB Device
  - USB 2.0 Full-speed supported
  - Max 6 EndPoint supported
    - EndPoint 0 is control transfer
    - EndPoint 1,2 can be selected bulk-transfer, interrupt-transfer or isochronous-transfer
    - EndPoint 3 to 5 can select bulk-transfer or interrupt-transfer
  - EndPoint 1 to 5 comprise double buffer
  - The size of each endpoint is as follows.
    - Endpoint 0, 2 to 5: 64 byte
    - EndPoint 1: 256 byte
- USB Host
  - USB2.0 Full-Speed/Low-Speed supported
  - Bulk-transfer, interrupt-transfer, and isochronous-transfer support
  - USB Device connected/dis-connected automatically detect
  - IN/OUT token handshake packet automatically
  - Max 256-byte packet length supported
  - Wake-up function supported

CAN Interface (Max one channel) Available on S6E2GM and S6E2GH Devices Only

- Compatible with CAN specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32-message buffer

Multi-function Serial Interface (Max 10 Channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 1 and channels 4 to 7.
- Operation mode is selectable for each channel from the following:
  - UART
  - CSIO (SPI)
  - LIN
  - I^2C
  - I^2S
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch 6 and ch 7 only)
  - Supports high-speed SPI (ch 4 and ch 6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/slave mode supported
  - LIN break field generation (can change to 13- to 16-bit length)

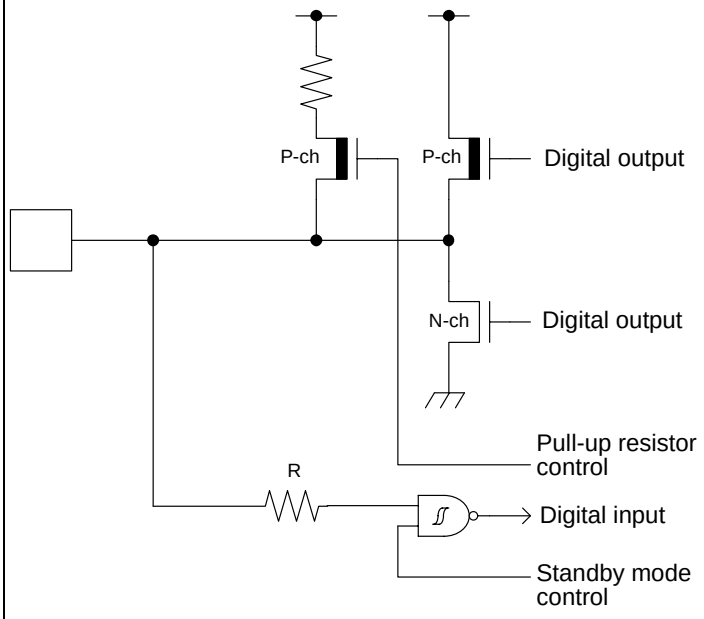
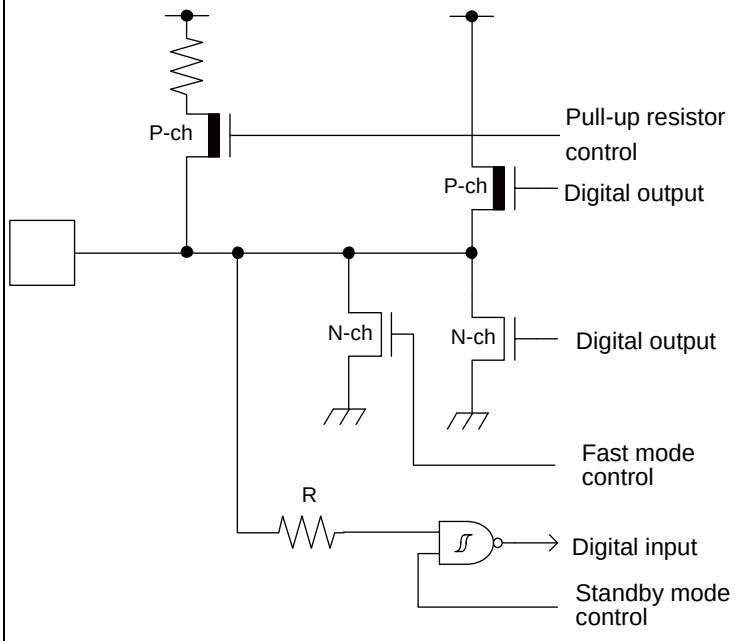
6. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
1	1	VCC	-	-
2	2	PA0 RTO00_1 (PPG00_1) TIOA8_0 INT00_0 MADATA00_0 IC0_CIN_0	E	K
3	3	PA1 RTO01_1 (PPG01_1) TIOA9_0 MADATA01_0 IC0_DATA_0	E	I
4	4	PA2 RTO02_1 (PPG02_1) TIOA10_0 MADATA02_0 IC0_RST_0	E	I
5	5	PA3 RTO03_1 (PPG03_1) TIOA11_0 MADATA03_0 IC0_VPEN_0	E	I
6	6	PA4 RTO04_1 (PPG04_1) TIOA12_0 MADATA04_0 IC0_VCC_0	E	I
7	7	PA5 RTO05_1 (PPG05_1) TIOA13_0 INT01_0 MADATA05_0 IC0_CLK_0	E	K

Type	Circuit	Remarks
L		・ CMOS level output ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -8 mA, I_{OL} = 8 mA ・ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
N		・ CMOS level output ・ CMOS level hysteresis input ・ 5V tolerant ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA (GPIO) ・ I_{OL} = 20mA (Fast mode Plus) ・ Available to control of PZR register (pseudo-open drain control) ・ For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856). ・ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Start Address	End Address	Bus	Peripherals
0x4004_0000	0x4004_FFFF	AHB	USB ch 0
0x4005_0000	0x4005_FFFF		USB ch 1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch 0
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x4006_5FFF		Ethernet-MAC ch 0
0x4006_6000	0x4006_6FFF		Ethernet-MAC setting register
0x4006_7000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x41FF_FFFF		Reserved

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
O	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected						Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7*10	5.5	V	
Power supply voltage (for USB ch 0)		$USBV_{CC}0$	-	3.0	3.6 ($\leqV_{CC}$)	V	*1
				2.7	5.5 ($\leqV_{CC}$)		*2
Power supply voltage (for USB ch 1)		$USBV_{CC}1$	-	3.0	3.6 ($\leqV_{CC}$)	V	*3
				2.7	5.5 ($\leqV_{CC}$)		*4
Power supply voltage (for Ethernet-MAC)		$ETHV_{CC}$	-	3.0	3.6 ($\leqV_{CC}$)	V	*5
				4.5	5.5 ($\leqV_{CC}$)		*5
				2.7	5.5 ($\leqV_{CC}$)		*6
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	$AV_{CC} = V_{CC}$
Analog reference voltage		AVRH	-	*9	AV_{CC}	V	
		AVRL	-	AV_{SS}	AV_{SS}	V	
Smoothing capacitor		C_S	-	1	10	µF	for built-in regulator *7
Operating temperature	Junction temperature	T_J	-	- 40	+ 125	°C	
	Ambient temperature	T_A	-	-40	*8	°C	

1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0)

2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80)

3: When P83/UDP1 and P82/UDM1 pins are used as USB (UDP1, UDM1)

4: When P83/UDP1 and P82/UDM1 pins are used as GPIO (P83, P82)

5: When the pins in Ethernet-MAC Timing, except P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as Ethernet-MAC pin

6: When the pins in Ethernet-MAC Timing, except P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as function pins

7: See "C pin" in 9 Handling Devices for the connection of the smoothing capacitor.

8: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).

The calculation formula of the ambient temperature (T_A) is:

$T_A (Max) = T_J(Max) - Pd(Max) \times \theta_{JA}$

Pd: Power dissipation (W)
θ_{JA}: Package thermal resistance (°C/W)

$Pd (Max) = V_{CC} \times I_{CC} (Max) + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC} - V_{OH}) \times (- I_{OH}))$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

9: The minimum value of analog reference voltage depends on the value of compare clock cycle (Tcck). See 12.5. 12-bit A/D Converter for the details.

10: For the voltage range between V_{CC}(min) and the low voltage detection reset (VDH), the MCU must be clocked from either the High-speed CR or the low-speed CR.

Ethernet-MAC Pins

Pin Name	Ethernet-MAC Function	Except For Ethernet-MAC Function	Power Supply Type
P6E/ADTG_5/SCK4_1/INT29_0/E_PPS	E_PPS *	P6E/ADTG_5/SCK4_1/INT29_0	V_{CC}
PC0/E_RXER	E_RXER	PC0	$ETHV_{CC}$
PC1/TIOB6_0/E_RX03	E_RX03	PC1/TIOB6_0	
PC2/TIOA6_0/E_RX02	E_RX02	PC2/TIOA6_0	
PC3/TIOB7_0/E_RX01	E_RX01	PC3/TIOB7_0	
PC4/TIOA7_0/E_RX00	E_RX00	PC4/TIOA7_0	
PC5/TIOB14_0/E_RXDV	E_RXDV	PC5/TIOB14_0	
PC6/TIOA14_0/E_MDIO	E_MDIO	PC6/TIOA14_0	
PC7/INT13_0/E_MDC/CROUT_1	E_MDC	PC7/INT13_0/CROUT_1	
PC8/E_RXCK_REFCK	E_RXCK_REFCK	PC8	
PC9/TIOB15_0/E_COL	E_COL	PC9/TIOB15_0	
PCA/TIOA15_0/E_CRS	E_CRS	PCA/TIOA15_0	
PCB/INT28_0/E_COUT	E_COUT	PCB/INT28_0	
PCC/E_TCK	E_TCK	PCC	
PCD/SOT4_1/INT14_0/E_TXER	E_TXER	PCD/SOT4_1/INT14_0	
PCE/SIN4_1/INT15_0/E_TX03	E_TX03	PCE/SIN4_1/INT15_0	
PCF/RTS4_1/INT12_0/E_TX02	E_TX02	PCF/RTS4_1/INT12_0	
PD0/INT30_1/E_TX01	E_TX01	PD0/INT30_1	
PD1/INT31_1/E_TX00	E_TX00	PD1/INT31_1	
PD2/CTS4_1/E_TXEN	E_TXEN	PD2/CTS4_1	

*: It is used to confirm the PTP counter cycle in Ethernet-MAC by waveforms.

Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	180 MHz	82	140	mA	*3 When all peripheral clocks are on
				*6	160 MHz	74	132	mA	
					144 MHz	68	126	mA	
					120 MHz	58	116	mA	
					100 MHz	49	107	mA	
					80 MHz	40	98	mA	
					60 MHz	31	89	mA	
					40 MHz	22	80	mA	
					20 MHz	13	71	mA	
					8 MHz	7.5	65	mA	
					4 MHz	5.6	63	mA	
				*5	180 MHz	48	106	mA	*3 When all peripheral clocks are off
				*6	160 MHz	44	102	mA	
					144 MHz	41	99	mA	
					120 MHz	35	93	mA	
					100 MHz	30	88	mA	
					80 MHz	25	83	mA	
					60 MHz	20	78	mA	
					40 MHz	14	72	mA	
					20 MHz	8.7	66	mA	
					8 MHz	5.6	63	mA	
					4 MHz	4.5	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

7: With data access to a MainFlash memory.

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-5 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation*5 (PLL)	180 MHz	58	116	mA	*3 When all peripheral clocks are on
				160 MHz	52	110	mA	
				144 MHz	48	106	mA	
				120 MHz	40	98	mA	
				100 MHz	35	93	mA	
				80 MHz	28	86	mA	
				60 MHz	22	80	mA	
				40 MHz	16	74	mA	
				20 MHz	9.7	67	mA	
				8 MHz	6.2	64	mA	
				4 MHz	5.0	63	mA	
				180 MHz	30	88	mA	*3 When all peripheral clocks are off
				160 MHz	27	85	mA	
				144 MHz	25	83	mA	
				120 MHz	21	79	mA	
				100 MHz	18	76	mA	
				80 MHz	15	73	mA	
				60 MHz	12	70	mA	
				40 MHz	9.3	67	mA	
				20 MHz	6.2	64	mA	
				8 MHz	4.5	62	mA	
				4 MHz	4.0	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-8 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.41	1.9	mA	*3, *4 T_A = +25°C
					-	18	mA	*3, *4 T_A = +85°C
					-	26	mA	*3, *4 T_A = +105°C
	I_{CCT}		Timer mode*5 (main oscillation)	4 MHz	1.4	2.9	mA	*3, *4 T_A = +25°C
					-	19	mA	*3, *4 T_A = +85°C
					-	27	mA	*3, *4 T_A = +105°C
			Timer mode (built-in High-speed CR)	4 MHz	0.71	2.2	mA	*3, *4 T_A = +25°C
					-	19	mA	*3, *4 T_A = +85°C
					-	27	mA	*3, *4 T_A = +105°C
			Timer mode*6 (sub oscillation)	32 kHz	0.41	1.9	mA	*3, *4 T_A = +25°C
					-	18	mA	*3, *4 T_A = +85°C
					-	27	mA	*3, *4 T_A = +105°C
			Timer mode (built-in low-speed CR)	100 kHz	0.42	1.9	mA	*3, *4 T_A = +25°C
					-	18	mA	*3, *4 T_A = +85°C
					-	27	mA	*3, *4 T_A = +105°C
	I_{CCR}		RTC mode*6 (sub oscillation)	32 kHz	0.42	1.9	mA	*3, *4 T_A = +25°C
					-	18	mA	*3, *4 T_A = +85°C
					-	27	mA	*3, *4 T_A = +105°C

1: V_{CC} = 3.3 V

2: V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: When LVD is off

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
			$ETHV_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5$ V, I_{OL} = 2 mA					
		8 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 4 mA					
			$ETHV_{CC} \geq 4.5$ V, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5$ V, I_{OL} = 4 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5$ V, I_{OL} = 18.5 mA	V_{SS}	-	0.4	V	*1
			$USBV_{CC} < 4.5$ V, I_{OL} = 10.5 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5$ V, I_{OL} = 3 mA					
			$V_{CC} \leq 4.5$ V, I_{OL} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, USBVCC0, USBVCC1, ETHVCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

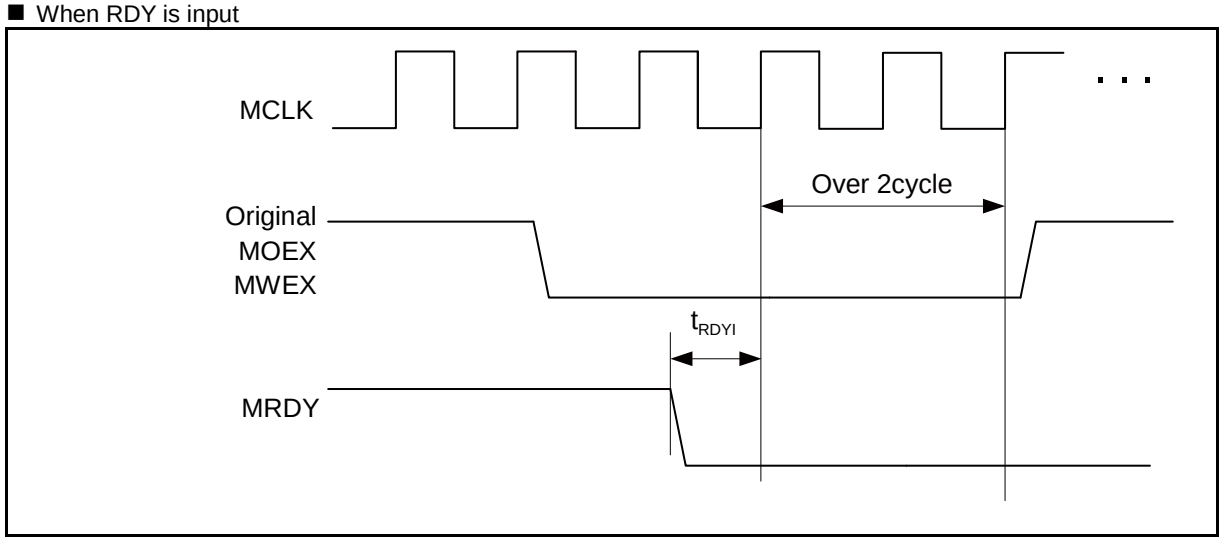
1: $USBV_{CC}0$ and $USBV_{CC}1$ are described as $USBV_{CC}$.

External Ready Input Timing

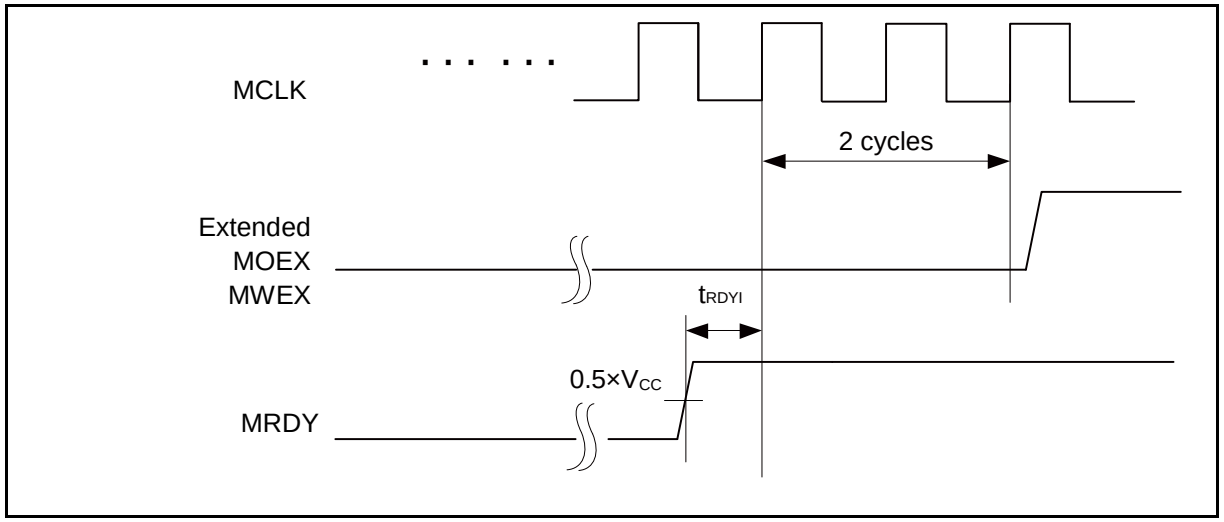
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

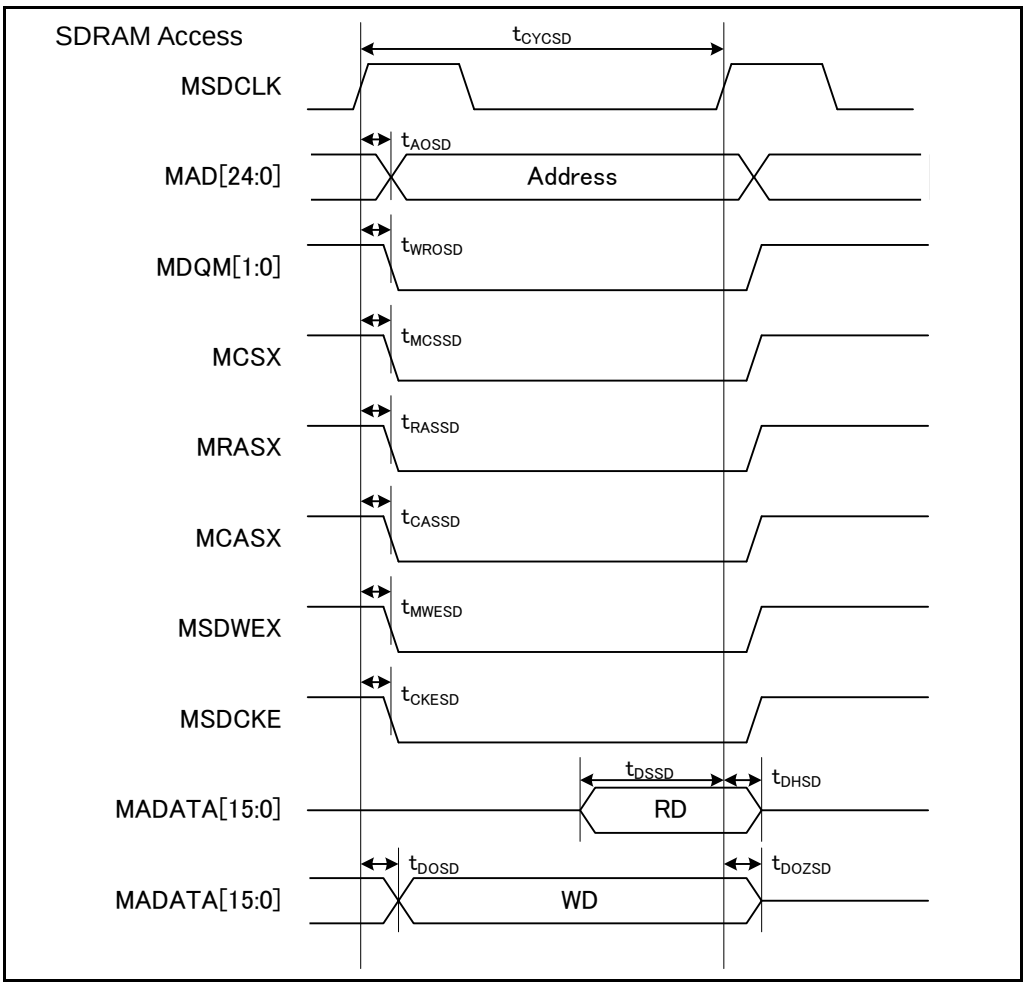
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

■ When RDY is input



■ When RDY is released




SDRAM Access
tCYCSD
MSDCLK
tAOSD
MAD[24:0]
Address
tWROSD
MDQM[1:0]
tMCSSD
MCSX
tRASSD
MRASX
tCASSD
MCASX
tMWESD
MSDWEX
tCKESD
MSDCKE
tDSSD
tDHSD
MADATA[15:0]
RD
tDOSD
tDOZSD
MADATA[15:0]
WD

12.4.12 CSIO (SPI) Timing

Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*

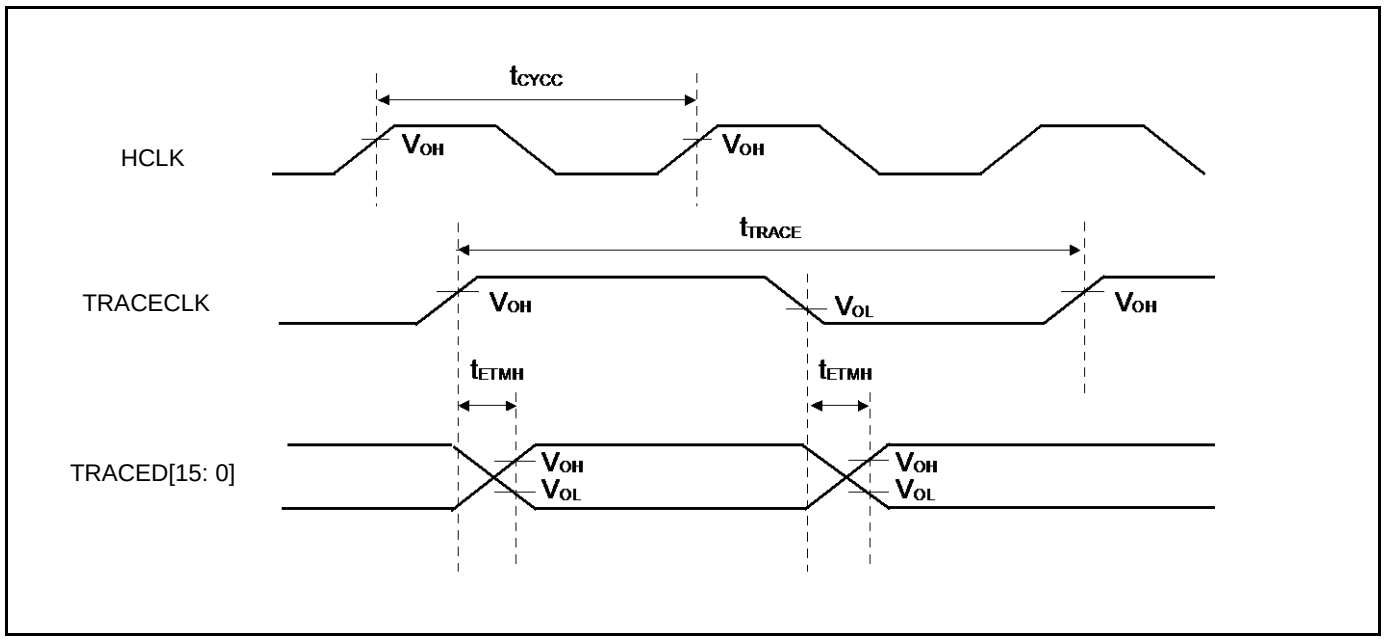
Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*


tCYCC
HCLK
VOH
VOH
tTRACE
TRACECLK
VOH
VOL
VOH
tETMH
tETMH
TRACED[15: 0]
VOH
VOL
VOH
VOL

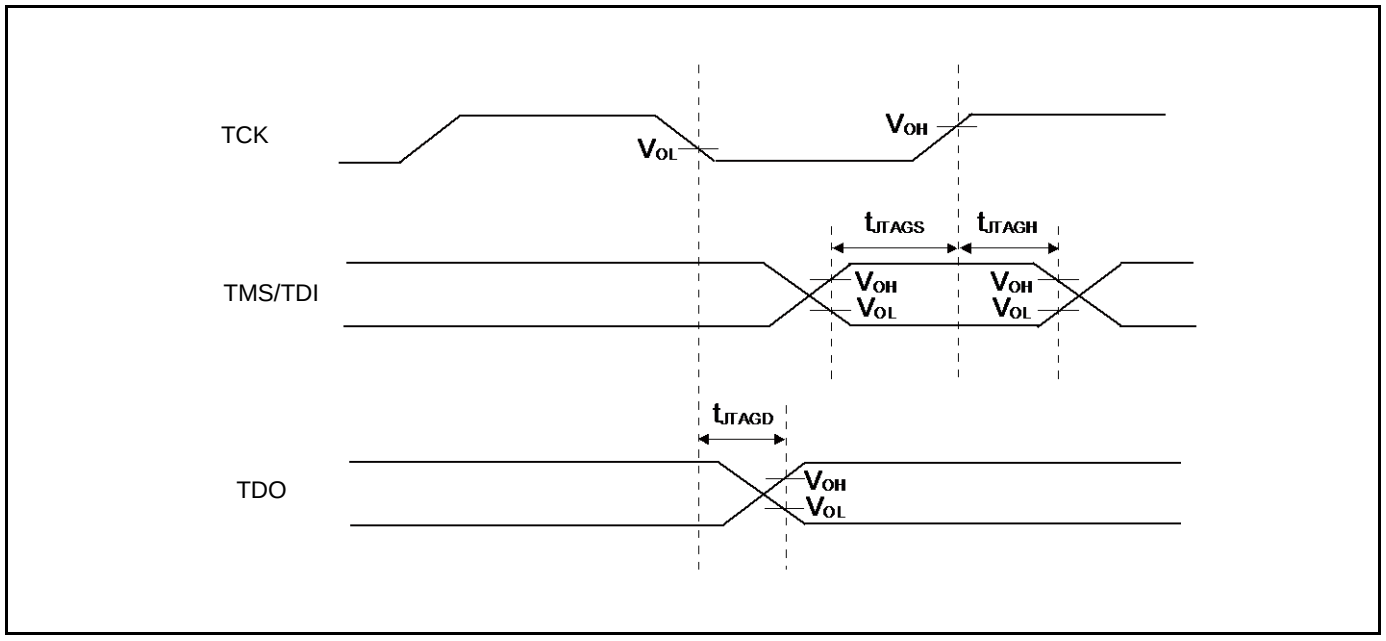
12.4.18 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

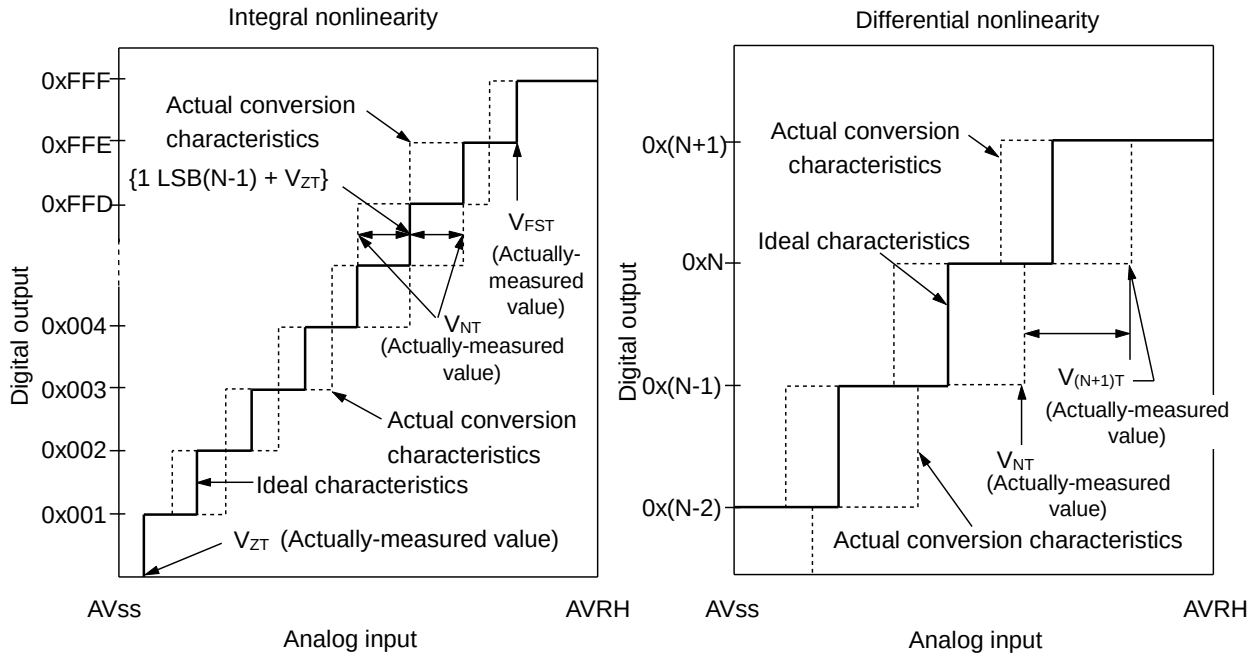
Note:

- *When the external load capacitance C_L = 30 pF.*



Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

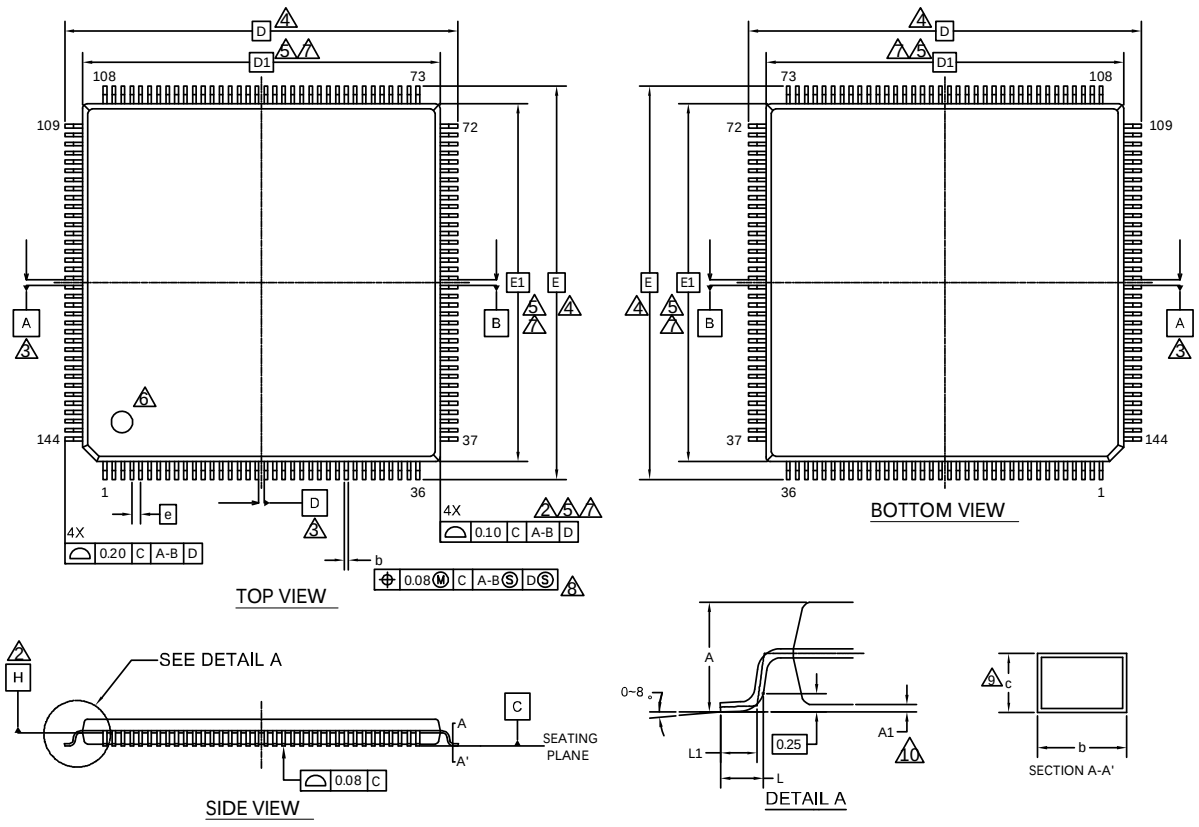
$$\text{Differential nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D		22.00 BSC	
D1		20.00 BSC	
e		0.50 BSC	
E		22.00 BSC	
E1		20.00 BSC	
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 REV*A

002-13015 *A

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