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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gk8h0agv2000a

6. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
1	1	VCC	-	-
2	2	PA0 RTO00_1 (PPG00_1) TIOA8_0 INT00_0 MADATA00_0 IC0_CIN_0	E	K
3	3	PA1 RTO01_1 (PPG01_1) TIOA9_0 MADATA01_0 IC0_DATA_0	E	I
4	4	PA2 RTO02_1 (PPG02_1) TIOA10_0 MADATA02_0 IC0_RST_0	E	I
5	5	PA3 RTO03_1 (PPG03_1) TIOA11_0 MADATA03_0 IC0_VPEN_0	E	I
6	6	PA4 RTO04_1 (PPG04_1) TIOA12_0 MADATA04_0 IC0_VCC_0	E	I
7	7	PA5 RTO05_1 (PPG05_1) TIOA13_0 INT01_0 MADATA05_0 IC0_CLK_0	E	K

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
66	56	P4E	L	Q
		SCK9_0 (SCL9_0)		
		INT05_0		
		WKUP2		
		MCSX1_0		
67	57	P70	L	I
		ADTG_7		
		SOT9_0 (SDA9_0)		
		MCSX0_0		
68	58	P71	I	K
		ADTG_8		
		SIN9_0		
		INT04_1		
		MRDY_0		
69	59	P72	E	I
		TIOB0_0		
		INT06_2		
		MAD00_0		
70	60	P73	E	K
		SIN8_0		
		TIOB1_0		
		INT20_0		
		MAD01_0		
71	61	P74	E	I
		SOT8_0 (SDA8_0)		
		TIOB2_0		
		MAD02_0		
72	62	P75	E	I
		SCK8_0 (SCL8_0)		
		TIOB3_0		
		MAD03_0		
73	63	P76	E	K
		SIN6_0		
		TIOB4_0		
		INT21_0		
		MAD04_0		
74	64	P77	L	I
		SOT6_0 (SDA6_0)		
		TIOB5_0		
		MAD05_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
112	-	PB6	F	N
		AN22		
		SOT8_1 (SDA8_1)		
		TIOA12_1		
		BIN1_2		
		TRACED14		
113	-	PB7	F	N
		AN23		
		SCK8_1 (SCL8_1)		
		TIOB12_1		
		ZIN1_2		
		TRACED15		
114	90	P1C	F	N
		AN12		
		SCK0_1 (SCL0_1)		
		TIOA5_2		
		TRACECLK		
115	91	P1D	F	L
		AN13		
		SOT0_1 (SDA0_1)		
		TIOB5_2		
		MAD09_0		
116	92	P1E	F	M
		AN14		
		SIN0_1		
		TIOA8_1		
		INT26_1		
		MAD10_0		
117	93	P1F	F	M
		AN15		
		RTS5_0		
		TIOB8_1		
		INT27_1		
		MAD11_0		
118	94	P2A	F	M
		AN24		
		CTS5_0		
		INT08_2		
		MAD12_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
141	-	P92	E	K
		SOT5_1 (SDA5_1)		
		RTO12_1 (PPG12_1)		
		TIOB2_1		
		INT14_1		
		IC0_VPEN_1		
142	-	P93	E	K
		SCK5_1 (SCL5_1)		
		RTO13_1 (PPG13_1)		
		TIOB3_1		
		INT15_1		
		IC0_RST_1		
143	-	P94	E	I
		CTS5_1		
		RTO14_1 (PPG14_1)		
		TIOB4_1		
		IC0_DATA_1		
144	-	P95	E	I
		RTS5_1		
		RTO15_1 (PPG15_1)		
		TIOB5_1		
		IC0_CIN_1		
145	115	PC0	K	V
		E_RXER		
146	116	PC1	K	V
		TIOB6_0		
		E_RX03		
147	117	PC2	K	V
		TIOA6_0		
		E_RX02		
148	118	PC3	K	V
		TIOB7_0		
		E_RX01		
149	119	PC4	K	V
		TIOA7_0		
		E_RX00		
150	120	PC5	K	V
		TIOB14_0		
		E_RXDV		

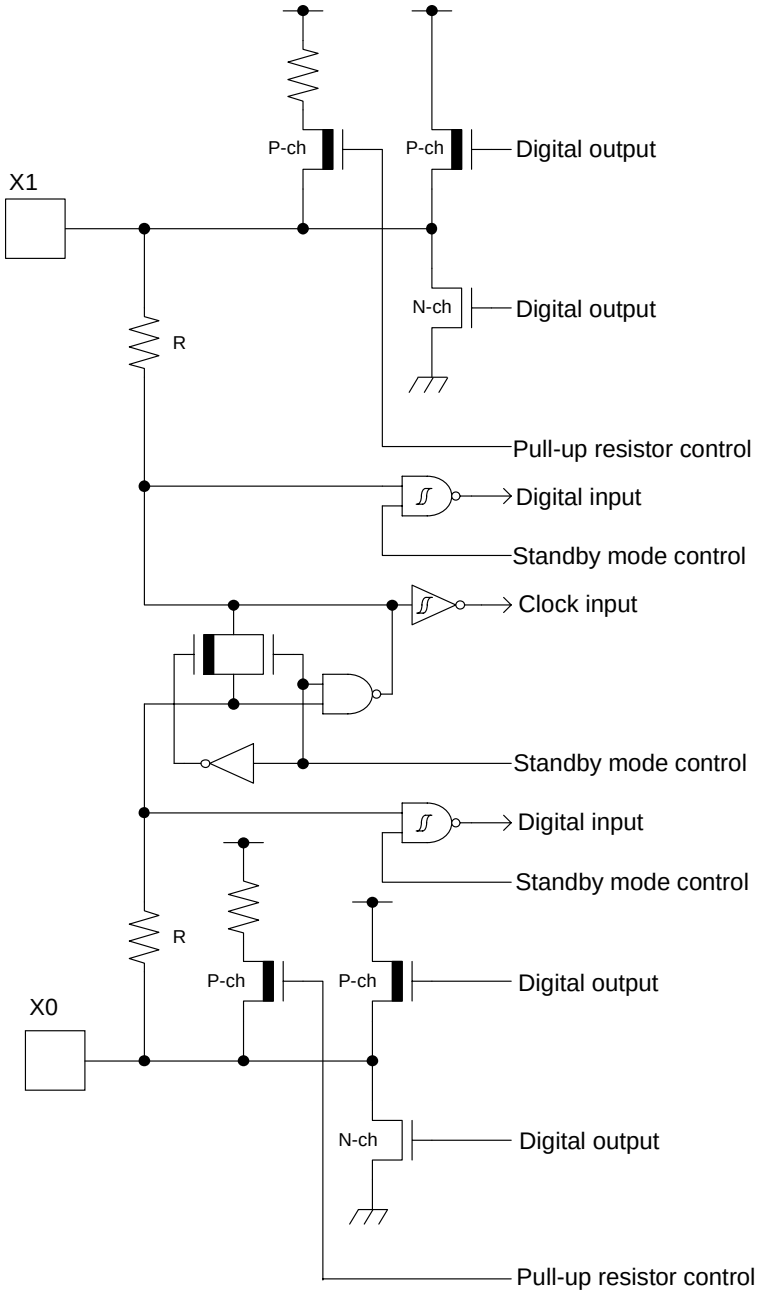
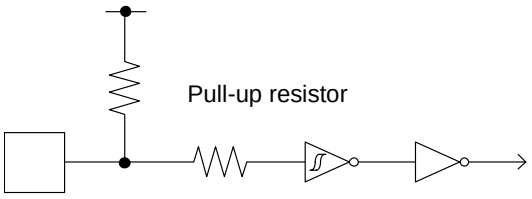
Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External bus	MAD00_0	External bus interface address bus	69	59
	MAD01_0		70	60
	MAD02_0		71	61
	MAD03_0		72	62
	MAD04_0		73	63
	MAD05_0		74	64
	MAD06_0		75	65
	MAD07_0		76	66
	MAD08_0		77	67
	MAD09_0		115	91
	MAD10_0		116	92
	MAD11_0		117	93
	MAD12_0		118	94
	MAD13_0		119	95
	MAD14_0		120	96
	MAD15_0		121	97
	MAD16_0		122	98
	MAD17_0		123	99
	MAD18_0		124	100
	MAD19_0		40	35
	MAD20_0		39	34
	MAD21_0		38	33
	MAD22_0		37	32
	MAD23_0		36	31
	MAD24_0		35	30
	MCSX0_0	External bus interface chip select output pin	67	57
	MCSX1_0		66	56
	MCSX2_0		51	43
	MCSX3_0		50	42
	MCSX4_0		49	41
	MCSX5_0		48	40
	MCSX6_0		47	39
	MCSX7_0		46	38
	MCSX8_0		63	53

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P00	General-purpose I/O port 0	134	110
	P01		135	111
	P02		136	112
	P03		137	113
	P04		138	114
	P08		21	18
	P09		22	19
	P0A		23	20
	P10	General-purpose I/O port 1	94	78
	P11		95	79
	P12		96	80
	P13		97	81
	P14		98	82
	P15		99	83
	P16		100	84
	P17		101	85
	P18		106	86
	P19		107	87
	P1A		108	88
	P1B		109	89
	P1C		114	90
	P1D		115	91
	P1E		116	92
	P1F		117	93
	P20	General-purpose I/O port 2	128	104
	P21		127	103
	P22		126	102
	P23		125	101
	P24		124	100
	P25		123	99
	P26		122	98
	P27		121	97
	P28		120	96
	P29		119	95
	P2A		118	94

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	121	97
	SIN5_1		140	-
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I²C (operation mode 4).	120	96
	SOT5_1 (SDA5_1)		141	-
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I²C (operation mode 4).	119	95
	SCK5_1 (SCL5_1)		142	-
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	118	94
	CTS5_1		143	-
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	117	93
	RTS5_1		144	-
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	73	63
	SIN6_1		100	84
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I²C (operation mode 4).	74	64
	SOT6_1 (SDA6_1)		101	85
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I²C (operation mode 4).	75	65
	SCK6_1 (SCL6_1)		102	-
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	76	66
	SCS60_1		103	-
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	77	67
	SCS61_1		104	-
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	78	-
	SCS62_1		105	-
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	79	-
	SCS63_1		110	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
SD I/F	S_CLK_0	SD memory card interface SD memory card clock output pin	28	23
	S_CMD_0	SD memory card interface SD memory card command output	31	26
	S_DATA1_0	SD memory card interface SD memory card data bus	26	21
	S_DATA0_0		27	22
	S_DATA3_0		32	27
	S_DATA2_0		33	28
	S_CD_0	SD memory card interface SD memory card detection pin	35	30
	S_WP_0	SD memory card interface SD memory card write protection	34	29
Ethernet	E_COL	Collision detection	154	124
	E_COUT	Clock output for Ethernet PHY	158	128
	E_CRS	Carrier detection	155	125
	E_MDC	Management clock	152	122
	E_MDIO	Management data I/O	151	121
	E_PPS	PTP counter monitor	166	136
	E_RX00	Received data0	149	119
	E_RX01	Received data1	148	118
	E_RX02	Received data2	147	117
	E_RX03	Received data3	146	116
	E_RXCK_REFCK	Received clock input/ Reference clock	153	123
	E_RXDV	Received data enable	150	120
	E_RXER	Received data error detection	145	115
	E_TCK	Transition clock input	159	129
	E_TX00	Transition data0	164	134
	E_TX01	Transition data1	163	133
	E_TX02	Transition data2	162	132
	E_TX03	Transition data3	161	131
	E_TXEN	Transition data enable	165	135
	E_TXER	Transition data error detection	160	130

7. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main Oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 1 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA
B		・ CMOS level hysteresis input ・ Pull-up resistor: approximately 50 kΩ

8. Handling Precautions

Every semiconductor device has a characteristic, inherent rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins that connect semiconductor devices to power supply and I/O functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present for extended periods of time, can damage the device; therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power-supply pin or ground pin.

9. Handling Devices

Power-Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. All of these pins should be connected externally to the power supply or ground lines, however, in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Be sure to connect the current-supply source with the power pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS near this device.

A malfunction may occur when the power-supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane, as this is expected to produce stable operation.

Evaluate the oscillation introduced by the use of the crystal oscillator by your mount board.

Sub Crystal Oscillator

The sub-oscillator circuit for devices in this family is low gain to keep current consumption low. To stabilize the oscillation, Cypress recommends a crystal oscillator that meets the following conditions:

- Surface mount type
  Size: More than 3.2 mm × 1.5 mm
  Load capacitance: approximately 6 pF to 7 pF
- Lead type
  Load capacitance: approximately 6 pF to 7 pF

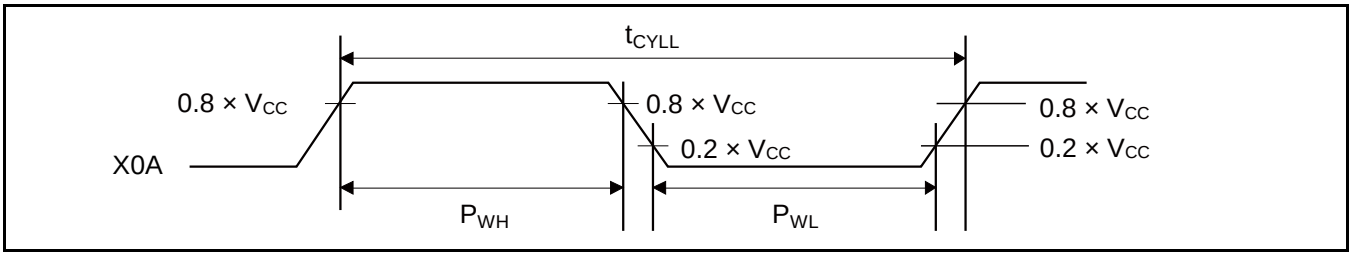
Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected					Maintain previous state	Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

12.4.2 Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see Sub crystal oscillator in 9. Handling Devices.



12.4.3 Built-In CR Oscillation Characteristics

Built-In High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = - 20°C to + 105°C	3.92	4	4.08	MHz	When trimmed *1
		T_J = - 40°C to + 125°C	3.88	4	4.12		
		T_J = - 40°C to + 125°C	2.9	4	5		When not trimmed
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

Built-In Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.8 Power-On Reset Timing

(V_{SS} = 0V)

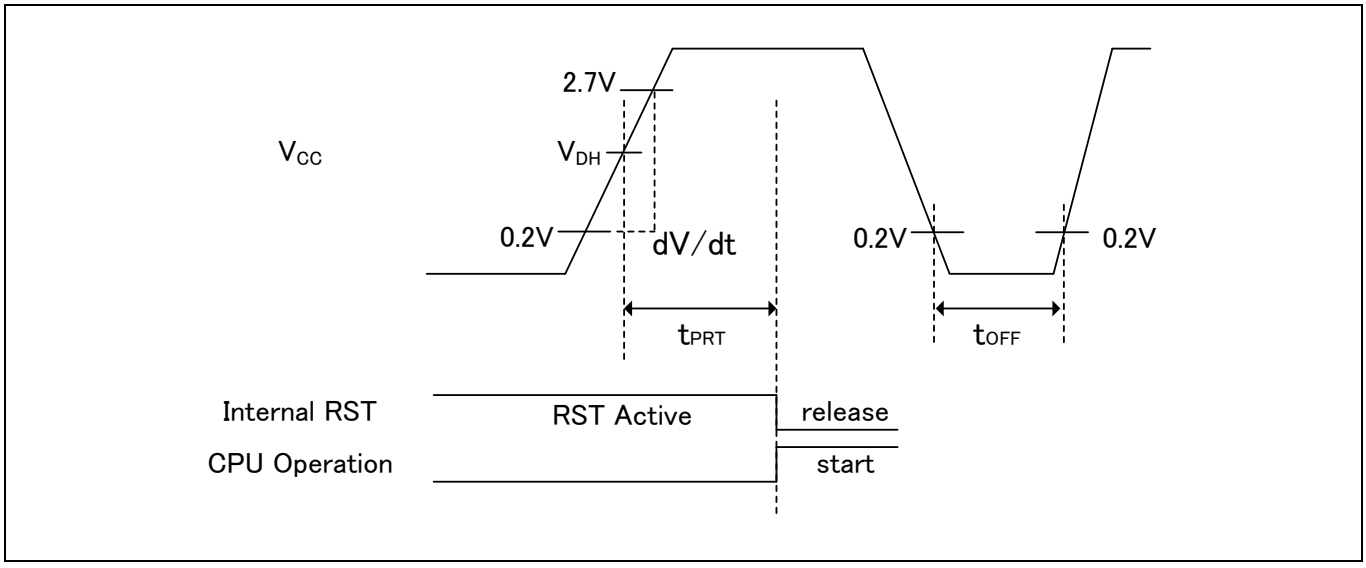
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	1	-	-	ms	*1
Power ramp rate	dV/dt		V_{CC}: 0.2V to 2.70V	0.6	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.33	-	0.60	ms	

1: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>1ms).

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 7.*



Glossary

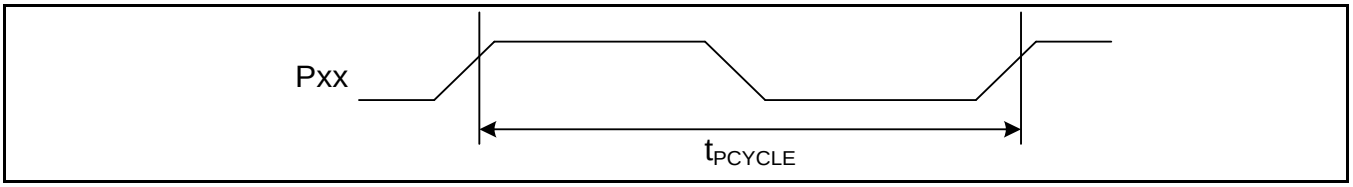
- V_{DH}: detection voltage of Low Voltage detection reset. See “12.7. Low-Voltage Detection Characteristics”.

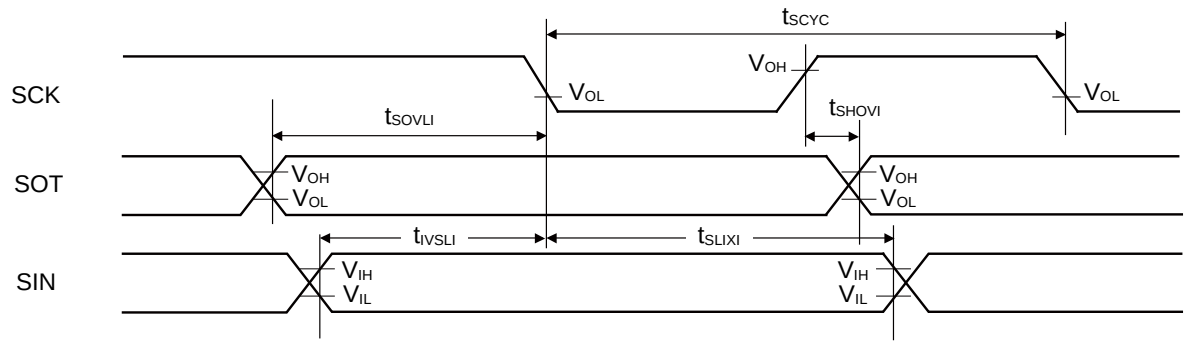
12.4.9 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

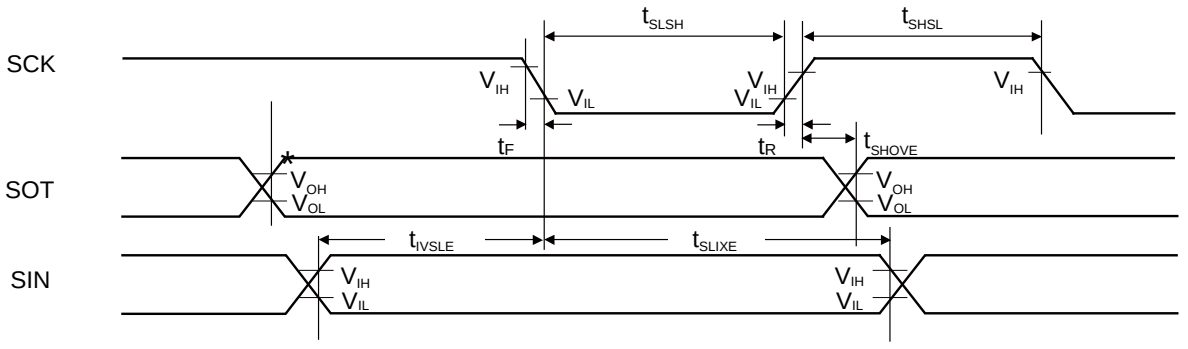
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{PCYCLE}	Pxx*	V_{CC} ≥ 4.5V	-	50	MHz	
			V_{CC} < 4.5V	-	32	MHz	

*: GPIO is a target.



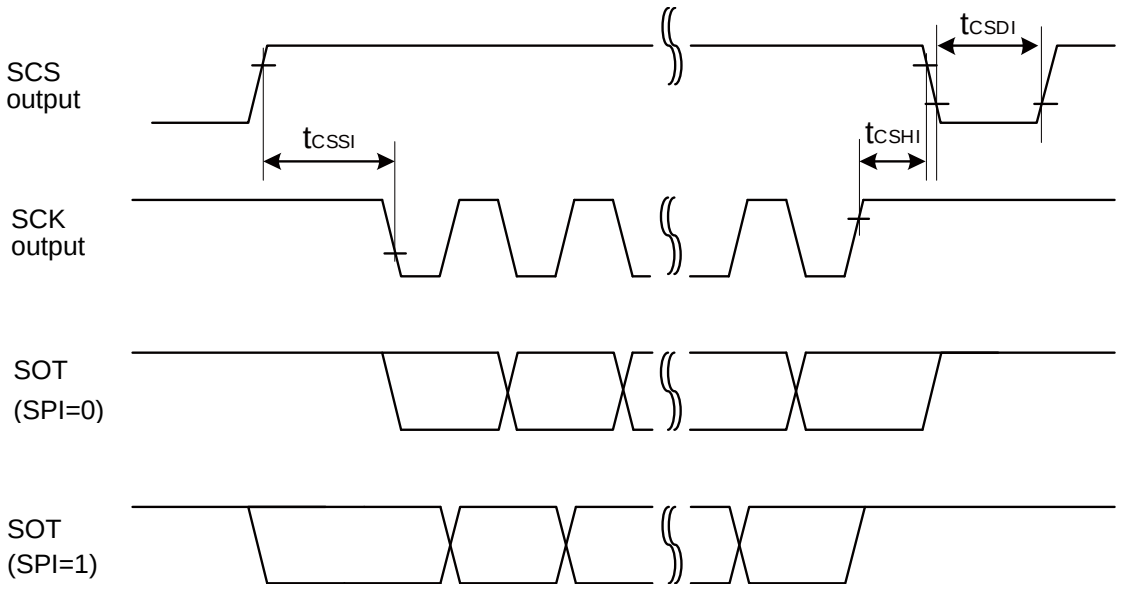


MS bit = 0

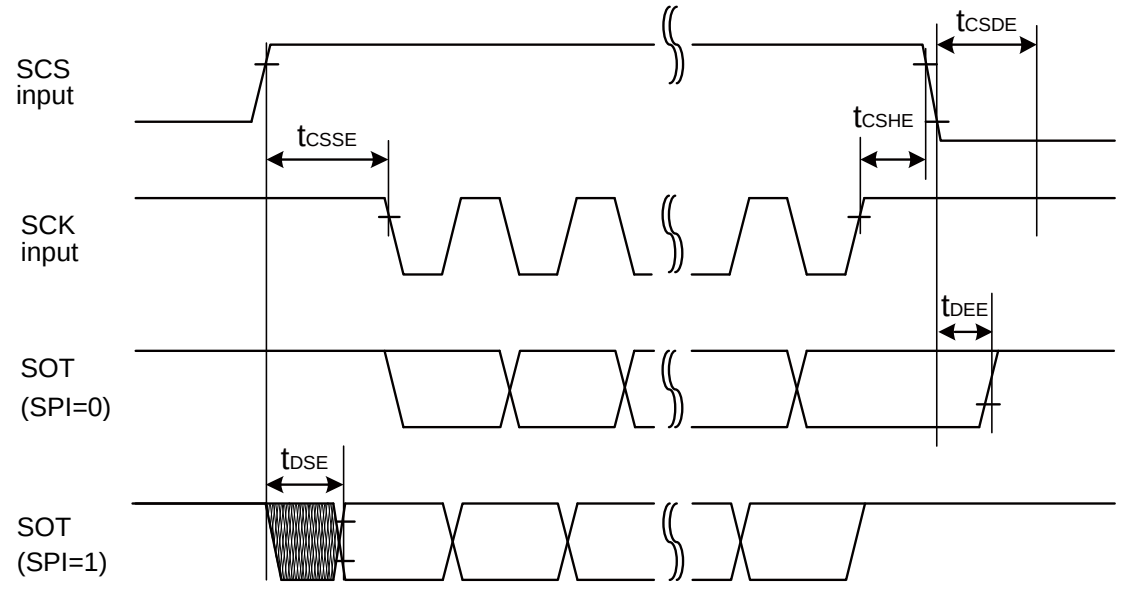


MS bit = 1

*: Changes when writing to TDR register



MS bit = 0



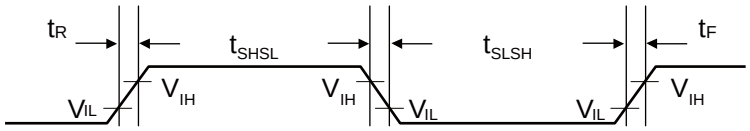
MS bit = 1

External Clock (EXT = 1): When in Asynchronous Mode Only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK fall time	t_F		-	5	ns	
SCK rise time	t_R		-	5	ns	

SCK



12.4.16 SD Card Interface Timing

Default-Speed Mode

■ Clock CLK (All values are referenced to V_{IH} and V_{IL} transition points)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1card)	0	25	MHz
Clock frequency Identification mode	f_{OD}	S_CLK		0/100	400	kHz
Clock low time	t_{WL}	S_CLK		10	-	ns
Clock high time	t_{WH}	S_CLK		10	-	ns
Clock rise time	t_{TLH}	S_CLK		-	10	ns
Clock fall time	t_{THL}	S_CLK		-	10	ns

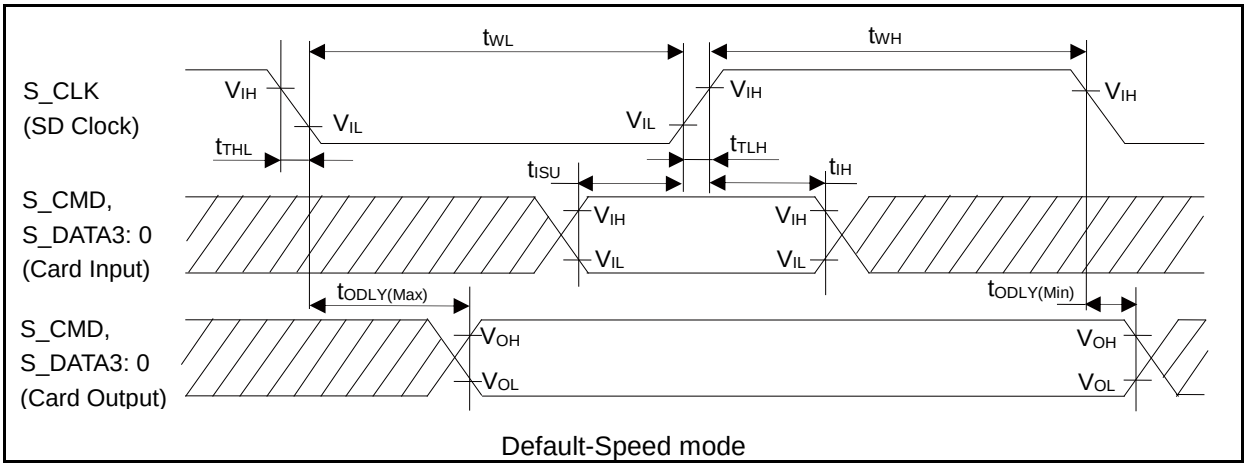
*: 0 Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

■ Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1card)	5	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		5	-	ns

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 40 pF (1card)	0	14	ns
Output Delay time during Identification mode	t_{ODLY}	S_CMD, S_DATA3: 0		0	50	ns



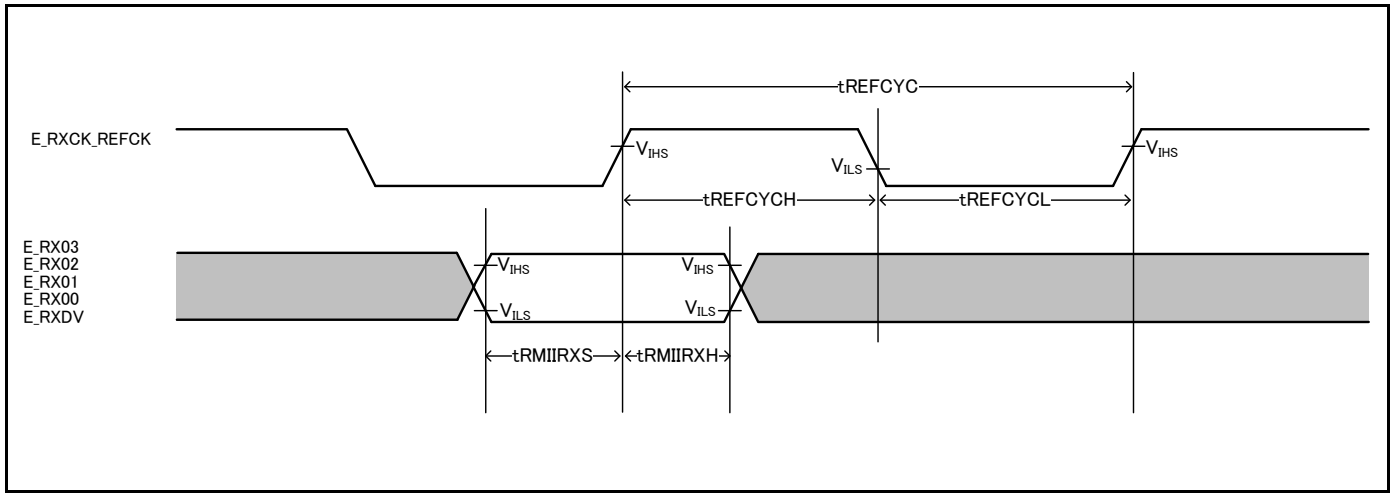
Default-Speed mode

RMII Receiving (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time*	t_{REFCYC}	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	$t_{REFCYCH}$	E_RXCK_REFCK	$t_{REFCYCH}/t_{REFCYC}$	35	65	%
Reference clock Low-pulse-width duty cycle	$t_{REFCYCL}$	E_RXCK_REFCK	$t_{REFCYCL}/t_{REFCYC}$	35	65	%
Received data → REFCK ↑ Setup time	$t_{RMIIRXS}$	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	4	-	ns
REFCK ↑ → Received data Hold time	$t_{RMIIRXH}$	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	2	-	ns

*: The reference clock is fixed to 50 MHz in the RMII specifications.
The clock accuracy should meet the PHY-device specifications.



13. Ordering Information

Part Number	Flash	RAM	CAN	Ethernet	SD Card	Crypto	Package
S6E2GM6H0AGV2000A	512 KB	128 KB	✓	✓	✓		Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2GM8H0AGV2000A	1 MB	192 KB	✓	✓	✓		
S6E2GM6HHAGV2000A	512 KB	128 KB	✓	✓	✓	✓	
S6E2GM8HHAGV2000A	1 MB	192 KB	✓	✓	✓	✓	
S6E2GM6J0AGV2000A	512 KB	128 KB	✓	✓	✓		Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2GM8J0AGV2000A	1 MB	192 KB	✓	✓	✓		
S6E2GM6JHAGV2000A	512 KB	128 KB	✓	✓	✓	✓	
S6E2GM8JHAGV2000A	1 MB	192 KB	✓	✓	✓	✓	
S6E2GK6H0AGV2000A	512 KB	128 KB		✓	✓		Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2GK8H0AGV2000A	1 MB	192 KB		✓	✓		
S6E2GK6HHAGV2000A	512 KB	128 KB		✓	✓	✓	
S6E2GK8HHAGV2000A	1 MB	192 KB		✓	✓	✓	
S6E2GK6J0AGV2000A	512 KB	128 KB		✓	✓		Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2GK8J0AGV2000A	1 MB	192 KB		✓	✓		
S6E2GK6JHAGV2000A	512 KB	128 KB		✓	✓	✓	
S6E2GK8JHAGV2000A	1 MB	192 KB		✓	✓	✓	
S6E2GH6H0AGV2000A	512 KB	128 KB	✓		✓		Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2GH8H0AGV2000A	1 MB	192 KB	✓		✓		
S6E2GH6J0AGV2000A	512 KB	128 KB	✓		✓		Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2GH8J0AGV2000A	1 MB	192 KB	✓		✓		
S6E2G36H0AGV2000A	512 KB	128 KB					Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2G38H0AGV2000A	1 MB	192 KB					
S6E2G36J0AGV2000A	512 KB	128 KB					Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2G38J0AGV2000A	1 MB	192 KB					
S6E2G26H0AGV2000A	512 KB	128 KB		✓			Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2G28H0AGV2000A	1 MB	192 KB		✓			
S6E2G26HHAGV2000A	512 KB	128 KB		✓		✓	
S6E2G28HHAGV2000A	1 MB	192 KB		✓		✓	
S6E2G26J0AGV2000A	512 KB	128 KB		✓			Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2G28J0AGV2000A	1 MB	192 KB		✓			
S6E2G26JHAGV2000A	512 KB	128 KB		✓		✓	
S6E2G28JHAGV2000A	1 MB	192 KB		✓		✓	