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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gk8hhagv2000a

- LIN break delimiter generation (can change to 1- to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

- I²C
  - Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported
- I²S
  - Using CSIO (SPI) (ch 1 only) and I²S clock generator
  - Supports two transfer protocol: I²S and MSB-justified
  - Master mode only

DMA Controller (Eight Channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System Data Transfer Controller; 256 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 32 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Built-in three units
  - Conversion time: 0.5 µs at 5 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max 16 channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer
- Event counter mode (External clock mode)

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 121 high-speed general-purpose I/O ports in 144-pin package
- Some pins 5 V tolerant I/O.
  See 6. Pin Descriptions and 7. I/O Circuit Type for the corresponding pins.

Multi-function Timer (Max two units)

The multi-function timer is composed of the following blocks:
Minimum resolution: 5.56 ns

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 6 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC)

The real-time clock can count year, month, day, hour, minute, second, or day of the week from 00 to 99.

- Interrupt function with specifying date and time (year/month/day/hour/minute) is available. This function is also available by specifying only year, month, day, hour, or minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detector reset
  - Clock supervisor reset

Clock Supervisor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include two-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, the low-voltage detector function generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Crypto Assist Function

These features are enabled for the crypto assist function.

The dedicated middleware is necessary for this calculator operation.

- PKA (Public Key Accelerator)
  - PKA（Public Key Accelerator）is modular exponentiation calculation accelerator used of RSA Public Key crypto and so on.
  - Available bit length: Up to 2048-bit
- AES calculator
  - AES (Advanced Encryption Standard) calculator is a AES common key crypto accelerator which is compliant with FIPS (Federal Information Processing Standard Publication)197.
  - Available key length: 128/192/256-bit
  - CBC mode and ECB mode support
- External Bus Data Scramble
  - It enables to scramble input/output data of External Bus Interface.

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

- Four power supplies
  - Wide range voltage: VCC = 2.7 V to 5.5 V
  - Power supply for USB ch 0 I/O: USBVCC0
= 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for USB ch 1 I/O: USBVCC1
= 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for Ethernet-MAC I/O: ETHVCC
= 3.0 V to 5.5 V (when Ethernet is used.)

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
166	136	P6E ADTG_5 SCK4_1 (SCL4_1) INT29_0 E_PPS	E	W
167	-	P65 INT28_1	E	K
168	-	P64 CTS4_0 INT29_1	I	K
169	137	P63 ADTG_3 RTS4_0 INT30_0 MOEX_0	L	K
170	138	P62 SCK4_0 (SCL4_0) TIOB7_2 MWEX_0	L	I
171	139	P61 UHCONX0 SOT4_0 (SDA4_0) TIOA7_2 MALE_0 RTCCO_0 SUBOUT_0	L	I
172	140	P60 SIN4_0 INT31_0 WKUP3	I	Q
173	141	USBVCC0	-	-
174	142	P80 UDM0	H	R
175	143	P81 UDP0	H	R
176	144	VSS	-	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 7	SIN7_0	Multi-function serial interface ch 7 input pin	13	10
	SIN7_1		46	38
	SOT7_0 (SDA7_0)	Multi-function serial interface ch 7 output pin This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I²C (operation mode 4).	14	11
	SOT7_1 (SDA7_1)		47	39
	SCK7_0 (SCL7_0)	Multi-function serial interface ch 7 clock I/O pin This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I²C (operation mode 4).	15	12
	SCK7_1 (SCL7_1)		48	40
	SCS70_0	Multi-function serial interface ch 7 chip select 0 input/output pin	16	13
	SCS70_1		49	41
	SCS71_0	Multi-function serial interface ch 7 chip select 1 input/output pin	17	14
	SCS71_1		50	42
	SCS72_0	Multi-function serial interface ch 7 chip select 2 input/output pin	10	-
	SCS72_1		51	43
	SCS73_0	Multi-function serial interface ch 7 chip select 3 input/output pin	11	-
	SCS73_1		58	-
Multi-Function Serial 8	SIN8_0	Multi-function serial interface ch 8 input pin	70	60
	SIN8_1		111	-
	SOT8_0 (SDA8_0)	Multi-function serial interface ch 8 output pin This pin operates as SOT8 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA8 when it is used in an I²C (operation mode 4).	71	61
	SOT8_1 (SDA8_1)		112	-
	SCK8_0 (SCL8_0)	Multi-function serial interface ch 8 clock I/O pin This pin operates as SCK8 when it is used in a CSIO (operation mode 2) and as SCL8 when it is used in an I²C (operation mode 4).	72	62
	SCK8_1 (SCL8_1)		113	-
Multi-Function Serial 9	SIN9_0	Multi-function serial interface ch 9 input pin	68	58
	SIN9_1		97	81
	SOT9_0 (SDA9_0)	Multi-function serial interface ch 9 output pin This pin operates as SOT9 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA9 when it is used in an I²C (operation mode 4).	67	57
	SOT9_1 (SDA9_1)		98	82
	SCK9_0 (SCL9_0)	Multi-function serial interface ch 9 clock I/O pin This pin operates as SCK9 when it is used in a CSIO (operation mode 2) and as SCL9 when it is used in an I²C (operation mode 4).	66	56
	SCK9_1 (SCL9_1)		99	83

List of Pin Behavior by Mode State

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Main crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enabled	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops*[1], it will be Hi-Z/ Internal input fixed at 0					
C	INITX input pin	Pull-up/ input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ input enabled	GPIO selected	Hi-Z/ input enabled	GPIO selected

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θja (°C/W)	Maximum Permissible Power (mW)	
			T_A = +85 °C	T_A = +105 °C
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645

WARNING:

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
  Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
- *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
  Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Current Explanation Diagram

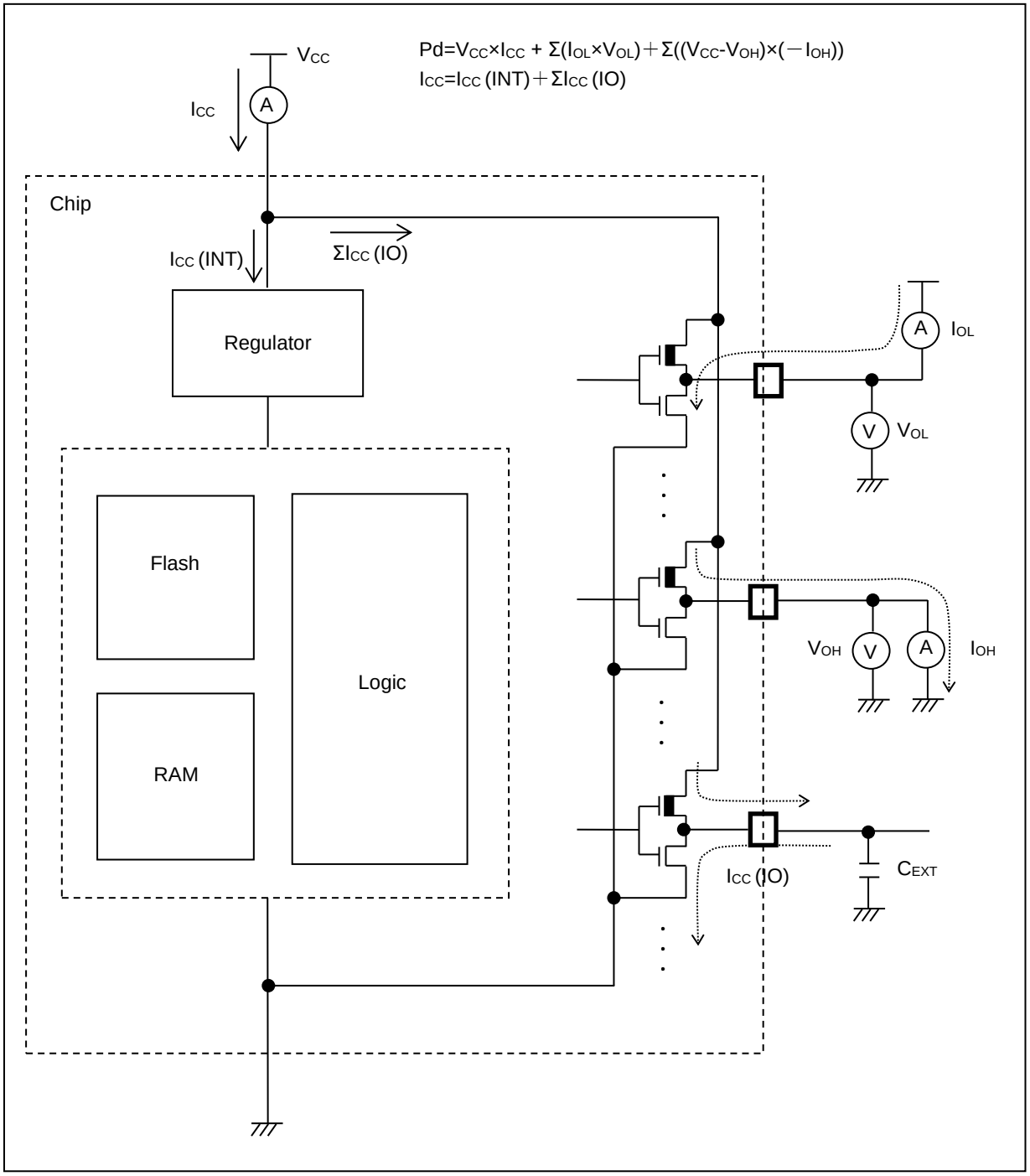


Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7 (PLL)	*5	72 MHz	54	112	mA	*3 When all peripheral clocks are on
					60 MHz	47	105	mA	
					48 MHz	39	97	mA	
					36 MHz	31	89	mA	
					24 MHz	23	81	mA	
					12 MHz	14	72	mA	
					8 MHz	11	69	mA	
					4 MHz	7.2	65	mA	
				*5	72 MHz	37	95	mA	*3 When all peripheral clocks are off
					60 MHz	33	91	mA	
					48 MHz	28	86	mA	
					36 MHz	23	81	mA	
					24 MHz	17	75	mA	
					12 MHz	11	69	mA	
					8 MHz	8.3	66	mA	
					4 MHz	5.9	63	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

6: With data access to a MainFlash memory.

7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-6 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation*5 (PLL)	72 MHz	32	90	mA	*3 When all peripheral clocks are on
				60 MHz	27	85	mA	
				48 MHz	23	81	mA	
				36 MHz	18	76	mA	
				24 MHz	13	71	mA	
				12 MHz	8.5	66	mA	
				8 MHz	6.9	64	mA	
				4 MHz	5.3	63	mA	
				72 MHz	15	73	mA	*3 When all peripheral clocks are off
				60 MHz	13	71	mA	
				48 MHz	11	69	mA	
				36 MHz	9.3	67	mA	
				24 MHz	7.3	65	mA	
				12 MHz	5.4	63	mA	
				8 MHz	4.7	62	mA	
				4 MHz	4.1	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

12.4 AC Characteristics

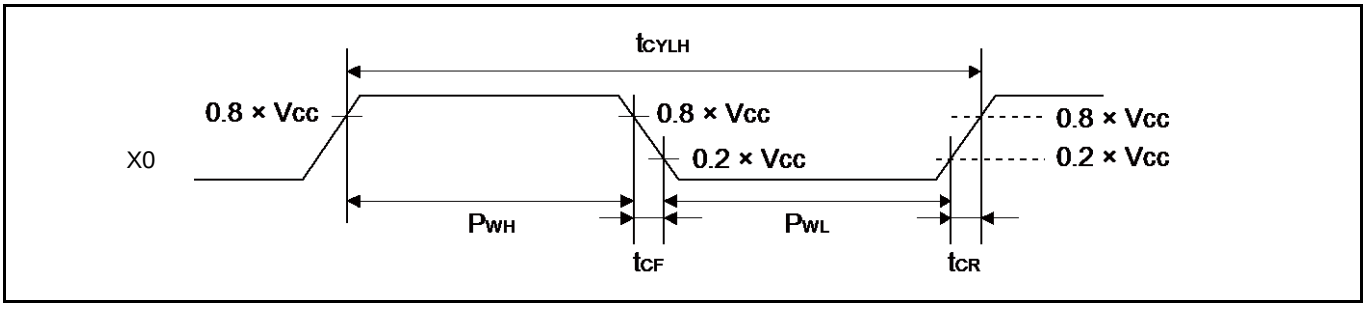
12.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥4.5 V	4	48	MHz	When crystal oscillator is connected
			V_{CC} < 4.5 V	4	20		
			V_{CC} ≥4.5 V	4	48	MHz	When using external clock
			V_{CC} < 4.5 V	4	20		
Input clock cycle	t_{CYLH}		V_{CC} ≥4.5 V	20.83	250	ns	When using external clock
			V_{CC} < 4.5 V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock *1 frequency	f_{CC}	-	-	-	180	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	90	MHz	APB0bus clock *2
	f_{CP1}	-	-	-	180	MHz	APB1bus clock *2
	f_{CP2}	-	-	-	90	MHz	APB2bus clock *2
Internal operating clock *1 cycle time	t_{CYCC}	-	-	5.56	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	11.1	-	ns	APB0bus clock *2
	t_{CYCP1}	-	-	5.56	-	ns	APB1bus clock *2
	t_{CYCP2}	-	-	11.1	-	ns	APB2bus clock *2

1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

2: For more about each APB bus to which each peripheral is connected, see 1. S6E2G Series Block Diagram in this data sheet.

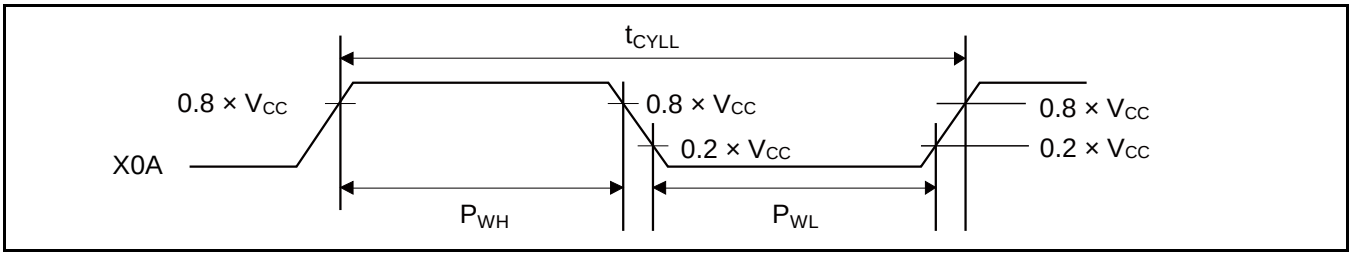


12.4.2 Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see Sub crystal oscillator in 9. Handling Devices.



12.4.3 Built-In CR Oscillation Characteristics

Built-In High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = - 20°C to + 105°C	3.92	4	4.08	MHz	When trimmed *1
		T_J = - 40°C to + 125°C	3.88	4	4.12		
		T_J = - 40°C to + 125°C	2.9	4	5		When not trimmed
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

Built-In Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	180	MHz	

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

12.4.5 Operating Conditions of USB/Ethernet PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB/Ethernet
USB/Ethernet clock frequency *2	f_{CLKPLL}	-	-	50	MHz	After the M frequency division

1: Time from when the PLL starts operating until the oscillation stabilizes

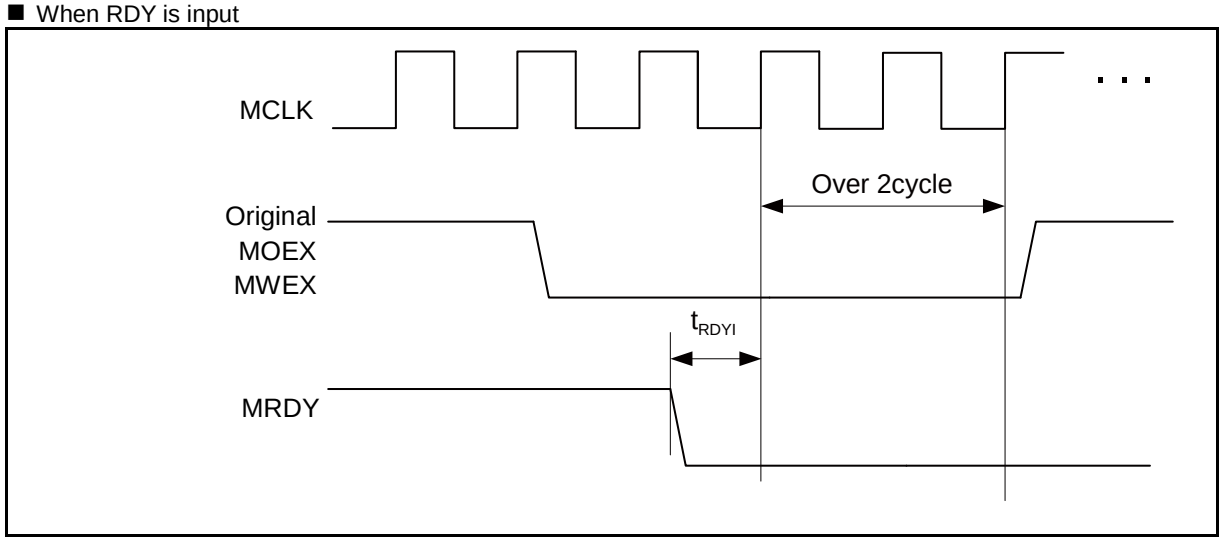
2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

External Ready Input Timing

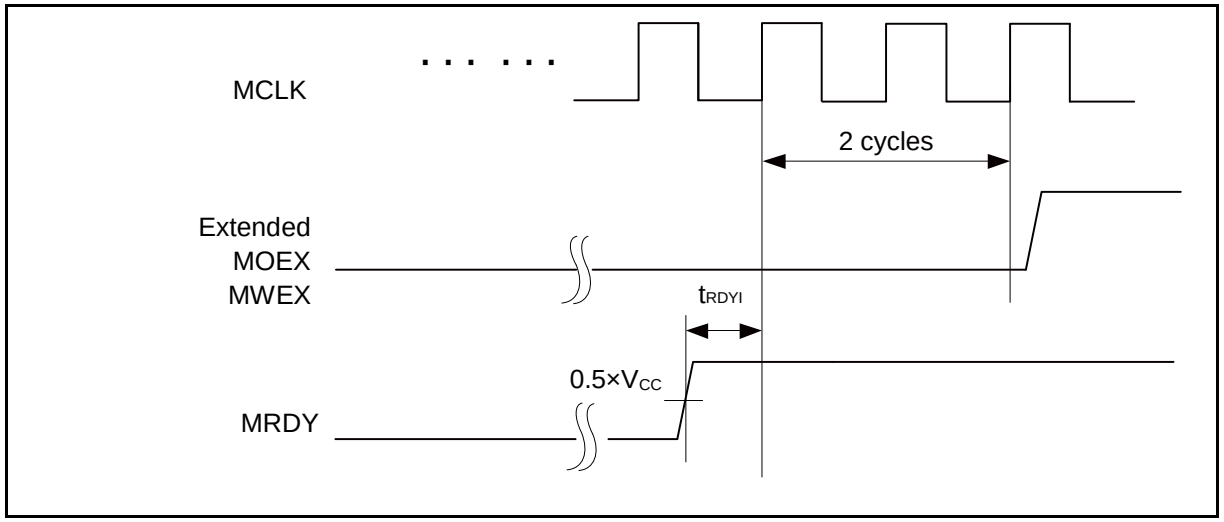
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

■ When RDY is input



■ When RDY is released



When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

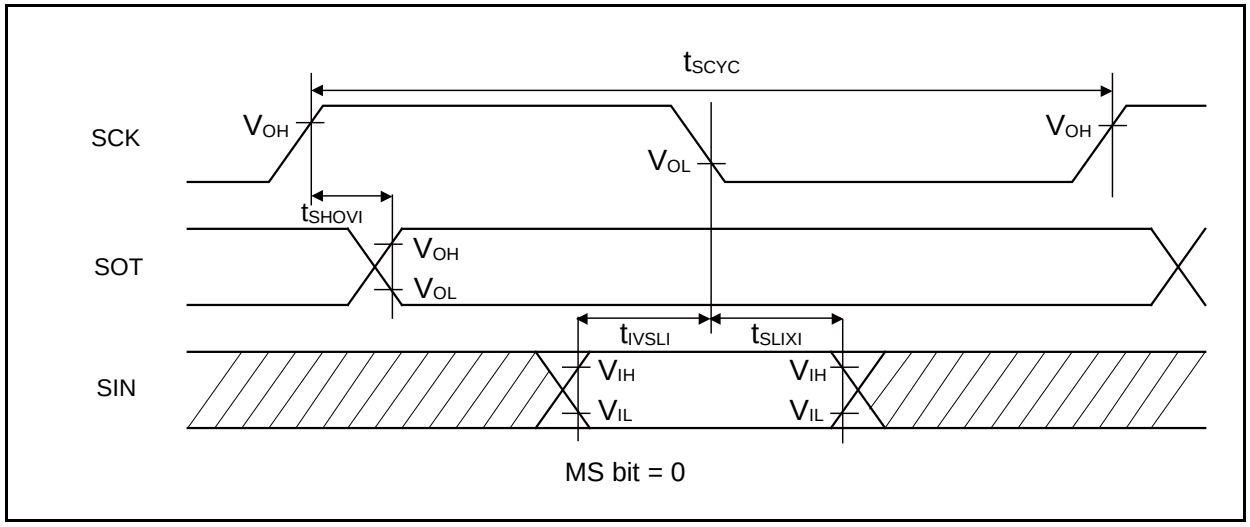
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

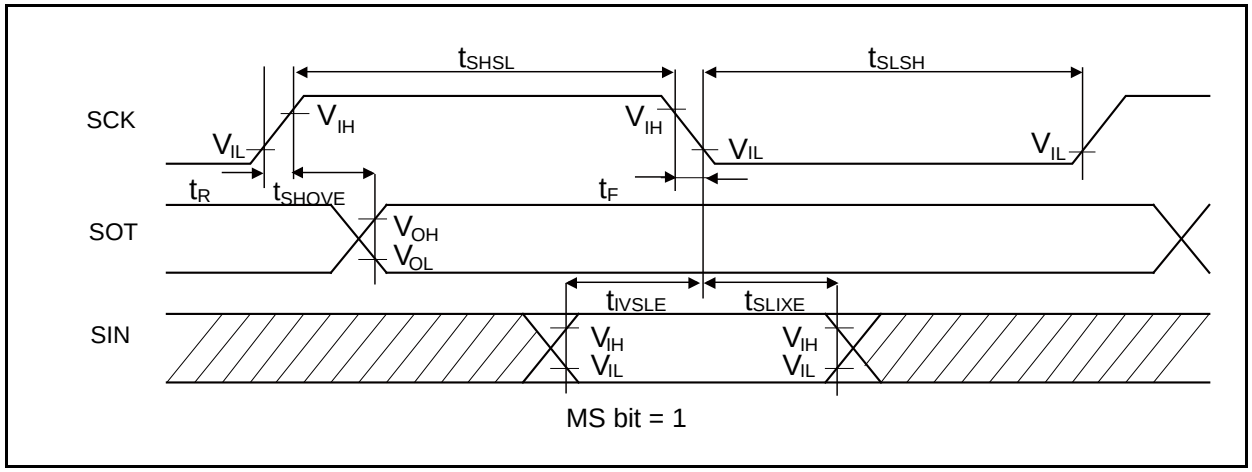
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

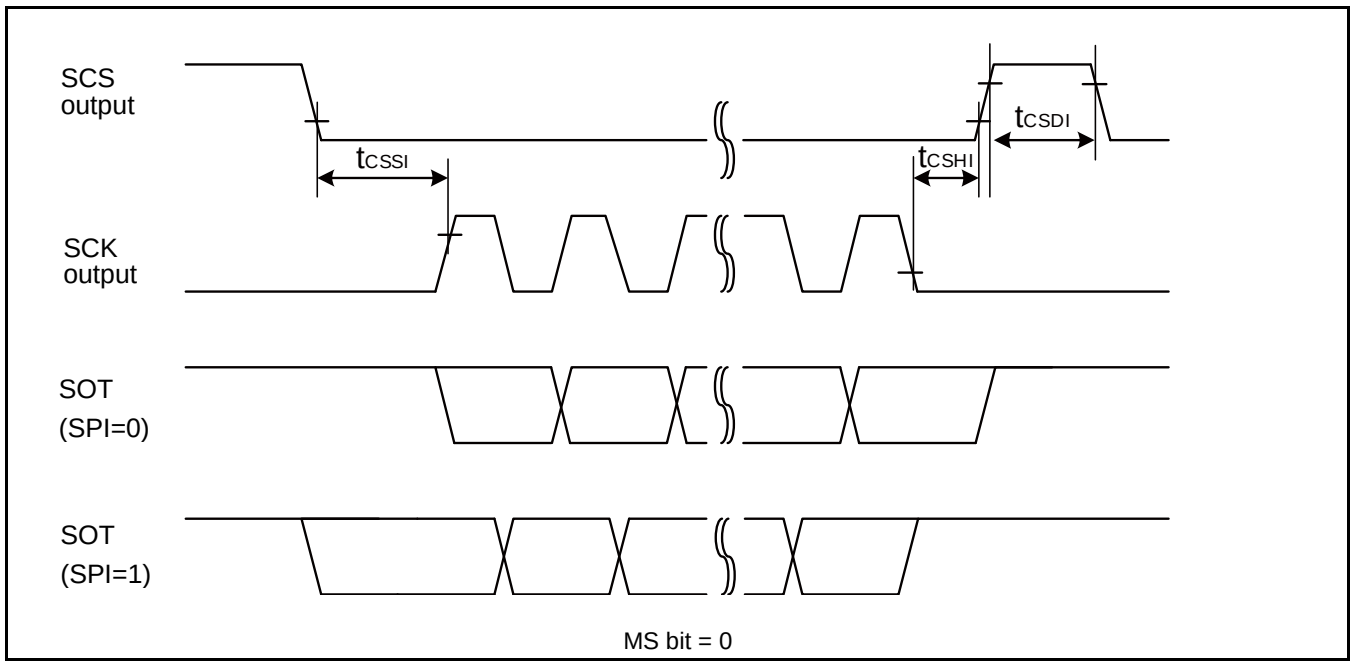
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



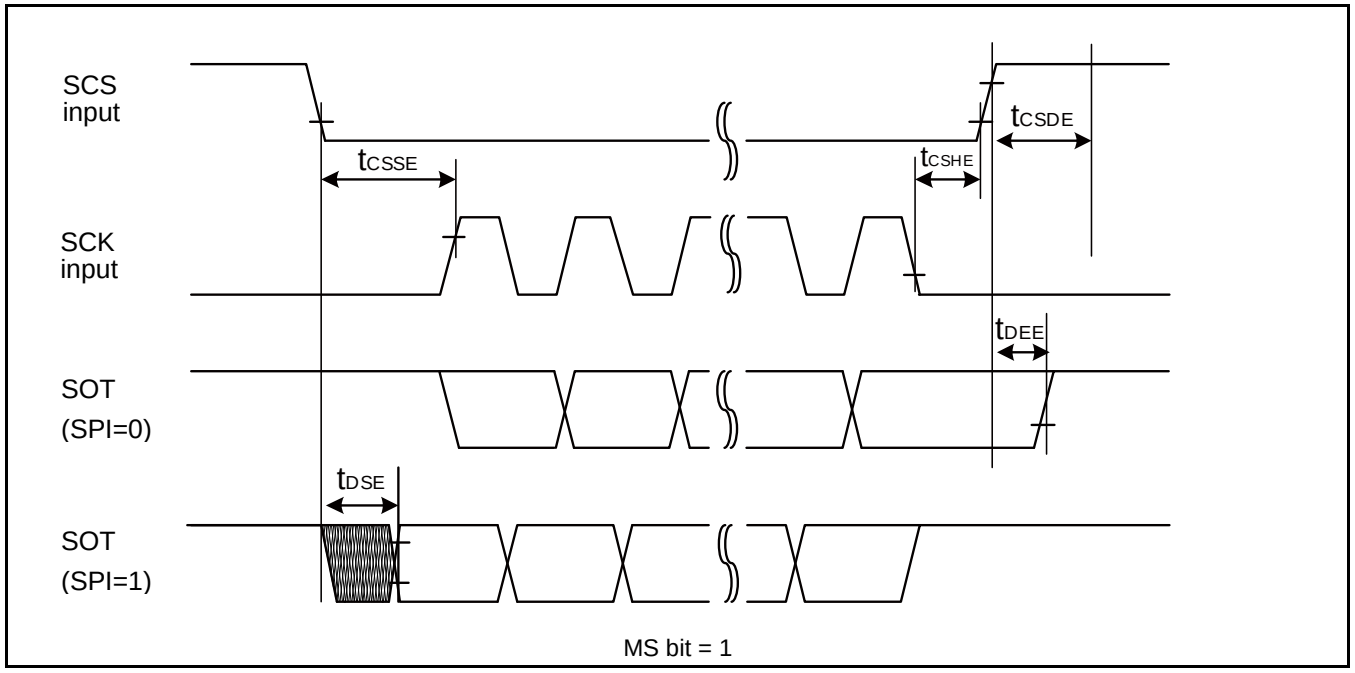
MS bit = 0



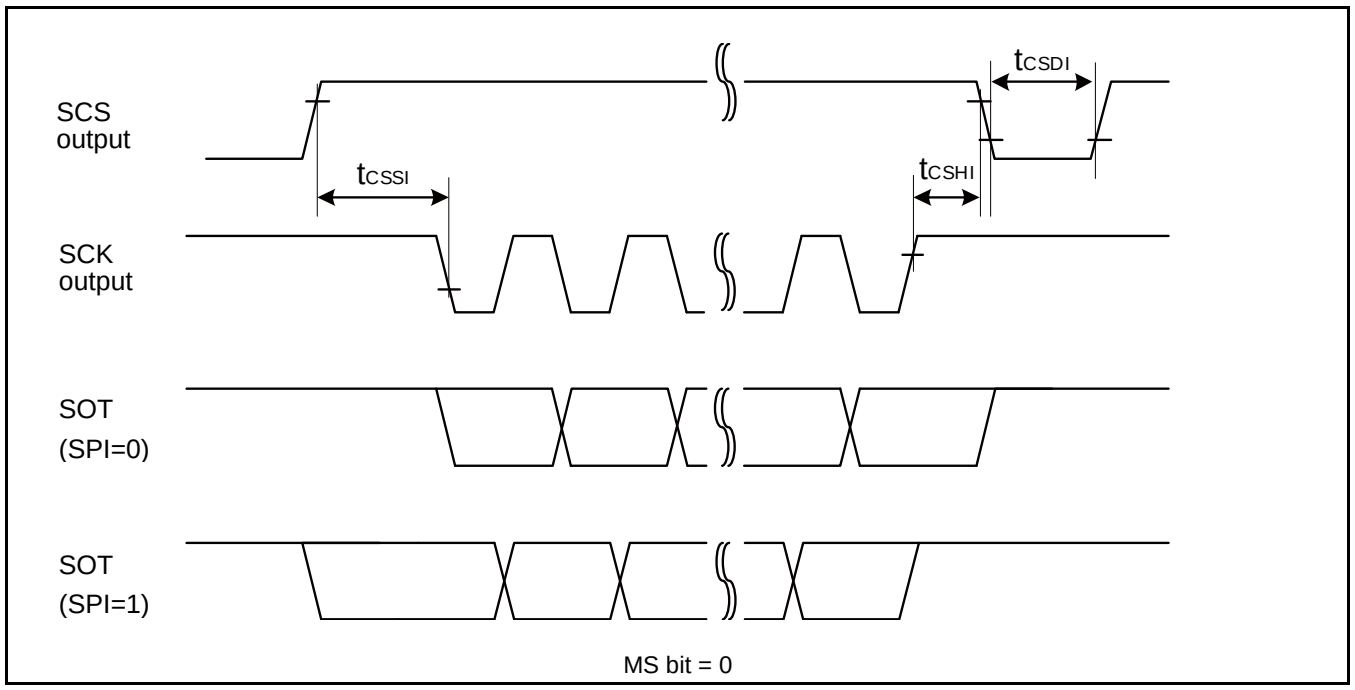
MS bit = 1



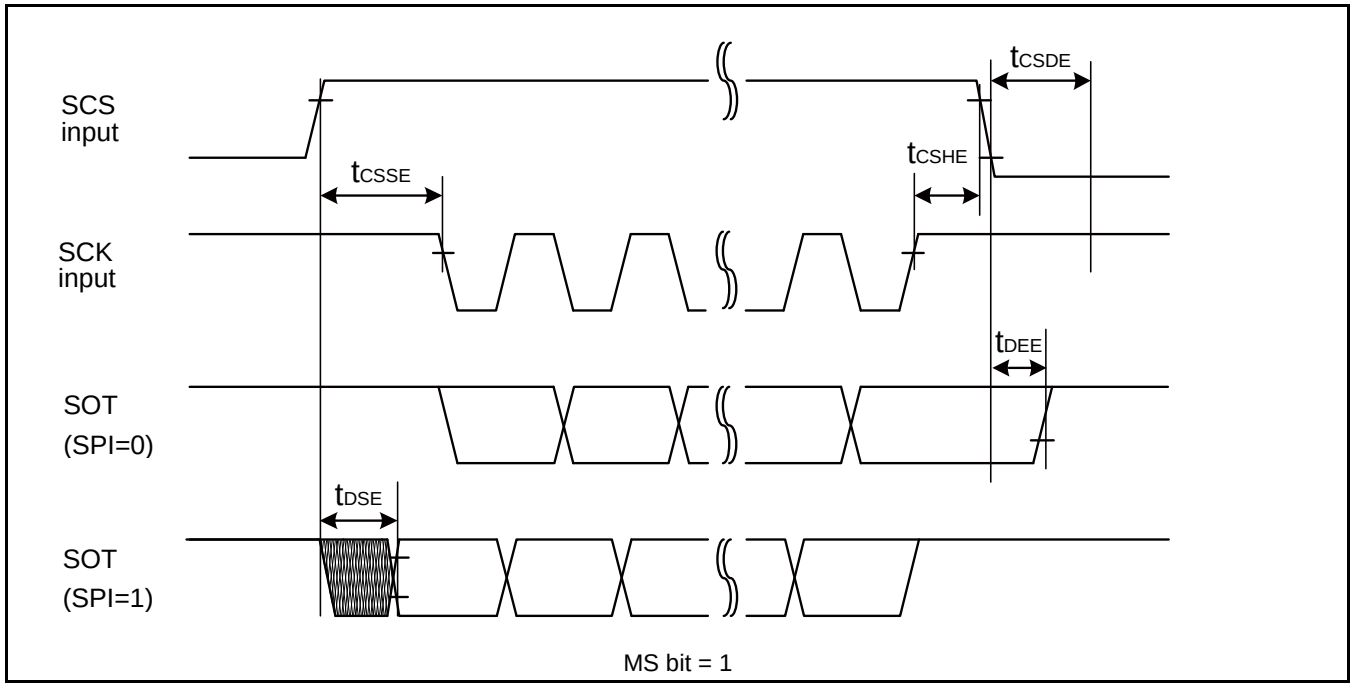
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

12.4.19 Ethernet-MAC Timing

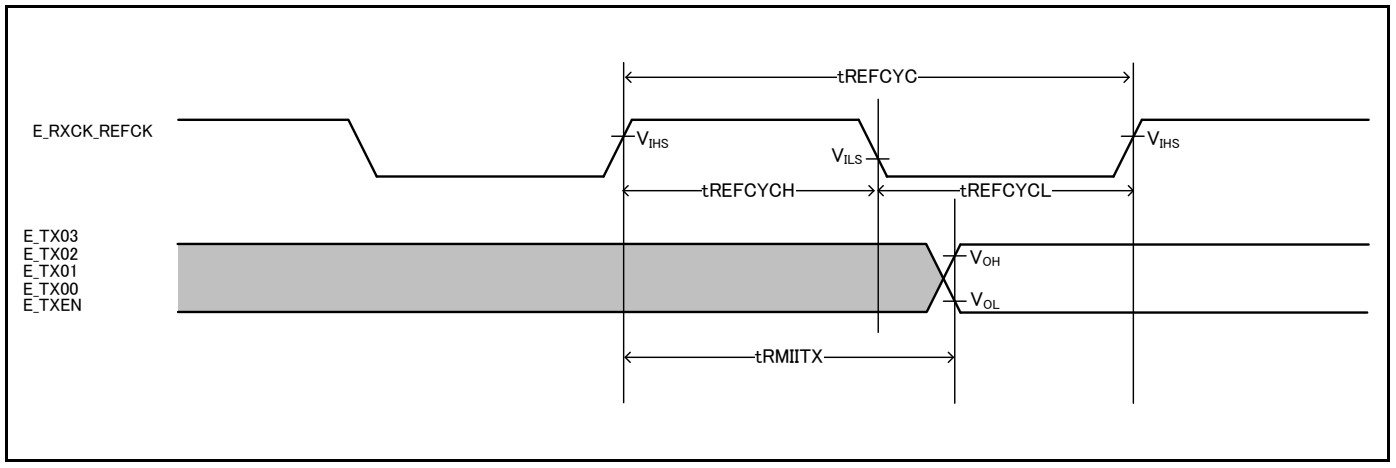
RMII Transmission (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V*1, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time*2	t_{REFCYC}	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	$t_{REFCYCH}$	E_RXCK_REFCK	$t_{REFCYCH}/t_{REFCYC}$	35	65	%
Reference clock Low-pulse-width duty cycle	$t_{REFCYCL}$	E_RXCK_REFCK	$t_{REFCYCL}/t_{REFCYC}$	35	65	%
REFCK ↑ → Transmitted data delay time	t_{RMIITX}	E_TX03, E_RX02, E_TX01, E_TX00, E_TXEN	-	-	12	ns

*1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

*2: The reference clock is fixed to 50 MHz in the RMII specifications. The clock accuracy should meet the PHY-device specifications.



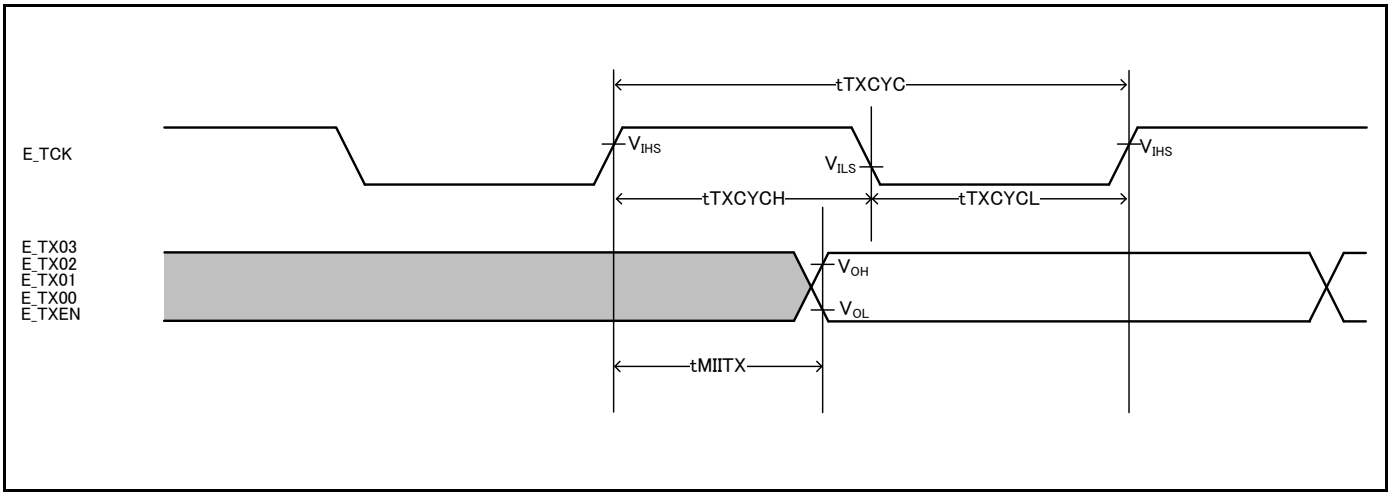
MII Transmission (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V[*1], V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Transmission clock Cycle time*2	t_{TXCYC}	E_TCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Transmission clock High-pulse-width duty cycle	t_{TXCYCH}	E_TCK	t_{TXCYCH}/t_{TXCYC}	35	65	%
Transmission clock Low-pulse-width duty cycle	t_{TXCYCL}	E_TCK	t_{TXCYCL}/t_{TXCYC}	35	65	%
TXCK ↑ → Transmitted data delay time	t_{MIITX}	E_TX03, E_TX02, E_TX01, E_TX00, E_TXEN	-	-	24	ns

1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

2: The transmission clock is fixed to 25 MHz or 2.5 MHz in the MII specifications. The clock accuracy should meet the PHY-device specifications.



12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	-	-	± 4.5	LSB	AVRH = 2.7 V to 5.5 V Offset calibration when used
Differential nonlinearity	-	-	-	-	± 2.5	LSB	
Zero transition voltage	V_{ZT}	Anxx	-	± 2	± 7	LSB	
Full-scale transition voltage	V_{FST}	Anxx	-	AVRH ± 2	AVRH ± 7	LSB	
Total error	-	-	-	± 3	± 8	LSB	
Conversion time	-	-	0.5 *1	-	-	µs	AV_{CC} ≥ 4.5 V
Sampling time *2	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-	1000		AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	Anxx	-	-	5	µA	
Analog input voltage	-	Anxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck ＜50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

1: The conversion time is the value of sampling time (t_S) + compare time (t_C).
The condition of the minimum conversion time is when the value of Ts = 150 ns and Tc = 350 ns (AV_{CC} ≥ 4.5V). Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).
For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 1. S6E2G Series Block Diagram in this data sheet.
The sampling clock and compare clock are set at base clock (HCLK).

2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

3: The compare time (t_C) is the value of (Equation 2).