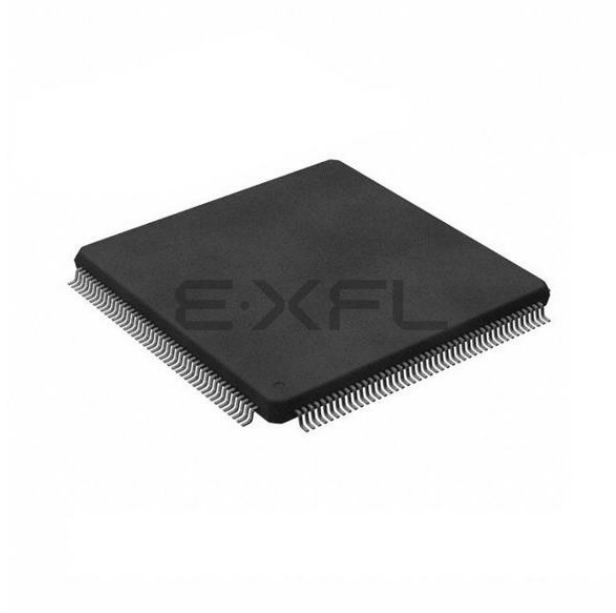


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gk8j0agv2000a

Table of Contents

4. Product Features in Detail

32-bit ARM Cortex-M4F Core

- Up to 180 MHz frequency operation
- FPU built-in
- Support DSP instructions
- Memory protection unit (MPU): improves the reliability of an embedded system
- Integrated nested vectored interrupt controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit system timer (Sys Tick): system timer for OS task management

On-chip Memories

- Flash memory

This series is on-chip flash memories.

  - Up to 1024 Kbytes
  - Built-in flash accelerator for zero wait state
  - Security function for code protection

- SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to the I-code bus and D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to system bus of Cortex-M4F core.

  - SRAM0: up to 128 Kbytes
  - SRAM1: 32 Kbytes
  - SRAM2: 32 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-/32-bit data width
- Up to 25-bit address bus
- Supports address/data multiplexing
- Supports external RDY function
- Supports scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key
  - **Note:** It is necessary to use the Cypress provided software library to use the scramble function.

USB Interface (Max two channels)

The USB interface is composed of a Device and a Host.

- USB Device
  - USB 2.0 Full-speed supported
  - Max 6 EndPoint supported
    - EndPoint 0 is control transfer
    - EndPoint 1,2 can be selected bulk-transfer, interrupt-transfer or isochronous-transfer
    - EndPoint 3 to 5 can select bulk-transfer or interrupt-transfer
  - EndPoint 1 to 5 comprise double buffer
  - The size of each endpoint is as follows.
    - Endpoint 0, 2 to 5: 64 byte
    - EndPoint 1: 256 byte
- USB Host
  - USB2.0 Full-Speed/Low-Speed supported
  - Bulk-transfer, interrupt-transfer, and isochronous-transfer support
  - USB Device connected/dis-connected automatically detect
  - IN/OUT token handshake packet automatically
  - Max 256-byte packet length supported
  - Wake-up function supported

CAN Interface (Max one channel) Available on S6E2GM and S6E2GH Devices Only

- Compatible with CAN specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32-message buffer

Multi-function Serial Interface (Max 10 Channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 1 and channels 4 to 7.
- Operation mode is selectable for each channel from the following:
  - UART
  - CSIO (SPI)
  - LIN
  - I^2C
  - I^2S
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch 6 and ch 7 only)
  - Supports high-speed SPI (ch 4 and ch 6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/slave mode supported
  - LIN break field generation (can change to 13- to 16-bit length)

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
66	56	P4E	L	Q
		SCK9_0 (SCL9_0)		
		INT05_0		
		WKUP2		
		MCSX1_0		
67	57	P70	L	I
		ADTG_7		
		SOT9_0 (SDA9_0)		
		MCSX0_0		
68	58	P71	I	K
		ADTG_8		
		SIN9_0		
		INT04_1		
		MRDY_0		
69	59	P72	E	I
		TIOB0_0		
		INT06_2		
		MAD00_0		
70	60	P73	E	K
		SIN8_0		
		TIOB1_0		
		INT20_0		
		MAD01_0		
71	61	P74	E	I
		SOT8_0 (SDA8_0)		
		TIOB2_0		
		MAD02_0		
72	62	P75	E	I
		SCK8_0 (SCL8_0)		
		TIOB3_0		
		MAD03_0		
73	63	P76	E	K
		SIN6_0		
		TIOB4_0		
		INT21_0		
		MAD04_0		
74	64	P77	L	I
		SOT6_0 (SDA6_0)		
		TIOB5_0		
		MAD05_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
119	95	P29 AN25 SCK5_0 (SCL5_0) INT09_2 MAD13_0	F	M
120	96	P28 AN26 SOT5_0 (SDA5_0) INT10_2 MAD14_0	F	M
121	97	P27 AN27 SIN5_0 INT24_0 MAD15_0	F	M
122	98	P26 ADTG_6 TIOA6_2 INT11_2 MAD16_0	E	M
123	99	P25 AN28 TIOB6_2 INT25_0 MAD17_0	F	M
124	100	P24 AN29 TIOA13_1 MAD18_0	F	L
125	101	P23 UHCONX1 AN30 SCK0_0 (SCL0_0) TIOB13_1	F	L
126	102	P22 AN31 SOT0_0 (SDA0_0) INT26_0	E	M

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
151	121	PC6 TIOA14_0 E_MDIO	K	V
152	122	PC7 INT13_0 E_MDC CROUT_1	E	W
153	123	PC8 E_RXCK_REFCK	K	V
154	124	PC9 TIOB15_0 E_COL	K	V
155	125	PCA TIOA15_0 E_CRS	K	V
156	126	ETHVCC	-	-
157	127	VSS	-	-
158	128	PCB INT28_0 E_COUT	L	W
159	129	PCC E_TCK	K	V
160	130	PCD SOT4_1 (SDA4_1) INT14_0 E_TXER	L	W
161	131	PCE SIN4_1 INT15_0 E_TX03	L	W
162	132	PCF RTS4_1 INT12_0 E_TX02	L	W
163	133	PD0 INT30_1 E_TX01	L	W
164	134	PD1 INT31_1 E_TX00	L	W
165	135	PD2 CTS4_1 E_TXEN	L	V

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External interrupt	INT14_0	External interrupt request 14 input pin	160	130
	INT14_1		141	-
	INT15_0	External interrupt request 15 input pin	161	131
	INT15_1		142	-
	INT16_0	External interrupt request 16 input pin	20	17
	INT16_1		35	30
	INT17_0	External interrupt request 17 input pin	21	18
	INT17_1		36	31
	INT18_0	External interrupt request 18 input pin	22	19
	INT18_1		37	32
	INT19_0	External interrupt request 19 input pin	26	21
	INT19_1		38	33
	INT20_0	External interrupt request 20 input pin	70	60
	INT20_1		82	-
	INT21_0	External interrupt request 21 input pin	73	63
	INT21_1		83	-
	INT22_0	External interrupt request 22 input pin	76	66
	INT22_1		58	-
	INT23_0	External interrupt request 23 input pin	46	38
	INT23_1		59	-
	INT24_0	External interrupt request 24 input pin	121	97
	INT24_1		107	87
	INT25_0	External interrupt request 25 input pin	123	99
	INT25_1		97	81
	INT26_0	External interrupt request 26 input pin	126	102
	INT26_1		116	92
	INT27_0	External interrupt request 27 input pin	127	103
	INT27_1		117	93
	INT28_0	External interrupt request 28 input pin	158	128
	INT28_1		167	-
	INT29_0	External interrupt request 29 input pin	166	136
	INT29_1		168	-
	INT30_0	External interrupt request 30 input pin	169	137
	INT30_1		163	133
	INT31_0	External interrupt request 31 input pin	172	140
	INT31_1		164	134
	NMIX	Non-maskable interrupt input pin	128	104

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P30	General-purpose I/O port 3	24	-
	P31		25	-
	P32		26	21
	P33		27	22
	P34		28	23
	P35		31	26
	P36		32	27
	P37		33	28
	P38		34	29
	P39		35	30
	P3A		36	31
	P3B		37	32
	P3C		38	33
	P3D		39	34
	P3E		40	35
	P40	General-purpose I/O port 4	46	38
	P41		47	39
	P42		48	40
	P43		49	41
	P44		50	42
	P45		51	43
	P46		55	47
	P47		56	48
	P48		60	50
	P49		61	51
	P4A		62	52
	P4B		63	53
	P4C		64	54
	P4D		65	55
	P4E		66	56
	P50	General-purpose I/O port 5	10	-
	P51		11	-
	P52		12	-
	P5D		41	-
	P5E		42	-
	P5F		43	-
	P60	General-purpose I/O port 6	172	140
	P61		171	139
	P62		170	138
	P63		169	137
	P64		168	-
	P65		167	-
	P6E		166	136

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Timer 1	DTTI1X_0	Input signal controlling waveform generator outputs RTO10 to RTO15 of Multi-Function Timer 1.	60	50
	DTTI1X_1		78	-
	FRCK1_0	16-bit free-run timer ch 1 external clock input pin	65	55
	FRCK1_1		79	-
	IC10_0	16-bit input capture input pin of Multi-Function Timer 1. ICxx describes channel number.	61	51
	IC10_1		80	-
	IC11_0		62	52
	IC11_1		81	-
	IC12_0		63	53
	IC12_1		82	-
	IC13_0		64	54
	IC13_1		83	-
	RTO10_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	46	38
	RTO10_1 (PPG10_1)		139	-
	RTO11_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	47	39
	RTO11_1 (PPG10_1)		140	-
	RTO12_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	48	40
	RTO12_1 (PPG12_1)		141	-
	RTO13_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	49	41
	RTO13_1 (PPG12_1)		142	-
	RTO14_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	50	42
	RTO14_1 (PPG14_1)		143	-
	RTO15_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	51	43
	RTO15_1 (PPG14_1)		144	-

8. Handling Precautions

Every semiconductor device has a characteristic, inherent rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins that connect semiconductor devices to power supply and I/O functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present for extended periods of time, can damage the device; therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power-supply pin or ground pin.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) *1,*3	$USBV_{CC}0$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) *1,*3	$USBV_{CC}1$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for Ethernet-MAC) *1, *4	$ETHV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1 ,*5	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1 ,*5	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	Except for USB and Ethernet-MAC pin
		V_{SS} - 0.5	$USBV_{CC}0$ + 0.5 (≤ 6.5 V)	V	USB ch 0 pin
		V_{SS} - 0.5	$USBV_{CC}1$ + 0.5 (≤ 6.5 V)	V	USB ch 1 pin
		V_{SS} - 0.5	$ETHV_{CC}$ + 0.5 (≤ 6.5 V)	V	Ethernet-MAC Pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current *6	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
L level average output current *7	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*8	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current *6	I_{OH}	-	- 10	mA	4 mA type
			-20	mA	8 mA type
			- 20	mA	12 mA type
H level average output current *7	I_{OHAV}	-	- 4	mA	4 mA type
			-8	mA	8 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current *8	$\sum I_{OHAV}$	-	- 50	mA	
Storage temperature	T_{STG}	- 55	+ 150	°C	

1: These parameters are based on the condition that V_{SS} = AV_{SS} = 0.0 V.

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$$

- I_{OL}: L level output current
- I_{OH}: H level output current
- V_{OL}: L level output voltage
- V_{OH}: H level output voltage

I_{CC} is the current drawn by the device.
It can be analyzed as follows.

$$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$$

I_{CC} (INT): Current drawn by internal logic and memory, etc. through the regulator

ΣI_{CC} (IO): Sum of current (I/O switching current) drawn by the output pin

For I_{CC} (INT), it can be anticipated by "(1) Current Rating" in "12.3. DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For I_{CC} (IO), it depends on system used by customers.
The calculation formula is shown below.

$$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times f_{SW}$$

- C_{INT}: Pin internal load capacitance
- C_{EXT}: External load capacitance of output pin
- f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself:

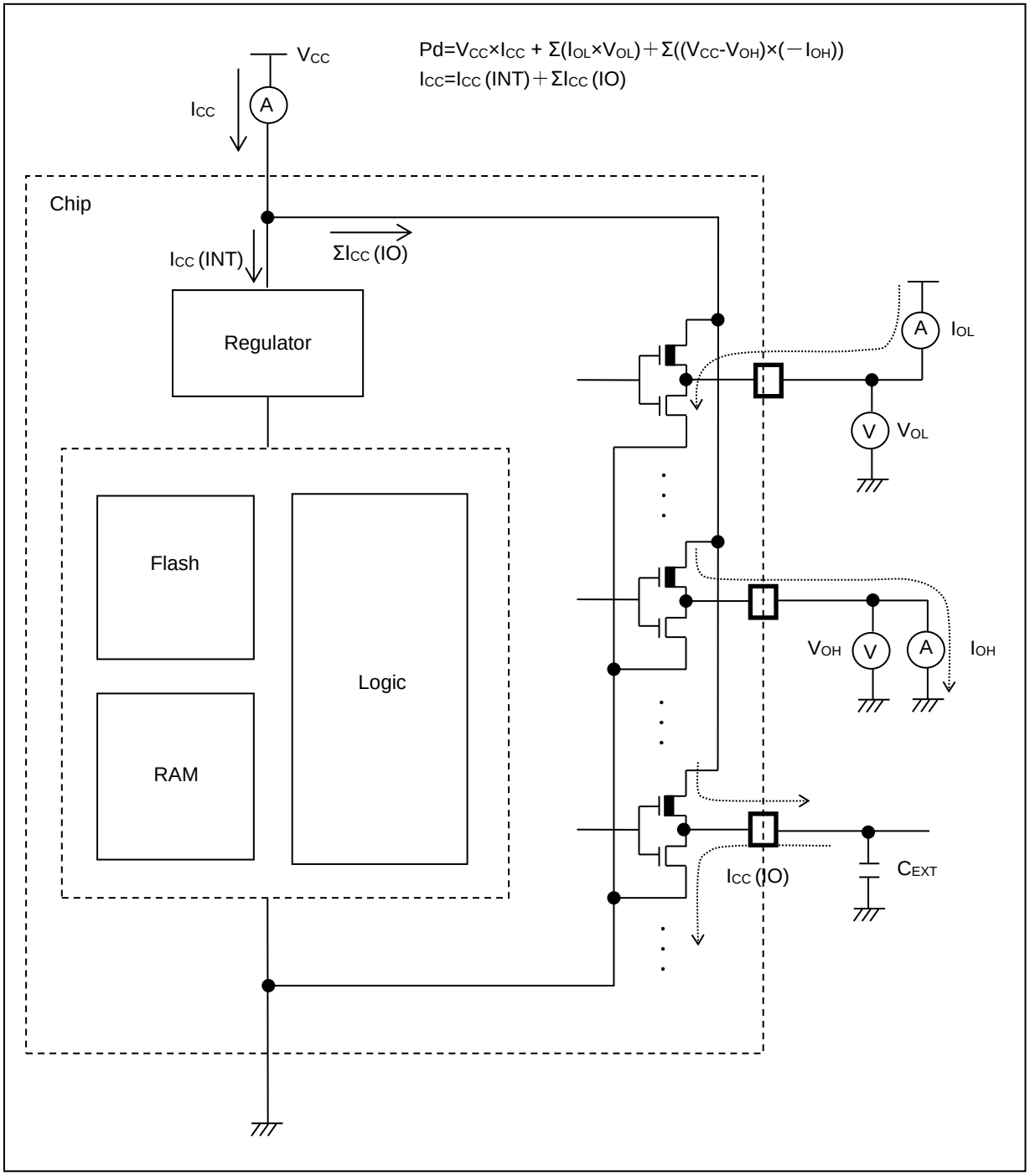
Measure current value I_{CC} (Typ) at normal temperature (+25°C).

Add maximum leakage current value I_{CC} (leak_max) at operating on a value in (1).

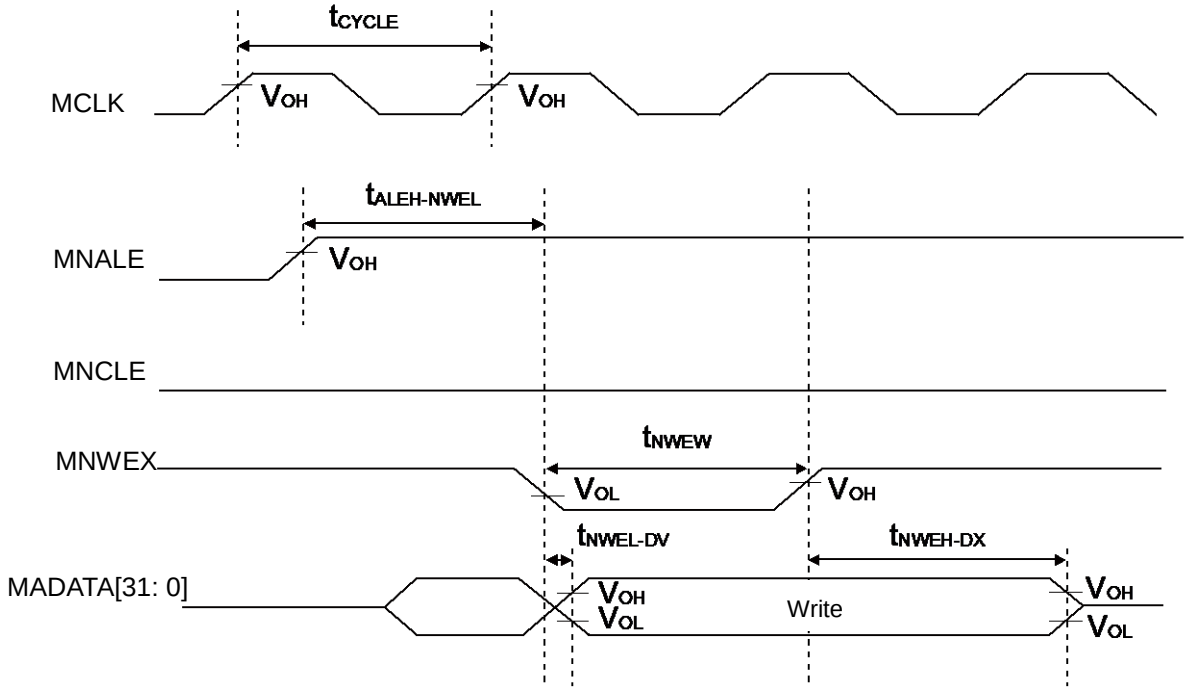
$$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	I_{CC} (leak_max)	T_J = +125 °C	53.6 mA
		T_J = +105 °C	26.6 mA
		T_J = +85 °C	17.5 mA

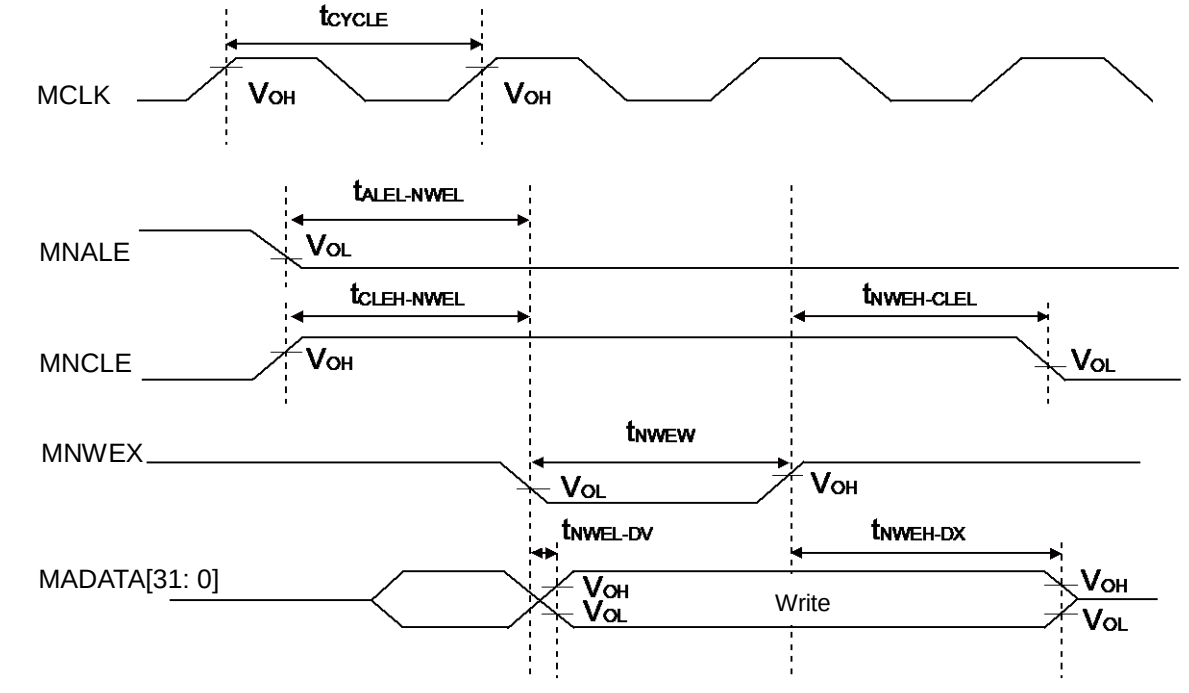
Current Explanation Diagram



NAND Flash Address Write



NAND Flash Command Write



When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↓ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t_{DEE}		0	-	0	-	ns

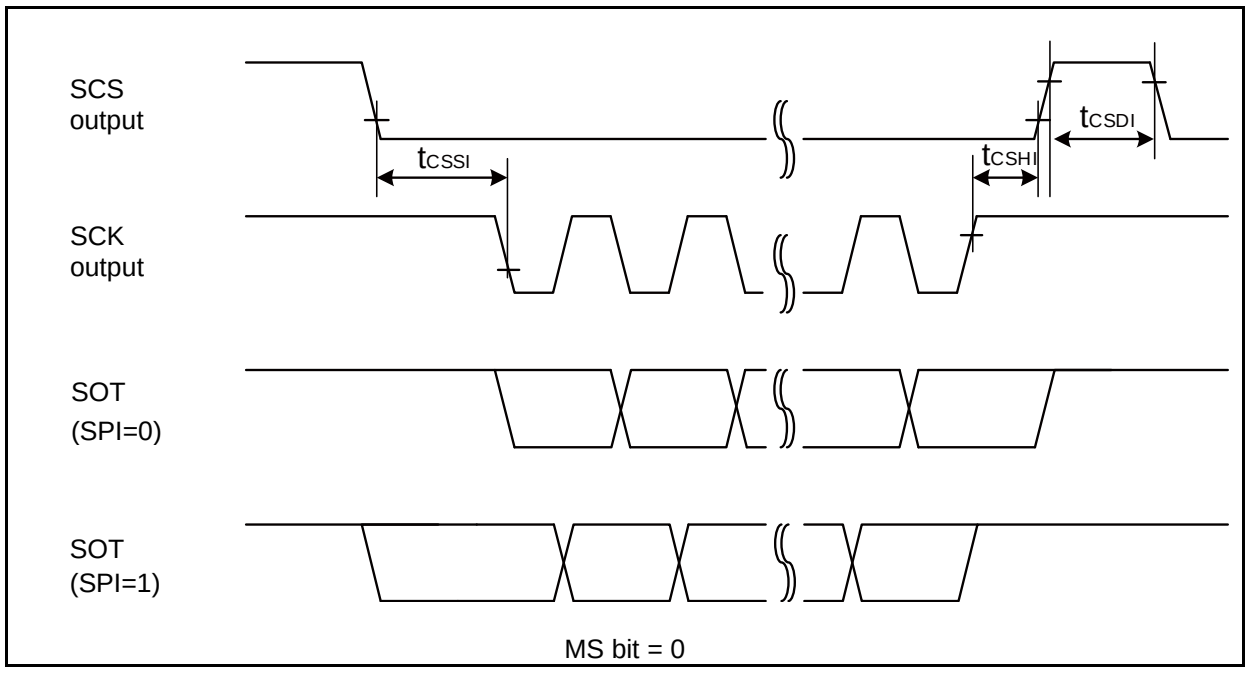
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

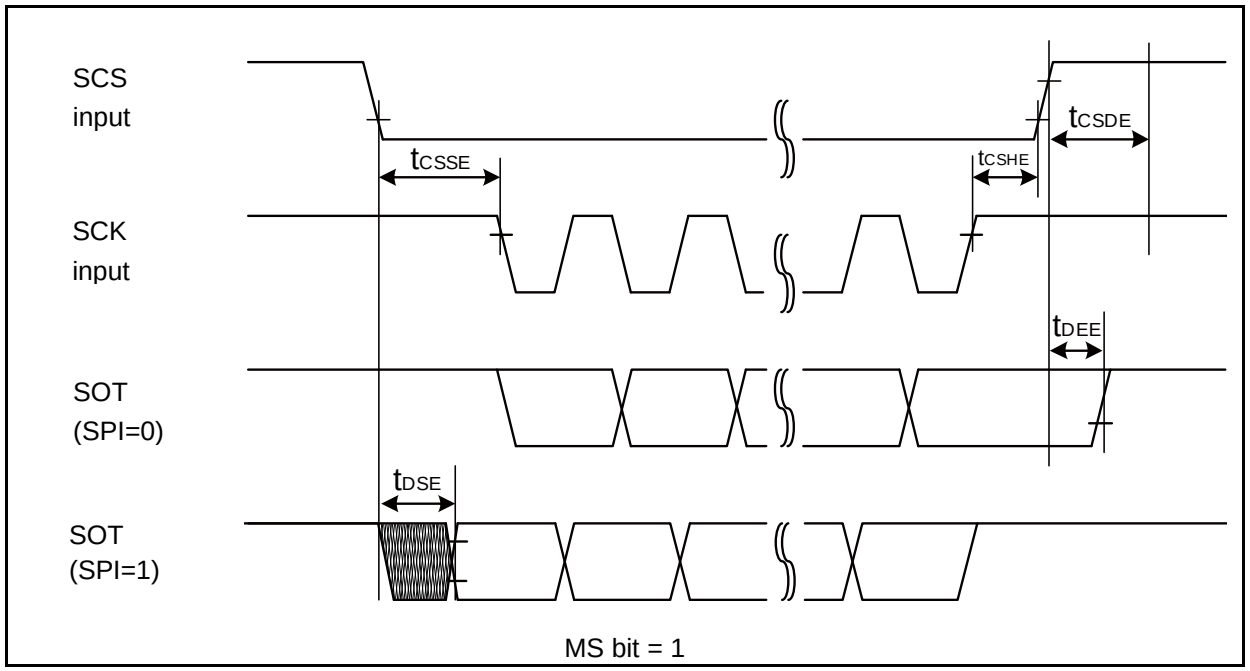
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*


SCS
output
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSHI
tCSDI
MS bit = 0


SCS
input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSHE
tCSDE
tDEE
tDSE
MS bit = 1

High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

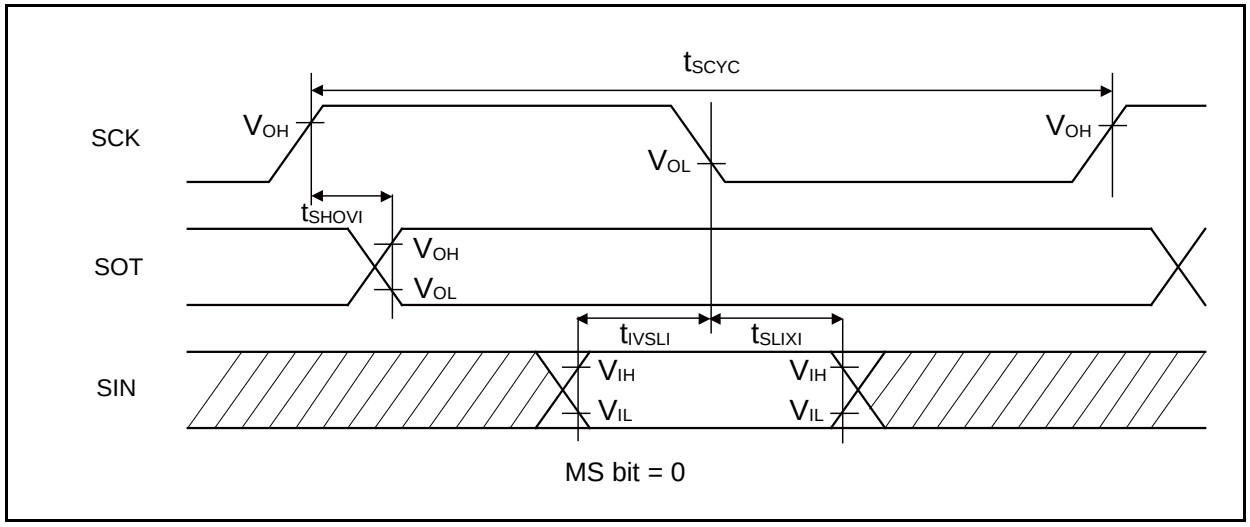
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

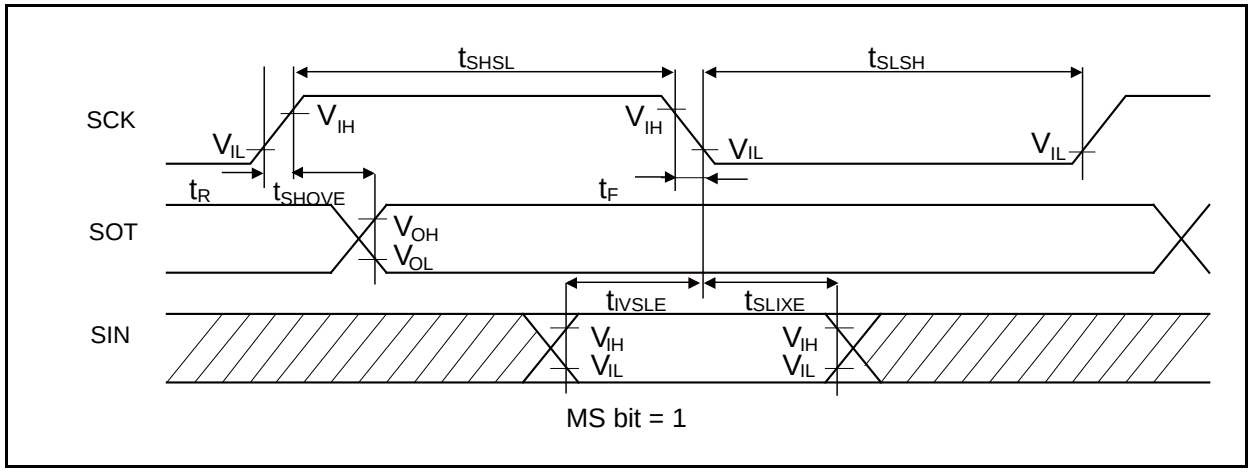
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

12.9 Standby Recovery Time

12.9.1 Recovery Cause: Interrupt/WKUP

The time from the interrupt occurring to the time of program operation start is shown.

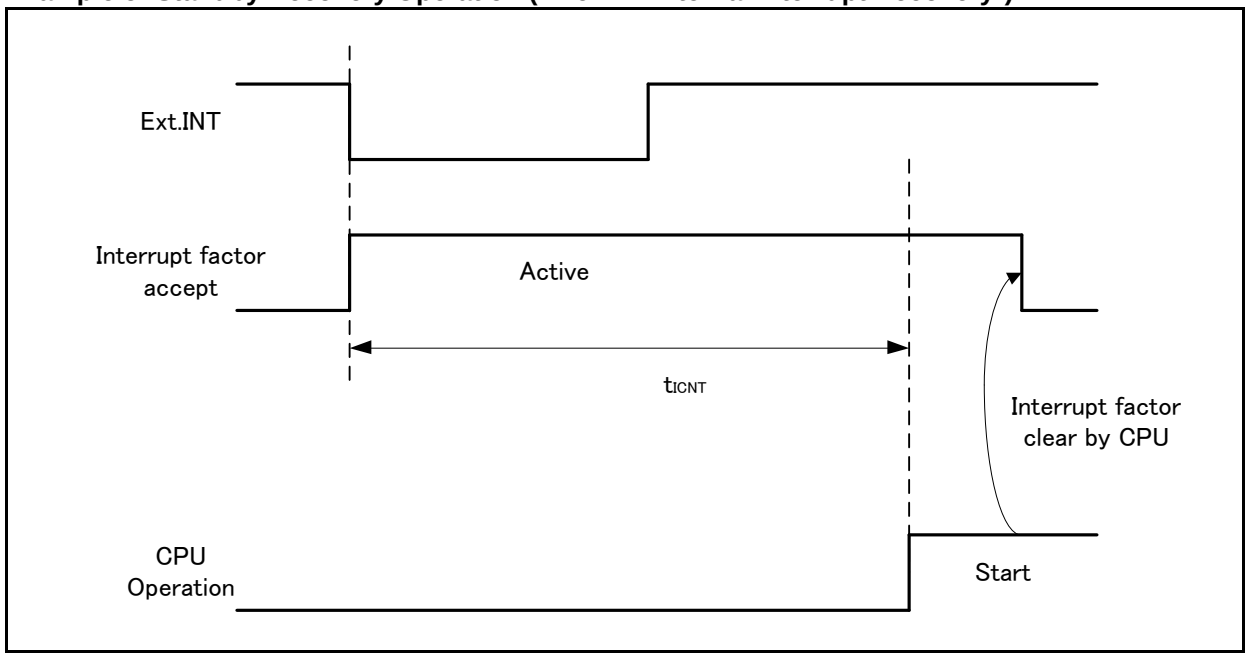
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		450	900	µs	
Sub Timer mode		896	1136	µs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		316	581	µs	
RTC mode Stop mode (Low-speed CR/sub Run mode return)		270	540	µs	
Deep Standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		365	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

Document History

Document Title: S6E2G Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller
Document Number: 001-98708

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4861788	YOHO	07/27/2015	New Spec.
*A	4945035	HITK	11/20/2015	Changed status from Preliminary to Final. Updated 4 Pin Description: Added “Note” about TAP pins. Updated 12.2 Recommended Operating Conditions: Added the "Smoothing capacitor (C_S)”. Added the “Current Value” in “Maximum leak current at operating”. Updated 12.3.1 Current Rating: Updated Table 12-1 to Table 12-9: Added the “MAX” value. Updated Table 12-11: Updated 12.5 12-bit A/D Converter: Updated “Zero transition” and “Full-scale transition” value. Added “Total error”.
*B	5122844	BOO	03/29/2016	Removed full multiplexed signal names from the Pin Assignments drawing. Consolidated the G Series of Cypress MCUs into one data sheet. Added tables to differentiate parts in 2 Product Lineup and 3 Package-Dependent Features. Expanded 13 Ordering Information. Added hyperlinks to 6 Pin Descriptions. Added circuit type D to 7 I/O Circuit Type and pin state types S and T to 11 Pin Status in Each CPU State. Consolidated 10 Memory Map to two pages.
*C	5448447	YSKA	04/12/2017	Changed to new Cypress logo. Modified typo about the number(from 5 to 4) of powerts.(Page 11) Updated “12.4.8 Power-On Reset Timing”. Changed parameter from “Power Supply rise time(t_{VCCR}) [ms]” to “Power ramp rate(dV/dt) [mV/us]” and add some comments. (Page 107) Modified “12.4.12 CSIO(SPI) Timing”. Deleted “SPI=1, MS=0” in the titles and added MS=0,1 in the schematic (Page 128-135, 144-151) Deleted Baud rate spec for High-Speed Synchronous Serial in “12.4.12 CSIO(SPI) Timing”(Page 136-142) “Modified RTC description in “4. Product Features in Detail, Real-Time Clock(RTC)” Changed starting count value from 01 to 00. Deleted “second , or day of the week” in the Interrupt function (Page 9) Updated “14. Package dimensions”(Page 186-187) Change the name from “USB Function” to “USB Device” (Page 50) Deleted MPNs below from “13. Ordering Information” (Page 185) S6E2G26H0AGV20000, S6E2G26HHAGV20000, S6E2G26J0AGV20000, S6E2G26JHAGV20000, S6E2G28H0AGV20000, S6E2G28HHAGV20000, S6E2G28J0AGV20000, S6E2G28JHAGV20000, S6E2G36H0AGV20000, S6E2G36J0AGV20000, S6E2G38H0AGV20000, S6E2G38J0AGV20000, S6E2GH6H0AGV20000, S6E2GH6J0AGV20000, S6E2GH8H0AGV20000, S6E2GH8J0AGV20000, S6E2GK6H0AGV20000, S6E2GK6HHAGV20000, S6E2GK6J0AGV20000, S6E2GK6JHAGV20000, S6E2GK8H0AGV20000, S6E2GK8HHAGV20000, S6E2GK8J0AGV20000, S6E2GK8JHAGV20000, S6E2GM6H0AGV20000, S6E2GM6HHAGV20000, S6E2GM6J0AGV20000,