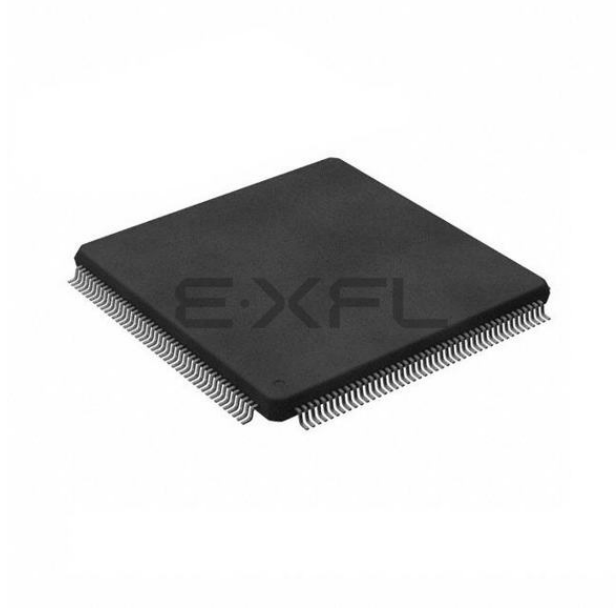

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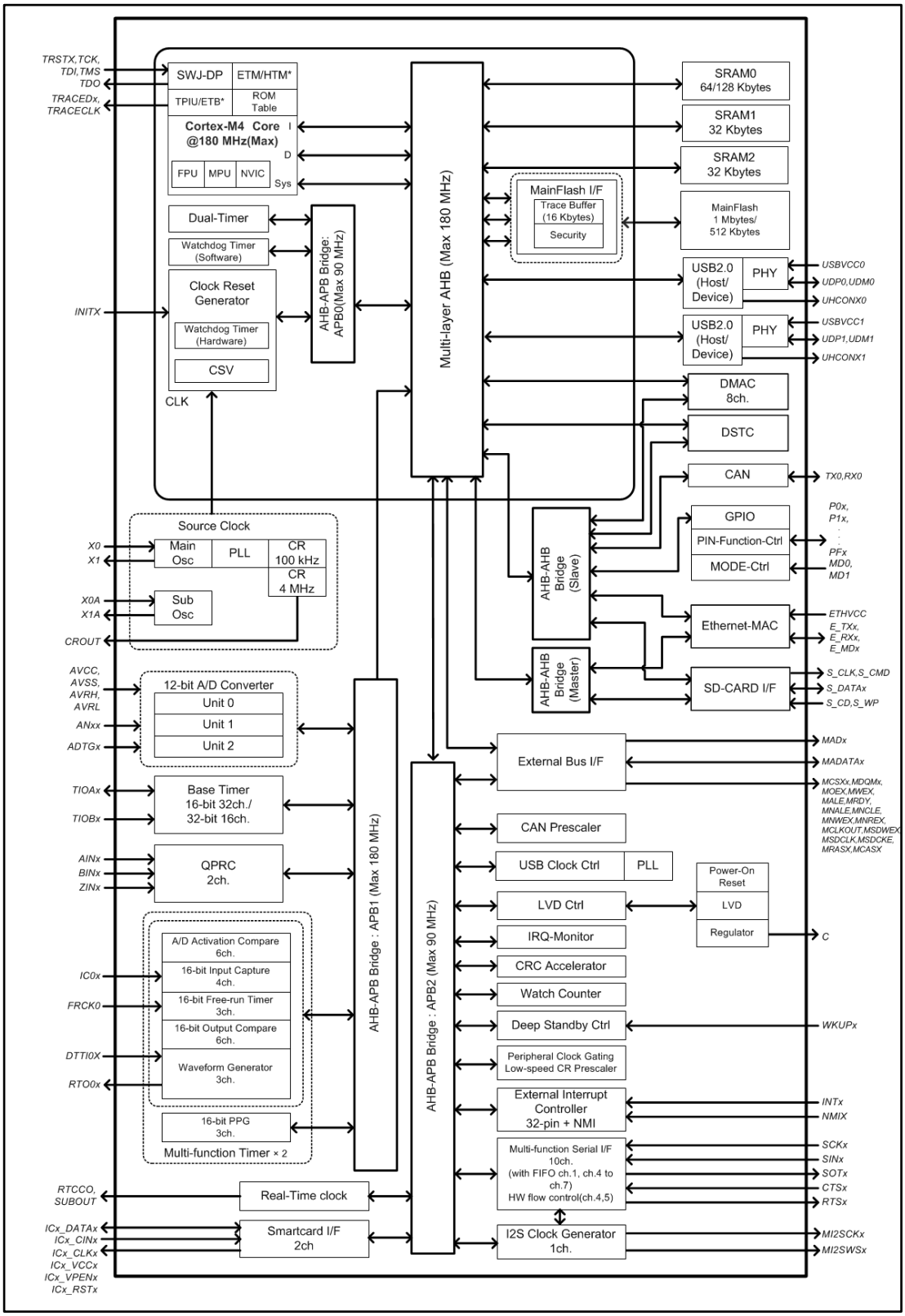
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gk8jhagv2000a

Table of Contents

1. S6E2G Series Block Diagram



6. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
1	1	VCC	-	-
2	2	PA0 RTO00_1 (PPG00_1) TIOA8_0 INT00_0 MADATA00_0 IC0_CIN_0	E	K
3	3	PA1 RTO01_1 (PPG01_1) TIOA9_0 MADATA01_0 IC0_DATA_0	E	I
4	4	PA2 RTO02_1 (PPG02_1) TIOA10_0 MADATA02_0 IC0_RST_0	E	I
5	5	PA3 RTO03_1 (PPG03_1) TIOA11_0 MADATA03_0 IC0_VPEN_0	E	I
6	6	PA4 RTO04_1 (PPG04_1) TIOA12_0 MADATA04_0 IC0_VCC_0	E	I
7	7	PA5 RTO05_1 (PPG05_1) TIOA13_0 INT01_0 MADATA05_0 IC0_CLK_0	E	K

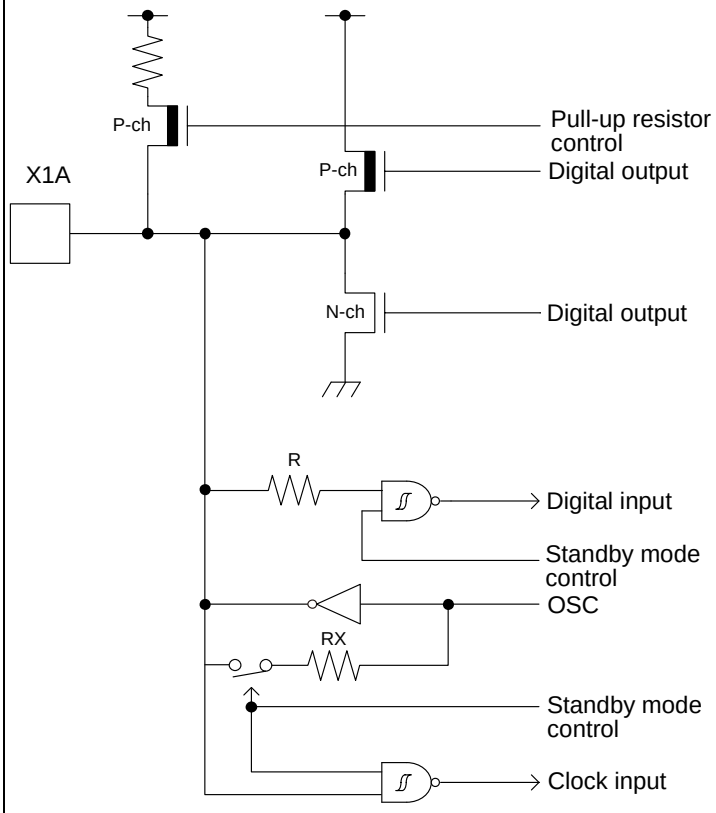
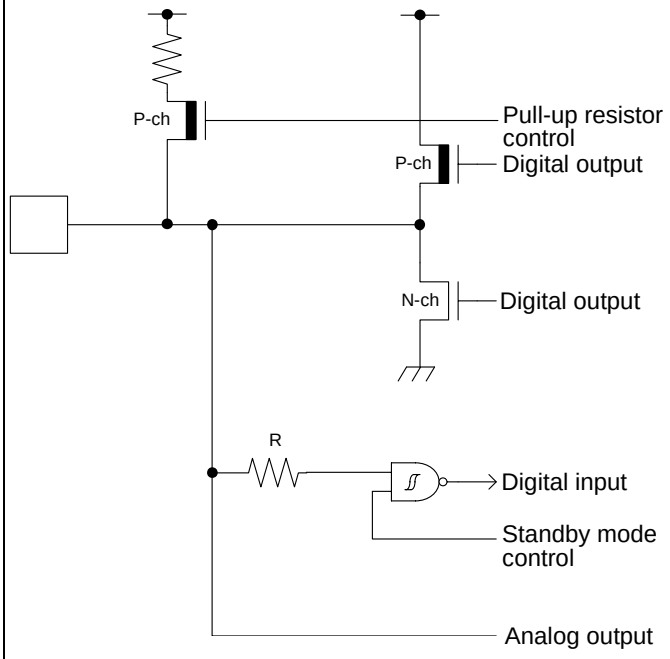
Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
18	15	PAD	N	I
		SCK3_0 (SCL3_0)		
		TIOB9_0		
		MADATA13_0		
19	16	PAE	N	I
		ADTG_0		
		SOT3_0 (SDA3_0)		
		TIOB10_0		
		MADATA14_0		
20	17	PAF	I	K
		SIN3_0		
		TIOB11_0		
		INT16_0		
		MADATA15_0		
21	18	P08	E	K
		TIOB12_0		
		INT17_0		
		MDQM0_0		
22	19	P09	E	K
		TIOB13_0		
		INT18_0		
		MDQM1_0		
23	20	P0A	L	I
		ADTG_1		
		MCLKOUT_0		
24	-	P30	E	K
		MI2SWS1_1		
		RX0_1		
		TIOB11_2		
		INT01_2		
25	-	P31	E	I
		MI2SMCK1_1		
		TX0_1		
		TIOA12_2		
26	21	P32	L	K
		INT19_0		
		S_DATA1_0		
27	22	P33	L	I
		FRCK0_0		
		S_DATA0_0		

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Timer 0	DTTI0X_0	Input signal controlling waveform generator outputs RTO00 to RTO05 of Multi-Function Timer 0.	34	29
	DTTI0X_1		8	8
	FRCK0_0	16-bit free-run timer ch 0 external clock input pin	27	22
	FRCK0_1		13	10
	IC00_0	16-bit input capture input pin of Multi-Function Timer 0. ICxx describes channel number.	33	28
	IC00_1		9	9
	IC01_0		32	27
	IC01_1		10	-
	IC02_0		31	26
	IC02_1		11	-
	IC03_0		28	23
	IC03_1		12	-
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	35	30
	RTO00_1 (PPG00_1)		2	2
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	36	31
	RTO01_1 (PPG00_1)		3	3
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	37	32
	RTO02_1 (PPG02_1)		4	4
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	38	33
	RTO03_1 (PPG02_1)		5	5
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	39	34
	RTO04_1 (PPG04_1)		6	6
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	40	35
	RTO05_1 (PPG04_1)		7	7

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Reset	INITX	External reset Input pin A reset is valid when INITX = L.	57	49
Mode	MD1	Mode 1 pin During serial programming to flash memory, MD1 = L must be input.	84	68
	MD0	Mode 0 pin During normal operation, MD0 = L must be input. During serial programming to flash memory, MD0 = H must be input.	85	69
Power	VCC	Power supply pin	1	1
			29	24
			45	37
			54	46
			89	73
			133	109
	USBVCC0	3.3V power supply port for USB I/O	173	141
	USBVCC1		129	105
	ETHVCC	Power supply pin for Ethernet I/O	156	126
GND	VSS	GND pin	30	25
			44	36
			53	45
			88	72
			132	108
			157	127
			176	144
Clock	X0	Main clock (oscillation) input pin	86	70
	X1	Main clock (oscillation) I/O pin	87	71
	X0A	Sub clock (oscillation) input pin	55	47
	X1A	Sub clock (oscillation) I/O pin	56	48
	CROUT_0	Built-in high-speed CR-oscillation clock output port	127	103
	CROUT_1		152	122
Analog power	AVCC	A/D converter and D/A converter analog power-supply pin	90	74
	AVRL	A/D converter analog reference voltage input pin	92	76
	AVRH	A/D converter analog reference voltage input pin	93	77
Analog GND	AVSS	A/D converter and D/A converter GND pin	91	75
C pin	C	Power supply stabilization capacity pin	52	44

Note:

- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

Type	Circuit	Remarks
Q		It is possible to select the sub oscillation/GPIO function. When the sub oscillation is selected: ・ Oscillation feedback resistor: approximately 10 MΩ When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA
R		・ CMOS level output ・ CMOS level hysteresis input ・ Analog output ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA (4.5V to 5.5V) ・ I_{OH} = -2 mA, I_{OL} = 2 mA (2.7V to 4.5V)

Latch-Up

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic pnpn junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF		Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_C8FF		Reserved
0x4003_C900	0x4003_C9FF		I2S clock generator
0x4003_CA00	0x4003_CAFF		Smartcard Interface
0x4003_CB00	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface

12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	180 MHz	73	131	mA	*3 When all peripheral clocks are on
				*6	160 MHz	65	123	mA	
					144 MHz	59	117	mA	
					120 MHz	50	108	mA	
					100 MHz	43	101	mA	
					80 MHz	35	93	mA	
					60 MHz	27	85	mA	
					40 MHz	19	77	mA	
					20 MHz	11	69	mA	
					8 MHz	6.9	64	mA	
					4 MHz	5.3	63	mA	
				*5	180 MHz	44	102	mA	*3 When all peripheral clocks are off
				*6	160 MHz	40	98	mA	
					144 MHz	36	94	mA	
					120 MHz	31	89	mA	
					100 MHz	27	85	mA	
					80 MHz	22	80	mA	
					60 MHz	17	75	mA	
					40 MHz	13	71	mA	
					20 MHz	7.9	65	mA	
					8 MHz	5.2	63	mA	
					4 MHz	4.3	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

6: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory."

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

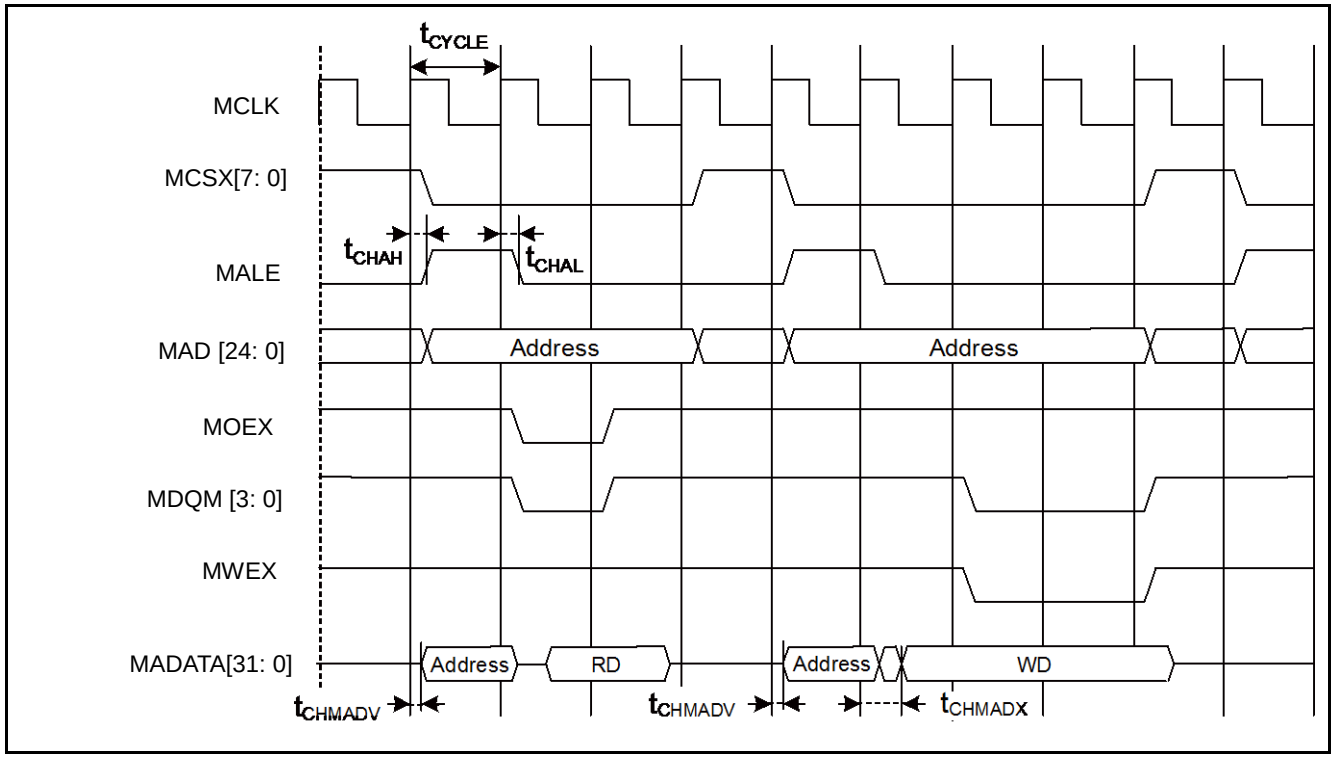
Multiplexed Bus Access Synchronous SRAM Mode

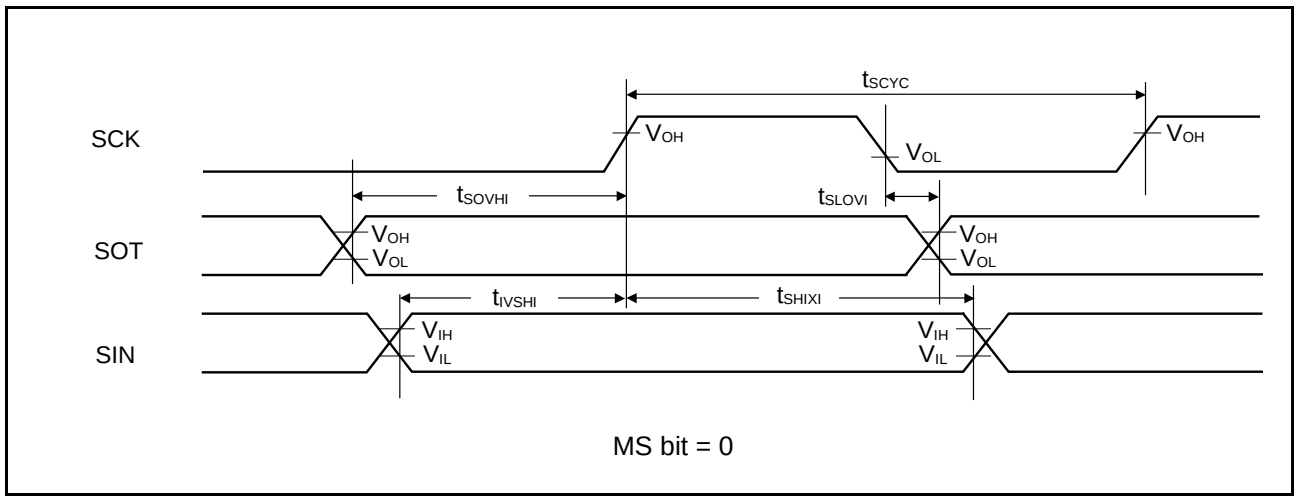
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, MALE	-	1	9		
	t_{CHAH}		-	1	9		
MCLK ↑ →Multiplexed address delay time	t_{CHMADV}	MCLK, MADATA[31: 0]	-	1	t_{OD}	ns	
MCLK ↑ →Multiplexed data output time	t_{CHMADX}		-	1	t_{OD}	ns	

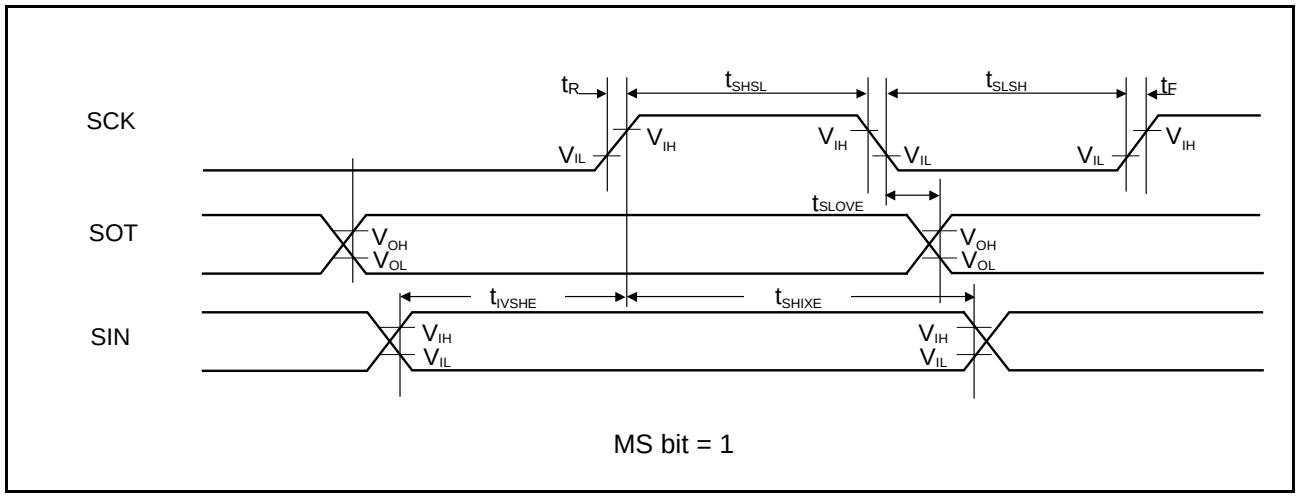
Note:

- *When the external load capacitance C_L = 30 pF*





MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↓ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t_{DEE}		0	-	0	-	ns

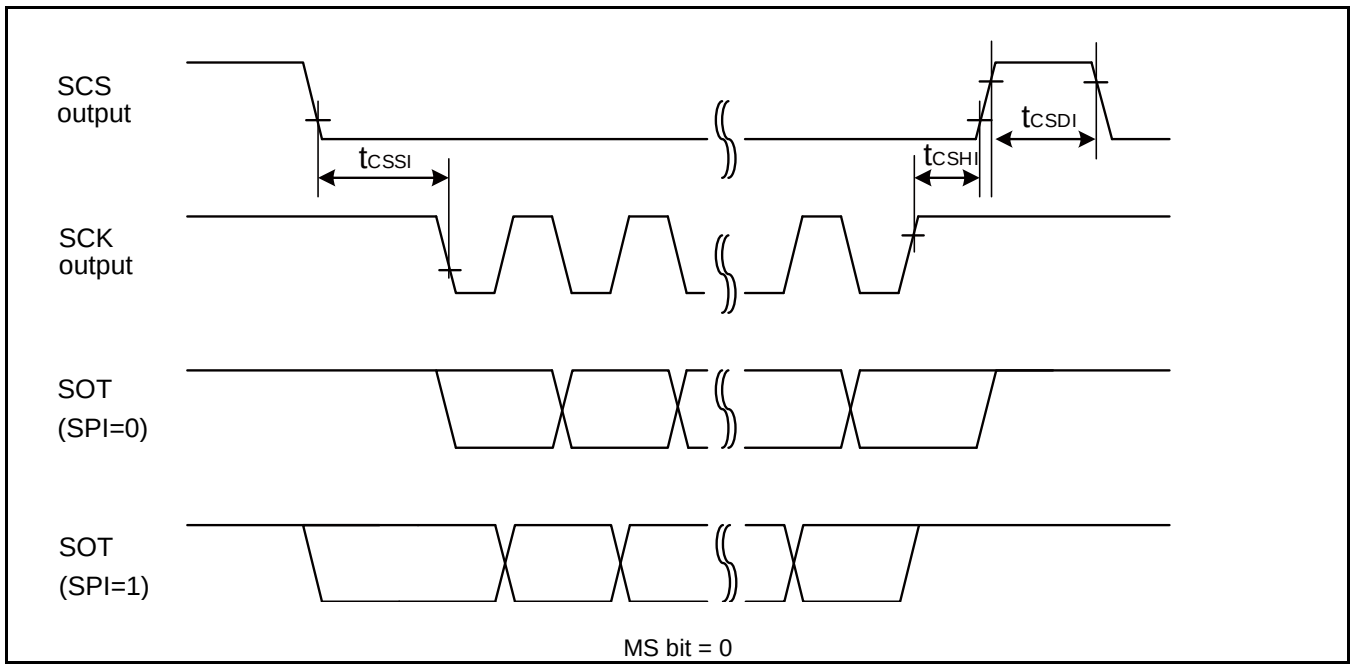
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

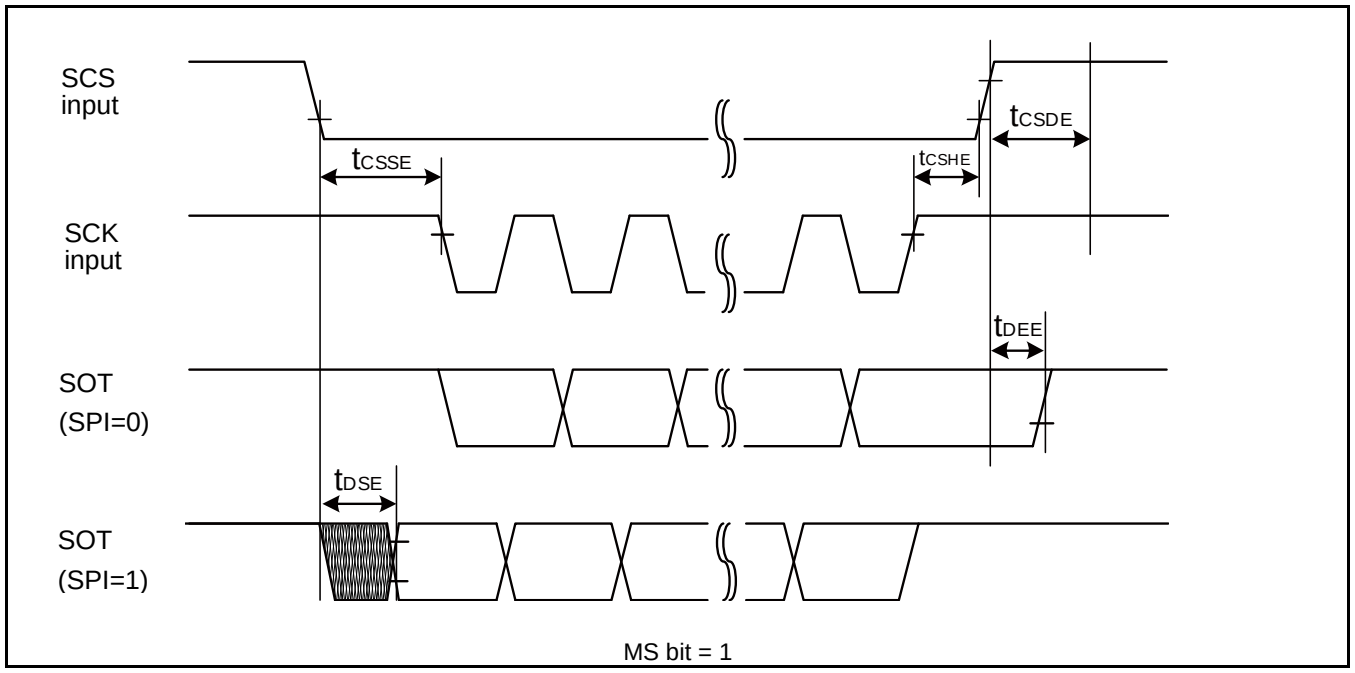
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

12.4.13 External Input Timing

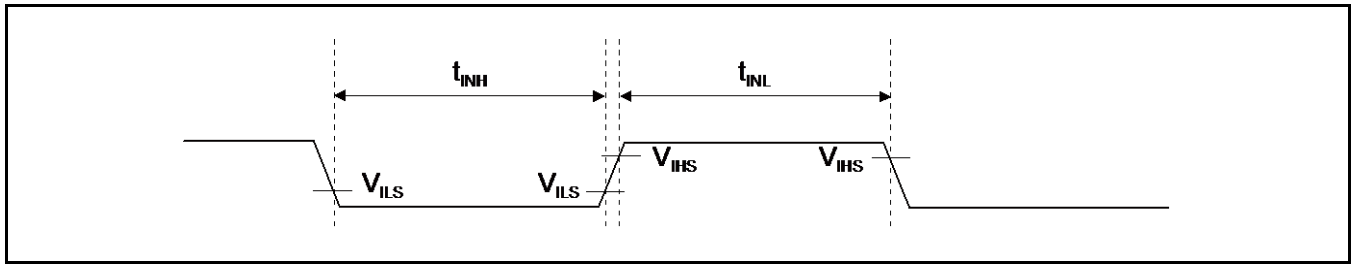
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

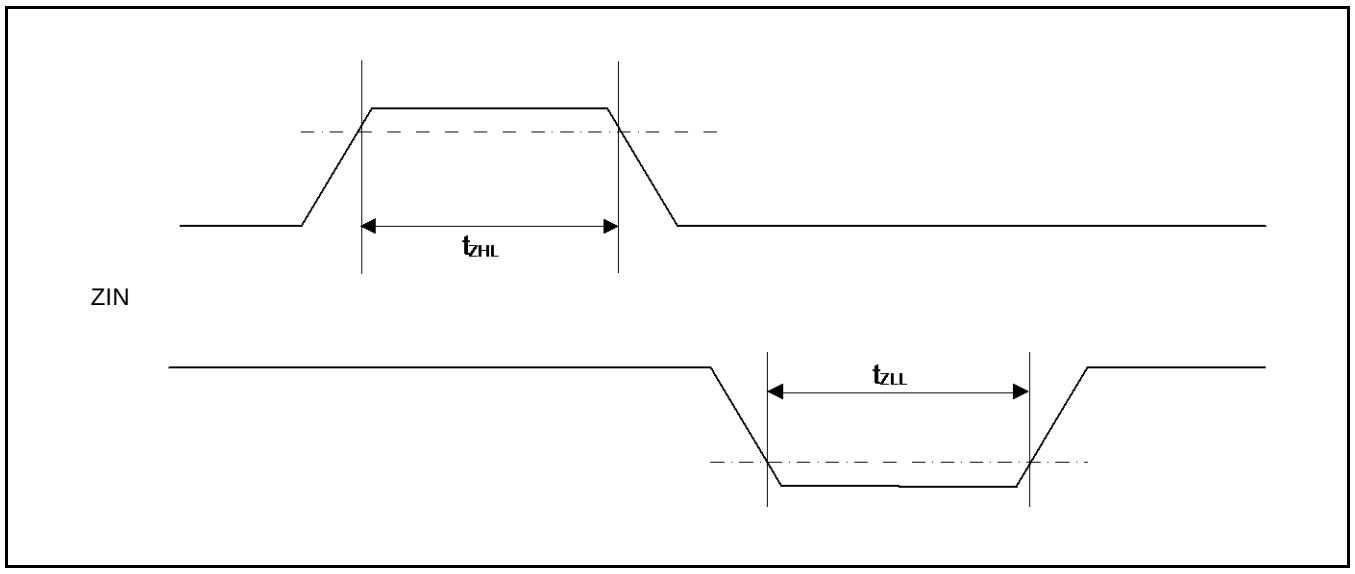
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		Icxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

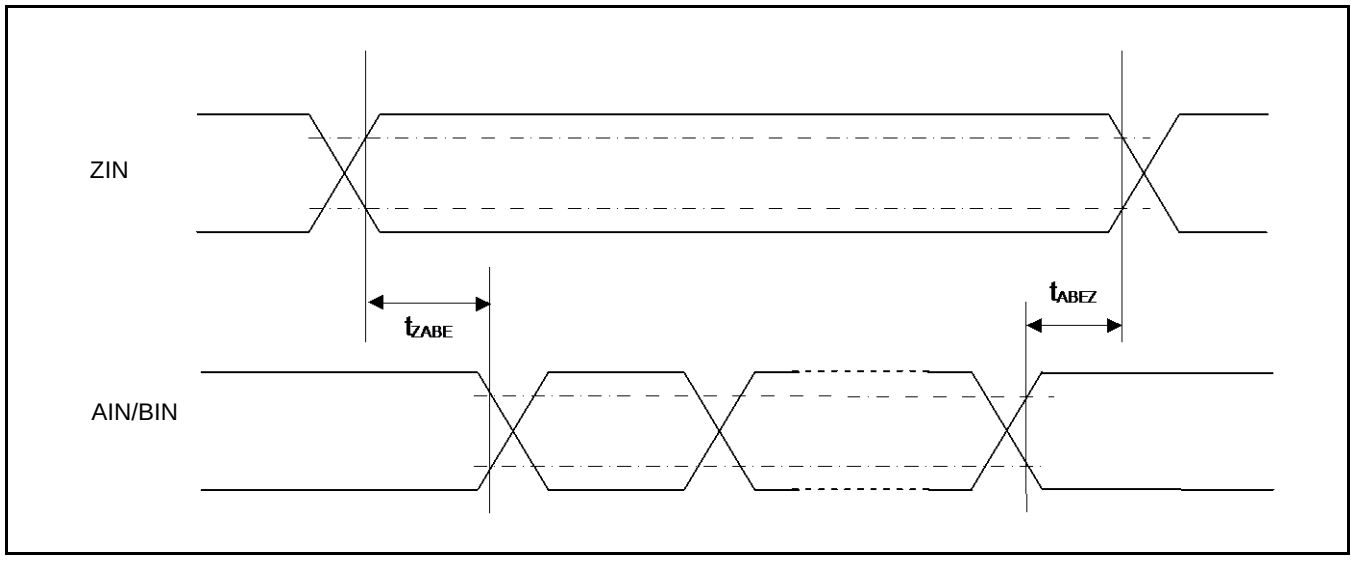
1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 1. S6E2G Series Block Diagram in this data sheet.

2: When in Stop mode, in Timer mode

3: When in Deep Standby RTC mode, in Deep Standby Stop mode




ZIN
tZHL
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.4.15 I²C Timing

Standard-Mode, Fast-Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and START condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP} < 40 MHz	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	*5
		40 MHz ≤ t_{CYCP} < 60 MHz	4 t_{CYCP}*4	-	4 t_{CYCP}*4	-	ns	
		60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	6 t_{CYCP}*4	-	ns	
		80 MHz ≤ t_{CYCP} ≤100 MHz	8 t_{CYCP}*4	-	8 t_{CYCP}*4	-	ns	

1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

2: The maximum t_{HDDAT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

3: Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns.

4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I²C is connected, see 1.S6E2G Series Block Diagram in this data sheet.
When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.
When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.

5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	-	-	± 4.5	LSB	AVRH = 2.7 V to 5.5 V Offset calibration when used
Differential nonlinearity	-	-	-	-	± 2.5	LSB	
Zero transition voltage	V_{ZT}	Anxx	-	± 2	± 7	LSB	
Full-scale transition voltage	V_{FST}	Anxx	-	AVRH ± 2	AVRH ± 7	LSB	
Total error	-	-	-	± 3	± 8	LSB	
Conversion time	-	-	0.5 *1	-	-	µs	AV_{CC} ≥ 4.5 V
Sampling time *2	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-	1000		AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	Anxx	-	-	5	µA	
Analog input voltage	-	Anxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck ＜50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

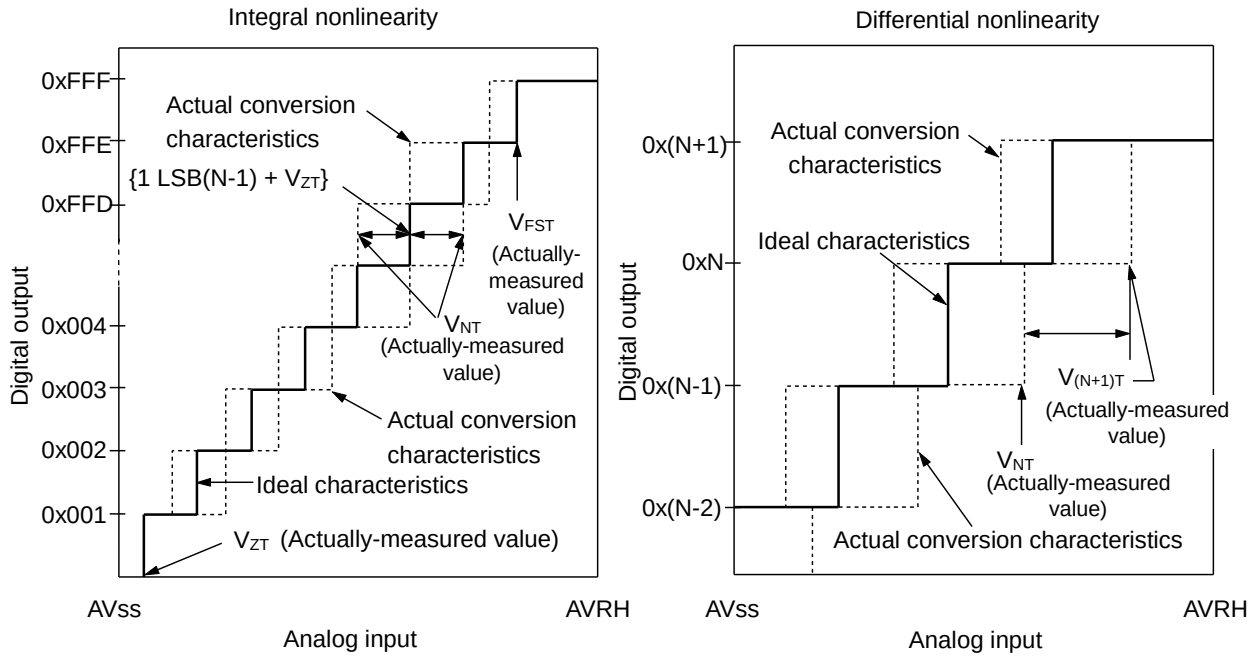
1: The conversion time is the value of sampling time (t_S) + compare time (t_C).
The condition of the minimum conversion time is when the value of Ts = 150 ns and Tc = 350 ns (AV_{CC} ≥ 4.5V). Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).
For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 1. S6E2G Series Block Diagram in this data sheet.
The sampling clock and compare clock are set at base clock (HCLK).

2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

3: The compare time (t_C) is the value of (Equation 2).

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

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