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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CSIO, EBI/EMI, I <sup>2</sup> C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I <sup>2</sup> S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192К х 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gk8jhagv2000a

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# **S6E2G Series**

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## 1. S6E2G Series Block Diagram







## 6. Pin Descriptions

## **List of Pin Functions**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number		Dia Mara	I/O	Pin State
LQFP-176	LQFP-144		Туре	Туре
1	1	VCC	-	-
		PA0		
		RTO00_1 (PPG00_1)		
2	2	TIOA8_0	Е	к
		INT00_0		
		MADATA00_0		
		IC0_CIN_0		
		PA1		
		RTO01_1 (PPG01_1)	_	
3	3	TIOA9_0	E	1
		MADATA01_0		
		IC0_DATA_0		
		PA2		
	4	RTO02_1 (PPG02_1)	_	
4		TIOA10_0	E	I.
		MADATA02_0		
		IC0_RST_0		
	5	PA3		
_		RTO03_1 (PPG03_1)	_	
5		TIOA11_0	E	
		MADATA03_0		
		IC0_VPEN_0		
		PA4		
		RTO04_1 (PPG04_1)	_	
6	6	TIOA12_0	E	1
		MADATA04_0		
		IC0_VCC_0		
		PA5		
		RTO05_1 (PPG05_1)		
7	7	TIOA13_0	Е	к
		INT01_0		
		MADATA05_0		
		IC0_CLK_0		





Pin N	umber	Dia Nama	I/O	Pin State	
LQFP-176	LQFP-144	Pin Name	Туре	Туре	
		PAD			
		SCK3_0			
18	15	(SCL3_0)	N	I	
-		TIOB9_0	_		
			_		
		SOT3 0	_		
19	16	(SDA3_0)	N	I	
		TIOB10_0			
		MADATA14_0			
		PAF			
		SIN3_0			
20	17	TIOB11_0	I	K	
		INT16_0			
		MADATA15_0			
		P08			
21	18	TIOB12_0	F	к	
21		INT17_0	_		
		MDQM0_0			
	19	P09			
22		TIOB13_0	E	К	
		INT18_0			
		MDQM1_0			
		P0A	_		
23	20	ADTG_1	L	l.	
		MCLKOUT_0			
		P30	_		
		MI2SWS1_1			
24	-	RX0_1	E	K	
		TIOB11_2			
		INT01_2			
		P31			
25		MI2SMCK1_1	_	I.	
20	-	TX0_1		I	
		TIOA12_2			
		P32			
26	21	INT19_0	L	K	
		S_DATA1_0			
		P33			
27	22	FRCK0_0	L	I.	
		S_DATA0_0			





Module Pin Name		From a film.	Pin Number			
wodule	Pin Name	Function	LQFP 176	LQFP 144		
	DTTI0X_0	Input signal controlling waveform	34	29		
	DTTI0X_1	Multi-Function Timer 0.	8	8		
	FRCK0_0	16-bit free-run timer ch 0 external	27	22		
	FRCK0_1	clock input pin	13	10		
	IC00_0		33	28		
	IC00_1		9	9		
	IC01_0		32	27		
	IC01_1	16-bit input capture input pin of	10	-		
	IC02_0	ICxx describes channel number.	31	26		
	IC02_1		11	-		
	IC03_0		28	23		
	IC03_1		12	-		
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0.	35	30		
N 414:	RTO00_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG0 output modes.	2	2		
Function	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0.	36	31		
	RTO01_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG0 output modes.	3	3		
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0.	37	32		
	RTO02_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output modes.	4	4		
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0.	38	33		
	RTO03_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output modes.	5	5		
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0.	39	34		
	RTO04_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output modes.	6	6		
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0.	40	35		
·	RTO05_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output modes.	7	7		





Modulo	Din Namo	Function	Pin Number			
Wodule	Fill Name	T unction	LQFP 176	LQFP 144		
Reset	INITX	External reset Input pin A reset is valid when INITX = L.	57	49		
	MD1	Mode 1 pin During serial programming to flash memory, MD1 = L must be input.	84	68		
Mode	MD0	Mode 0 pin During normal operation, MD0 = L must be input. During serial programming to flash memory, MD0 = H must be input.	85	69		
			1	1		
			29	24		
	2400	Dever events air	45	37		
	VCC	Power supply pin	54	46		
Power			89	73		
			133	109		
	USBVCC0		173	141		
	USBVCC1	3.3V power supply port for USB I/O	129	105		
	ETHVCC	Power supply pin for Ethernet I/O	156	126		
	VSS	GND pin	30	25		
			44	36		
			53	45		
GND			88	72		
			132	108		
			157	127		
			176	144		
	X0	Main clock (oscillation) input pin	86	70		
	X1	Main clock (oscillation) I/O pin	87	71		
Clask	X0A	Sub clock (oscillation) input pin	55	47		
CIOCK	X1A	Sub clock (oscillation) I/O pin	56	48		
	CROUT_0	Built-in high-speed CR-oscillation clock	127	103		
	CROUT_1	output port	152	122		
	AVCC	A/D converter and D/A converter analog power-supply pin	90	74		
Analog power	AVRL	A/D converter analog reference voltage input pin	92	76		
	AVRH	A/D converter analog reference voltage input pin	93	77		
Analog GND	AVSS	A/D converter and D/A converter GND pin	91	75		
C pin	С	Power supply stabilization capacity pin	52	44		

#### Note:

 While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.







### Latch-Up

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic pnpn junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- 1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- 2. Be sure that abnormal current flows do not occur during the power-on sequence.

#### **Observance of Safety Regulations and Standards**

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

#### Fail-Safe Design

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

#### **Precautions Related to Usage of Devices**

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

#### 8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

#### Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.



### **Peripheral Address Map**

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF		MainFlash I/F register
0x4000_1000	0x4000_FFFF	АНВ	Reserved
0x4001_0000	0x4001_0FFF		Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF	APB0	Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF		Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF	APB1	Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF		External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF	APB2	CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_C8FF		Reserved
0x4003_C900	0x4003_C9FF		I2S clock generator
0x4003_CA00	0x4003_CAFF		Smartcard Interface
0x4003_CB00	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface





#### 12.3 DC Characteristics

#### 12.3.1 Current Rating

Parameter Symbol		Pin	Conditions		<b>F</b> *4	Value		11	Pomorko
		Name			Frequency*	Typ* <sup>1</sup>	Max* <sup>2</sup>	Unit	Remarks
				*5	180 MHz	73	131	mA	
					160 MHz	65	123	mA	
					144 MHz	59	117	mA	
					120 MHz	50	108	mA	
					100 MHz	43	101	mA	*3
				*6	80 MHz	35	93	mA	When all peripheral
				0	60 MHz	27	85	mA	CIOCKS are on
					40 MHz	19	77	mA	
			Normal operation *7,*8 (PLL)		20 MHz	11	69	mA	
					8 MHz	6.9	64	mA	
Power	laa	VCC			4 MHz	5.3	63	mA	
supply current	ICC	VCC		*5	180 MHz	44	102	mA	
					160 MHz	40	98	mA	
					144 MHz	36	94	mA	
					120 MHz	31	89	mA	
					100 MHz	27	85	mA	*3
				*6	80 MHz	22	80	mA	When all peripheral
				0	60 MHz	17	75	mA	CIOCKS are off
					40 MHz	13	71	mA	
					20 MHz	7.9	65	mA	
					8 MHz	5.2	63	mA	
					4 MHz	4.3	62	mA	

 Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

1:  $T_A = +25 \text{ °C}, V_{CC} = 3.3 \text{ V}$ 

2:  $T_J$  = +125 °C,  $V_{CC}$  = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

6: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory."

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)



### Multiplexed Bus Access Synchronous SRAM Mode

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Devementer	0	Pin Name	Conditions	Va	11		
Parameter	Symbol			Min	Max	Unit	Remarks
	t <sub>CHAL</sub>	MCLK,	-	1	9		
MALE delay time	t <sub>CHAH</sub>	MALE	-	1	9		
MCLK ↑ →Multiplexed address delay time	tchmadv	MCLK,	-	1	top	ns	
MCLK ↑ →Multiplexed data output time	tchmadx	MADATA[31:0]	-	1	top	ns	

Note:

\_

When the external load capacitance  $C_L = 30 \ pF$ 











## When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Poromotor	Symbol	Conditions	Vcc <	4.5 V	V <sub>cc</sub> ≥	l In:t	
Falameter	Symbol	Conditions	Min	Max	Min	Max	Unit
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>		(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t <sub>CSHI</sub>	Internal shift clock	(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t <sub>CSDI</sub>	operation	(*3)-50 +5t <sub>CYCP</sub>	(*3)+50 +5t <sub>CYCP</sub>	(*3)-50 +5t <sub>СҮСР</sub>	(*3)+50 +5t <sub>СҮСР</sub>	ns
SCS↓→SCK↓ setup time	tcsse		3tcycp+30	-	3tcycp+30	-	ns
SCK↑→SCS↑ hold time	<b>t</b> CSHE		0	-	0	-	ns
SCS deselect time	t <sub>CSDE</sub>	External shift clock	3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCS↓→SOT delay time	tdse	operation	-	40	-	40	ns
SCS ↑ →SOT delay time	tDEE		0	-	0	-	ns

(\*1): CSSU bit valuexserial chip select timing operating clock cycle [ns]

(\*2): CSHD bit valuexserial chip select timing operating clock cycle [ns]

(\*3): CSDS bit valuexserial chip select timing operating clock cycle [ns]

#### Notes:

- tcycp indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance  $C_L = 30 \text{ pF}$ .









#### 12.4.13 External Input Timing

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Deremeter	Sympol	Din Nome	Conditions	Value	•	110:4	Domorko	
Parameter Symbol		Pin Name	Conditions	Min	Max	Unit	Remarks	
	tinh, tinl	ADTGx	- 2tcycp <sup>*1</sup>				A/D converter trigger input	
		FRCKx		-	2t <sub>CYCP</sub> *1	-	ns	ns
		lcxx					Input capture	
Input pulse		DTTIxX	-	2t <sub>CYCP</sub> *1	-	ns	Waveform generator	
width		INT00 to INT31, NMIX		2t <sub>CYCP</sub> + 100 <sup>*1</sup>	-	ns	External interrupt,	
				500 <sup>*2</sup>	-	ns	NMI	
		WKUPx	-	500 <sup>*3</sup>	-	ns	Deep standby wake up	

1: t<sub>CYCP</sub> indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 1. S6E2G Series Block Diagram in this data sheet.

2: When in Stop mode, in Timer mode

3: When in Deep Standby RTC mode, in Deep Standby Stop mode











#### 12.4.15 PC Timing

#### Standard-Mode, Fast-Mode

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		11		
			Min	Max	Min	Max	Unit	Remarks	
SCL clock frequency	f <sub>SCL</sub>		0	100	0	400	kHz		
(Repeated) START condition hold time SDA $\downarrow \rightarrow$ SCL $\downarrow$	<b>t</b> hdsta		4.0	-	0.6	-	μs		
SCL clock L width	tLOW		4.7	-	1.3	-	μs		
SCL clock H width	tнідн		4.0	-	0.6	-	μs		
(Repeated) START condition setup time SCL $\uparrow \rightarrow$ SDA $\downarrow$	tsusta	C <sub>L</sub> = 30 pF, R = (Vp/I <sub>OL</sub> ) <sup>*1</sup>	4.7	-	0.6	-	μs		
Data hold time SCL ↓ → SDA ↓ ↑	<b>t</b> hddat		0	3.45 <sup>*2</sup>	0	0.9 <sup>*3</sup>	μs		
Data setup time SDA $\downarrow \uparrow \rightarrow$ SCL $\uparrow$	<b>t</b> sudat		250	-	100	-	ns		
Stop condition setup time SCL $\uparrow \rightarrow$ SDA $\uparrow$	tsusтo		4.0	-	0.6	-	μs		
Bus free time between Stop condition and START condition	t <sub>BUF</sub>		4.7	-	1.3	-	μs		
Noise filter	tsp	2 MHz ≤ t <sub>CYCP</sub> <40 MHz	2 t <sub>CYCP</sub> *4	-	2 t <sub>CYCP</sub> *4	-	ns		
		40 MHz ≤         4 tcycp*4         -         4 tcycp           tcycp <60 MHz		4 tcycp*4	-	ns	*5		
		60 MHz ≤ t <sub>CYCP</sub> <80 MHz	6 tcycp*4	-	6 tcycp*4	-	ns	- 5	
		80 MHz ≤ t <sub>CYCP</sub> ≤100 MHz	8 t <sub>CYCP</sub> *4	-	8 t <sub>CYCP</sub> *4	-	ns		

1: R and C<sub>L</sub> represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.  $V_p$  indicates the power supply voltage of the pull-up resistance and  $I_{OL}$  indicates  $V_{OL}$  guaranteed current.

2: The maximum t<sub>HDDAT</sub> must not extend beyond the low period (t<sub>LOW</sub>) of the device's SCL signal.

3: Fast-mode I<sup>2</sup>C bus device can be used on a Standard-mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of "t<sub>SUDAT</sub> ≥ 250 ns.

4: t<sub>CYCP</sub> is the APB bus clock cycle time. For more information about the APB bus number to which the I<sup>2</sup>C is connected, see 1.S6E2G Series Block Diagram in this data sheet. When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.

When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.

5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.



 $(\sqrt{cc} - A)/cc - 2.7)/$  to 5.5)/  $\sqrt{cs} - A)/cs - A)/RI - 0)/)$ 

### 12.5 12-bit A/D Converter

#### **Electrical Characteristics for the A/D Converter**

Parameter	Symbol	Pin Name	Value					
			Min	Тур	Мах	Unit	Remarks	
Resolution	-	-	-	-	12	bit		
Integral nonlinearity	-	-	-	-	± 4.5	LSB		
Differential nonlinearity	-	-	-	-	± 2.5	LSB	AVRH = 2.7 V to 5.5 V Offset calibration when used	
Zero transition voltage	V <sub>ZT</sub>	Anxx	-	± 2	± 7	LSB		
Full-scale transition voltage	V <sub>FST</sub>	Anxx	-	AVRH ± 2	AVRH ± 7	LSB		
Total error	-	-	-	± 3	± 8	LSB		
Conversion time	-	-	0.5 <sup>*1</sup>	-	-	μs	AV <sub>CC</sub> ≥ 4.5 V	
Sampling time *2	ts	-	0.15	-	10	μs	AV <sub>CC</sub> ≥ 4.5 V	
			0.3	-	10		AVcc < 4.5 V	
Compare clock cycle <sup>*3</sup>	tсск	-	25	-	1000		AV <sub>CC</sub> ≥ 4.5 V	
			50	-	1000	ns	AVcc < 4.5 V	
State transition time to operation permission	t <sub>STT</sub>	-	-	-	1.0	μs		
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation	
			-	1.3	22	μA	When A/D stop	
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V	
			-	0.3	6.3	μA	When A/D stop	
Analog input capacity	CAIN	-	-	-	12.05	pF		
Analog input resistance	R <sub>AIN</sub>	-	-	-	1.2	1.0	AV <sub>CC</sub> ≥ 4.5 V	
					1.8	KΩ	AV <sub>CC</sub> < 4.5 V	
Interchannel disparity	-	-	-	-	4	LSB		
Analog port input leak current	-	Anxx	-	-	5	μA		
Analog input voltage	-	Anxx	AVss	-	AVRH	V		
			AVss	-	AVcc	V		
Reference voltage	-	AVRH	4.5	-	AVcc	, <i>.</i>	Tcck <50 ns	
			2.7	-	AVcc	V	Tcck ≥ 50 ns	
	-	AVRL	AVss	-	AVss	V		

1: The conversion time is the value of sampling time (ts) + compare time (tc).

The condition of the minimum conversion time is when the value of Ts = 150 ns and Tc = 350 ns (AV<sub>cc</sub>  $\ge$  4.5V). Ensure that it satisfies the value of sampling time (t<sub>s</sub>) and compare clock cycle (t<sub>CCK</sub>).

For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 1. S6E2G Series Block Diagram in this data sheet. The sampling clock and compare clock are set at base clock (HCLK).

2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

3: The compare time (t<sub>c</sub>) is the value of (Equation 2).



### Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral nonlinearity: Deviation of the line between the zero-transition point (0b0000000000 ←→ 0b0000000001) and the full-scale transition point (0b1111111110 ←→ 0b111111111) from the actual conversion characteristics.
- Differential nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.





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