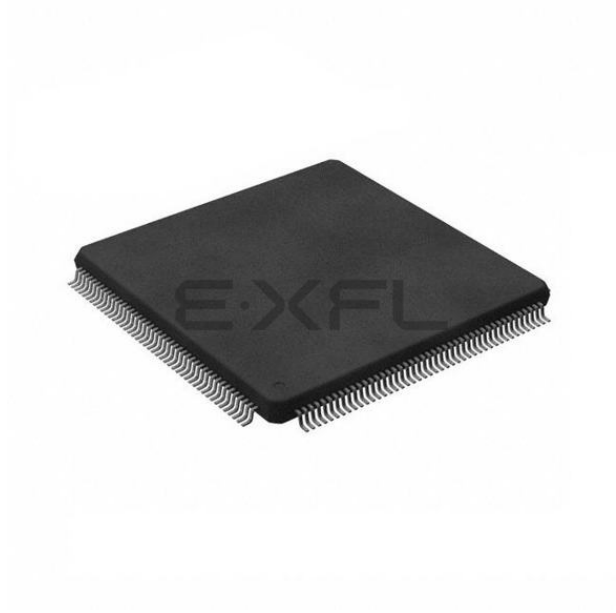

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

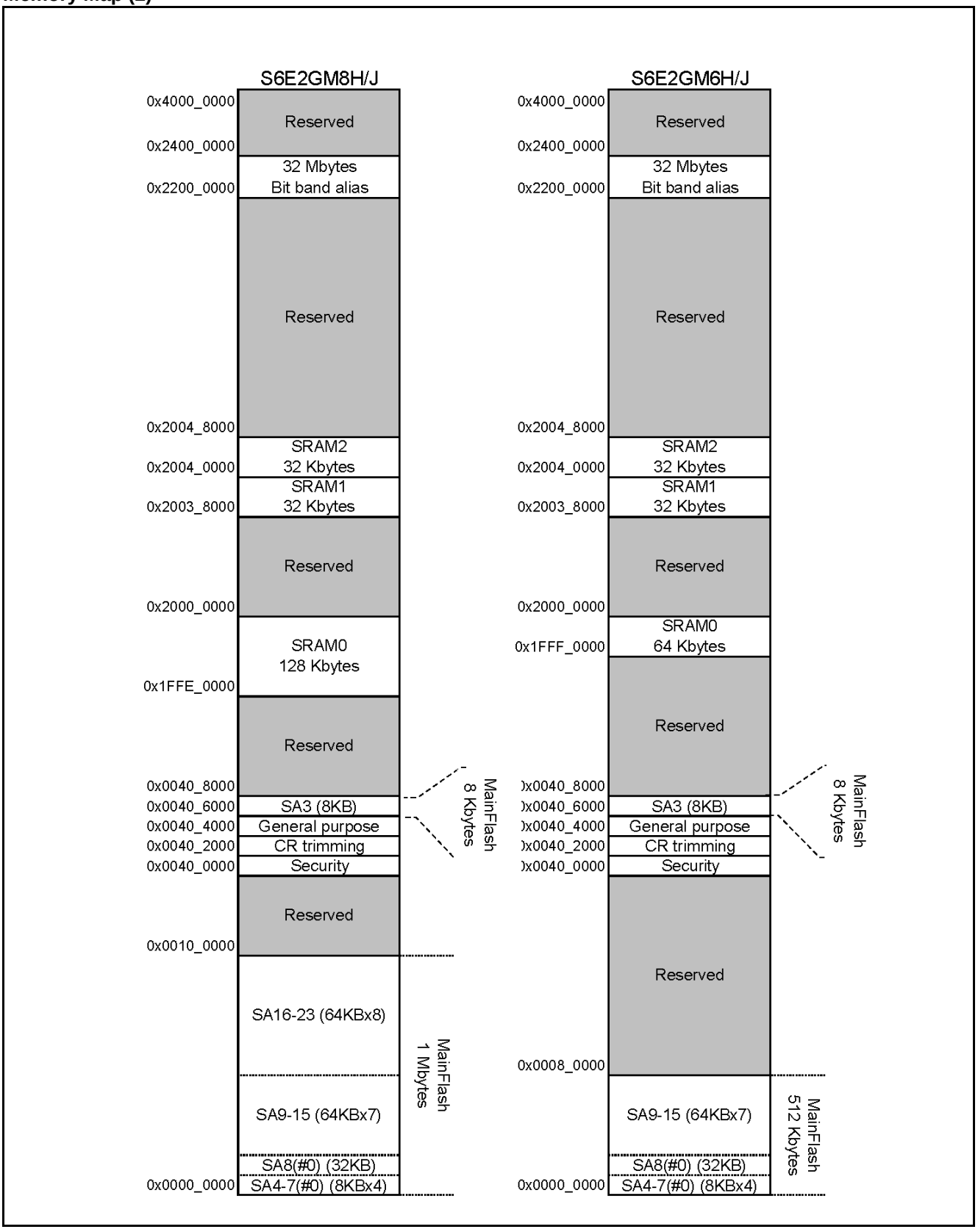
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gm6j0agv2000a

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
18	15	PAD	N	I
		SCK3_0 (SCL3_0)		
		TIOB9_0		
		MADATA13_0		
19	16	PAE	N	I
		ADTG_0		
		SOT3_0 (SDA3_0)		
		TIOB10_0		
		MADATA14_0		
20	17	PAF	I	K
		SIN3_0		
		TIOB11_0		
		INT16_0		
		MADATA15_0		
21	18	P08	E	K
		TIOB12_0		
		INT17_0		
		MDQM0_0		
22	19	P09	E	K
		TIOB13_0		
		INT18_0		
		MDQM1_0		
23	20	P0A	L	I
		ADTG_1		
		MCLKOUT_0		
24	-	P30	E	K
		MI2SWS1_1		
		RX0_1		
		TIOB11_2		
		INT01_2		
25	-	P31	E	I
		MI2SMCK1_1		
		TX0_1		
		TIOA12_2		
26	21	P32	L	K
		INT19_0		
		S_DATA1_0		
27	22	P33	L	I
		FRCK0_0		
		S_DATA0_0		

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 7	SIN7_0	Multi-function serial interface ch 7 input pin	13	10
	SIN7_1		46	38
	SOT7_0 (SDA7_0)	Multi-function serial interface ch 7 output pin This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I²C (operation mode 4).	14	11
	SOT7_1 (SDA7_1)		47	39
	SCK7_0 (SCL7_0)	Multi-function serial interface ch 7 clock I/O pin This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I²C (operation mode 4).	15	12
	SCK7_1 (SCL7_1)		48	40
	SCS70_0	Multi-function serial interface ch 7 chip select 0 input/output pin	16	13
	SCS70_1		49	41
	SCS71_0	Multi-function serial interface ch 7 chip select 1 input/output pin	17	14
	SCS71_1		50	42
	SCS72_0	Multi-function serial interface ch 7 chip select 2 input/output pin	10	-
	SCS72_1		51	43
	SCS73_0	Multi-function serial interface ch 7 chip select 3 input/output pin	11	-
	SCS73_1		58	-
Multi-Function Serial 8	SIN8_0	Multi-function serial interface ch 8 input pin	70	60
	SIN8_1		111	-
	SOT8_0 (SDA8_0)	Multi-function serial interface ch 8 output pin This pin operates as SOT8 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA8 when it is used in an I²C (operation mode 4).	71	61
	SOT8_1 (SDA8_1)		112	-
	SCK8_0 (SCL8_0)	Multi-function serial interface ch 8 clock I/O pin This pin operates as SCK8 when it is used in a CSIO (operation mode 2) and as SCL8 when it is used in an I²C (operation mode 4).	72	62
	SCK8_1 (SCL8_1)		113	-
Multi-Function Serial 9	SIN9_0	Multi-function serial interface ch 9 input pin	68	58
	SIN9_1		97	81
	SOT9_0 (SDA9_0)	Multi-function serial interface ch 9 output pin This pin operates as SOT9 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA9 when it is used in an I²C (operation mode 4).	67	57
	SOT9_1 (SDA9_1)		98	82
	SCK9_0 (SCL9_0)	Multi-function serial interface ch 9 clock I/O pin This pin operates as SCK9 when it is used in a CSIO (operation mode 2) and as SCL9 when it is used in an I²C (operation mode 4).	66	56
	SCK9_1 (SCL9_1)		99	83

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch 0 AIN input pin	46	38
	AIN0_1		75	65
	AIN0_2		103	-
	BIN0_0	QPRC ch 0 BIN input pin	47	39
	BIN0_1		76	66
	BIN0_2		104	-
	ZIN0_0	QPRC ch 0 ZIN input pin	48	40
	ZIN0_1		77	67
	ZIN0_2		105	-
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch 1 AIN input pin	35	30
	AIN1_1		14	11
	AIN1_2		111	-
	BIN1_0	QPRC ch 1 BIN input pin	36	31
	BIN1_1		15	12
	BIN1_2		112	-
	ZIN1_0	QPRC ch 1 ZIN input pin	37	32
	ZIN1_1		16	13
	ZIN1_2		113	-
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of real-time clock	171	139
	RTCCO_1		9	9
	SUBOUT_0	Sub-clock output pin	171	139
	SUBOUT_1		9	9
USB0	UDM0	USB ch 0 device/host D – pin	174	142
	UDP0	USB ch 0 device/host D + pin	175	143
	UHCONX0	USB ch 0 external pull-up control pin	171	139
USB1	UDM1	USB ch 1 device/host D – pin	130	106
	UDP1	USB ch 1 device/host D + pin	131	107
	UHCONX1	USB ch 1 external pull-up control pin	125	101
Low power consump-tion mode	WKUP0	Deep standby mode return signal input pin 0	128	104
	WKUP1	Deep standby mode return signal input pin 1	13	10
	WKUP2	Deep standby mode return signal input pin 2	66	56
	WKUP3	Deep standby mode return signal input pin 3	172	140

Memory Map (2)



*: See S6E2GM/GK/GH/G3/G2 Series Flash Programming Manual to confirm the detail of flash Memory.

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected					Maintain previous state	Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
M	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
O	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected						Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									

12.3.2 Pin Characteristics

(V_{CC} = $USBV_{CC}0$ = $USBV_{CC}1$ = $ETHV_{CC}$ = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
				$ETHV_{CC}$×0.8	-	$ETHV_{CC}$ + 0.3	V	
		MADATAxx	V_{CC} > 3.0 V, V_{CC} ≤ 3.6 V,	2.4	-	V_{CC} + 0.3	V	At External Bus
		5V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
		TTL Schmitt input pin	-	2.0	-	$ETHV_{CC}$+0.3	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
				V_{SS} - 0.3	-	$ETHV_{CC}$×0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
		TTL Schmitt input pin	-	V_{SS} - 0.3	-	0.8	V	
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2 mA					
			$ETHV_{CC}$ ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	$ETHV_{CC}$	V	
			$ETHV_{CC}$ < 4.5 V, I_{OH} = - 2 mA					
		8 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 4 mA					
			$ETHV_{CC}$ ≥ 4.5 V, I_{OH} = - 8 mA	$ETHV_{CC}$ - 0.5	-	$ETHV_{CC}$	V	
			$ETHV_{CC}$ < 4.5 V, I_{OH} = - 4 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
		The pin doubled as USB I/O	$USBV_{CC}$ ≥ 4.5 V, I_{OH} = - 20.5 mA	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	*1
			$USBV_{CC}$ < 4.5 V, I_{OH} = - 13.0 mA					
		The pin doubled as I^2C Fm+	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
			V_{CC} < 4.5V, I_{OH} = - 3 mA					

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
			$ETHV_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5$ V, I_{OL} = 2 mA					
		8 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 4 mA					
			$ETHV_{CC} \geq 4.5$ V, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5$ V, I_{OL} = 4 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5$ V, I_{OL} = 18.5 mA	V_{SS}	-	0.4	V	*1
			$USBV_{CC} < 4.5$ V, I_{OL} = 10.5 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5$ V, I_{OL} = 3 mA					
			$V_{CC} \leq 4.5$ V, I_{OL} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, USBVCC0, USBVCC1, ETHVCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

1: $USBV_{CC}0$ and $USBV_{CC}1$ are described as $USBV_{CC}$.

12.4.12 CSIO (SPI) Timing

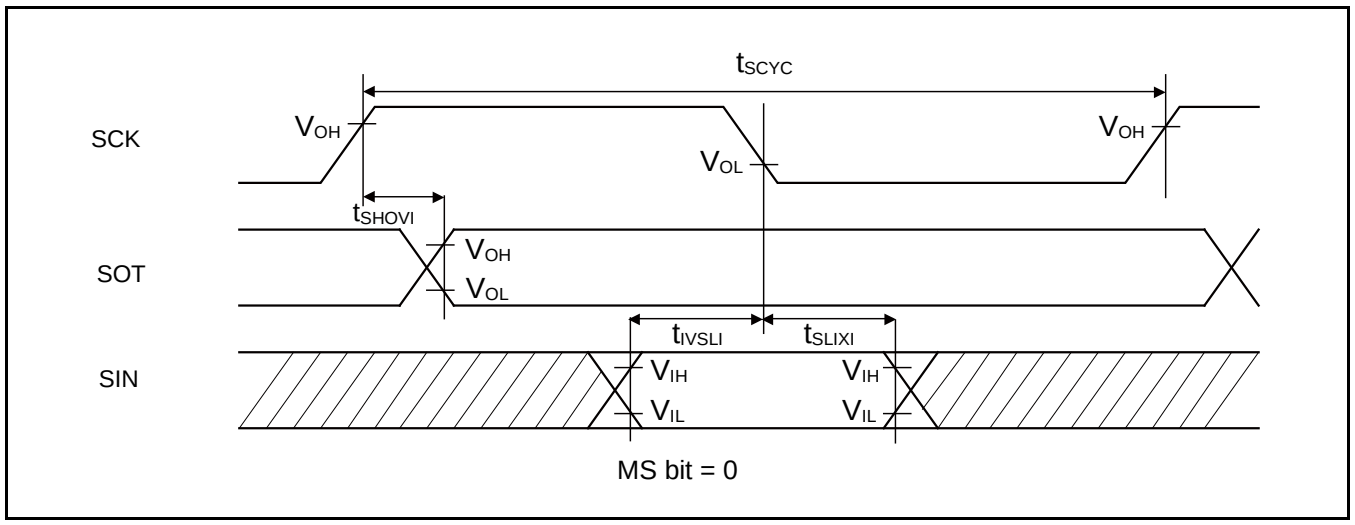
Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

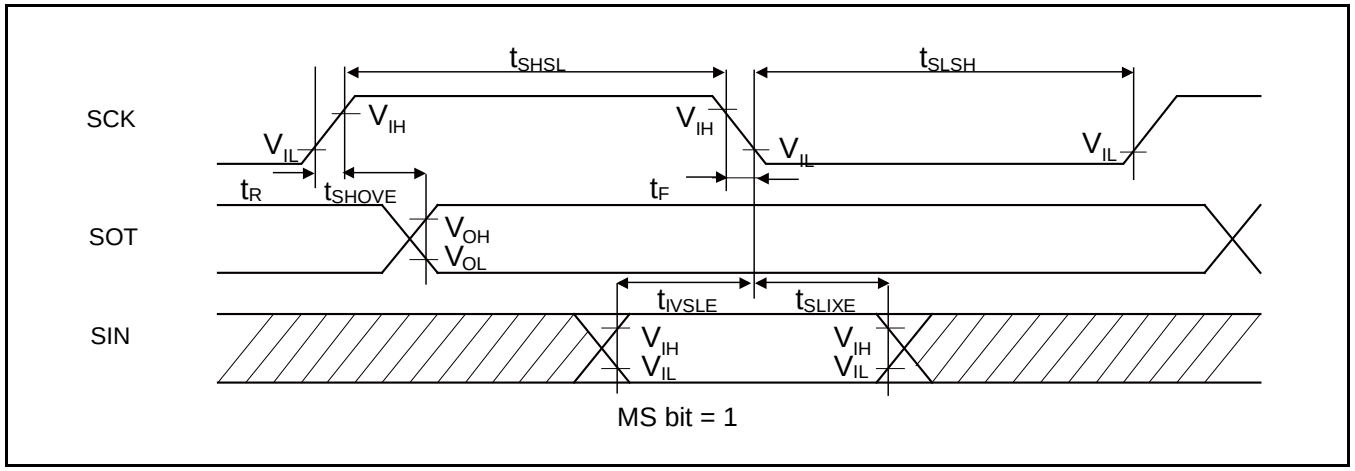
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	VCC < 4.5 V		VCC ≥ 4.5 V		Units
			Min	Max	Min	Max	
SCS ↑ →SCK ↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK ↓ →SCS ↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS ↑ →SCK ↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK ↓ →SCS ↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↑ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↓ →SOT delay time	t_{DEE}		0	-	0	-	ns

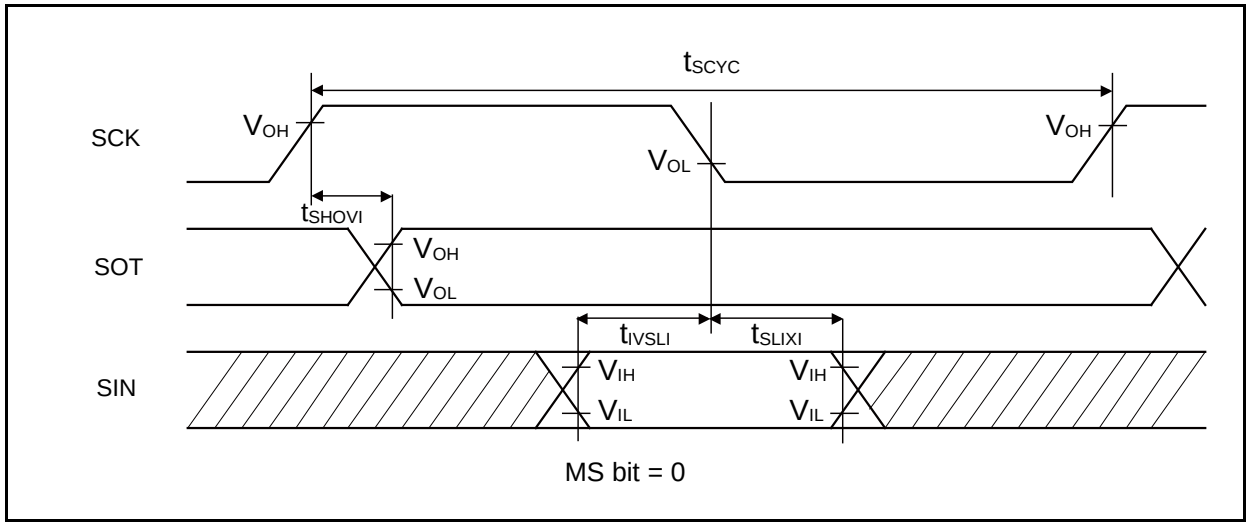
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

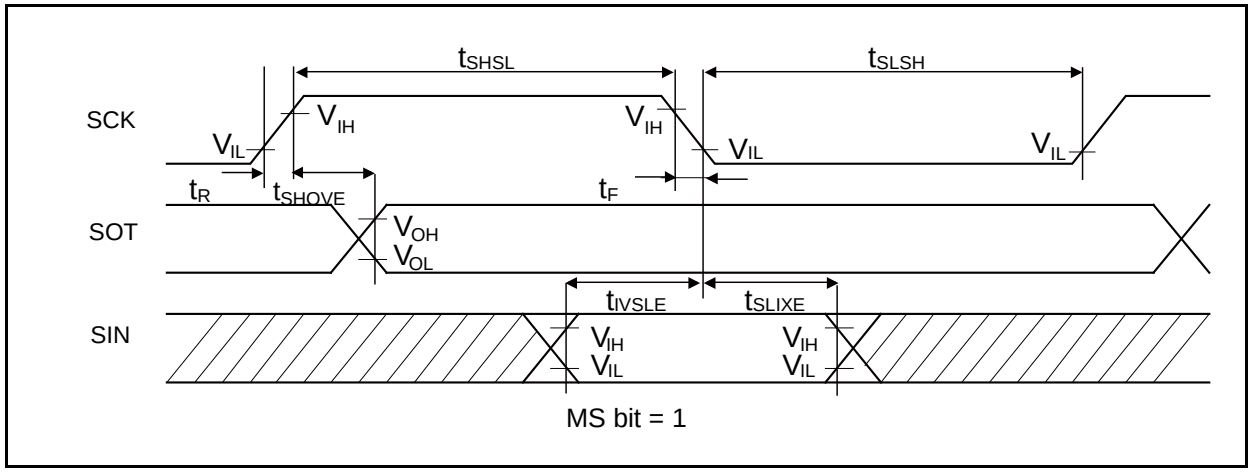
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

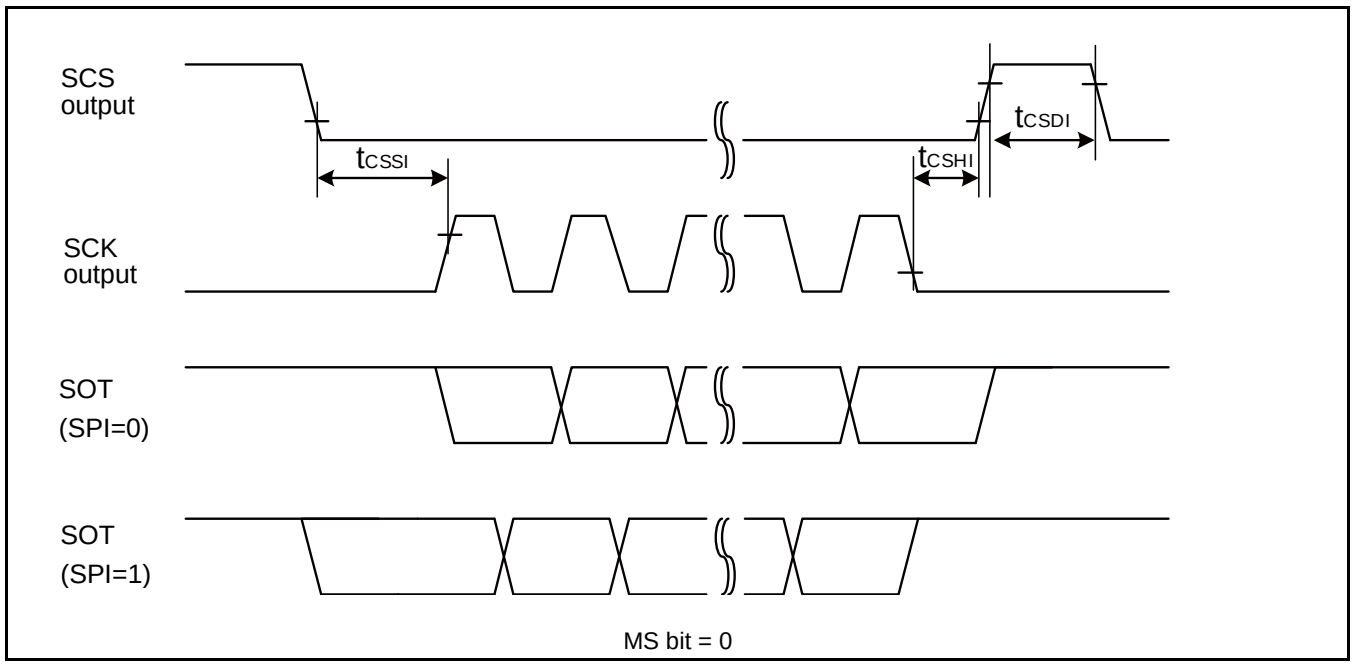
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



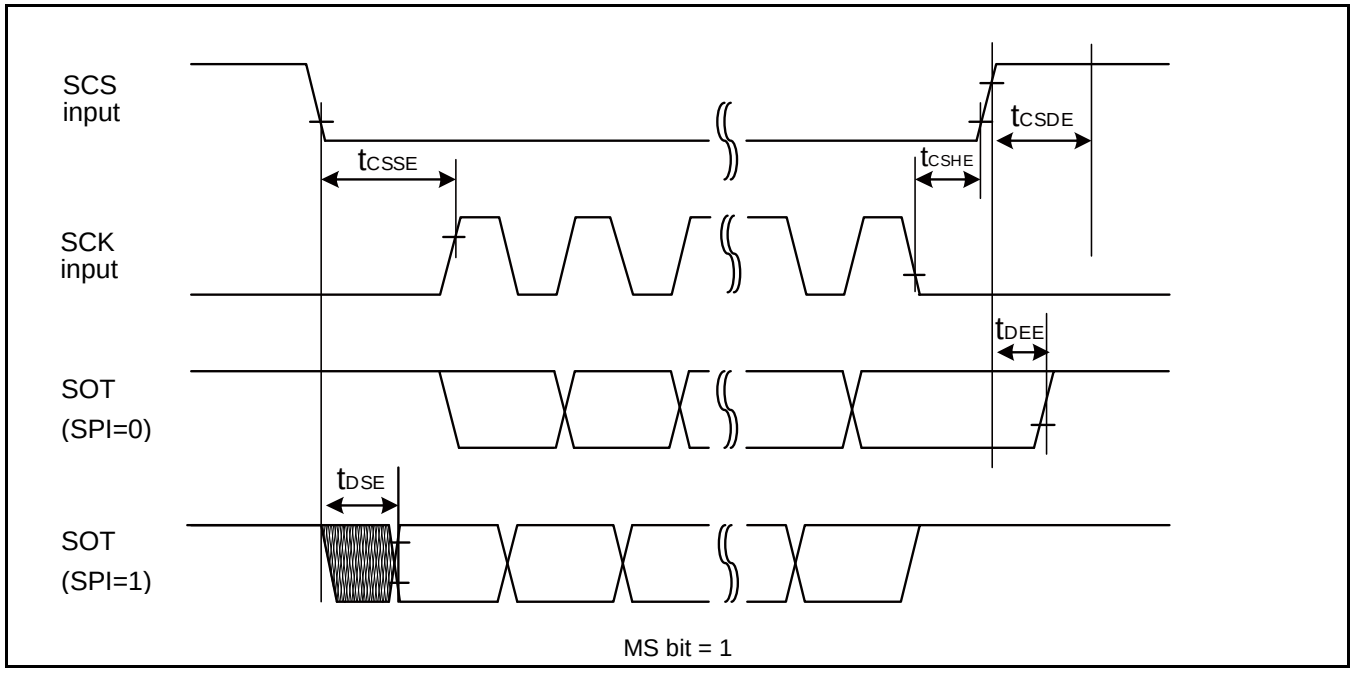
MS bit = 0



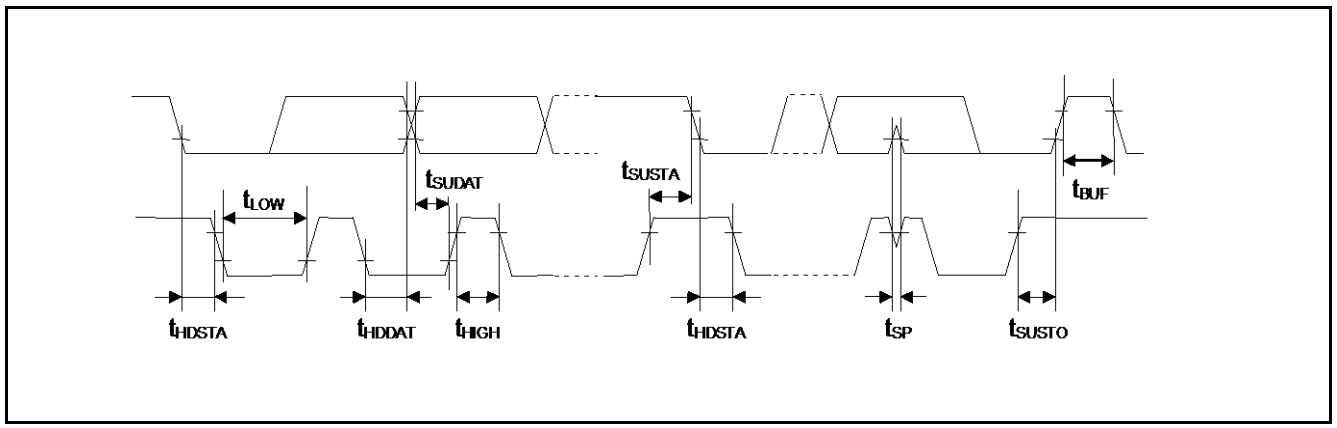
MS bit = 1



MS bit = 0



MS bit = 1


tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*

High-speed Mode

■ Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1 card)	0	45	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rise time	t_{TLH}	S_CLK		-	3	ns
Clock fall time	t_{THL}	S_CLK		-	3	ns

■ Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1 card)	6	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		2	-	ns

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output delay time during data transfer mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_L ≤ 40 pF (1 card)	0	14	ns
Output hold time	t_{OH}	S_CMD, S_DATA3: 0	C_L ≥ 15 pF (1 card)	2.5	-	ns
Total system capacitance for each line*	C_L	-	1 card	-	40	pF

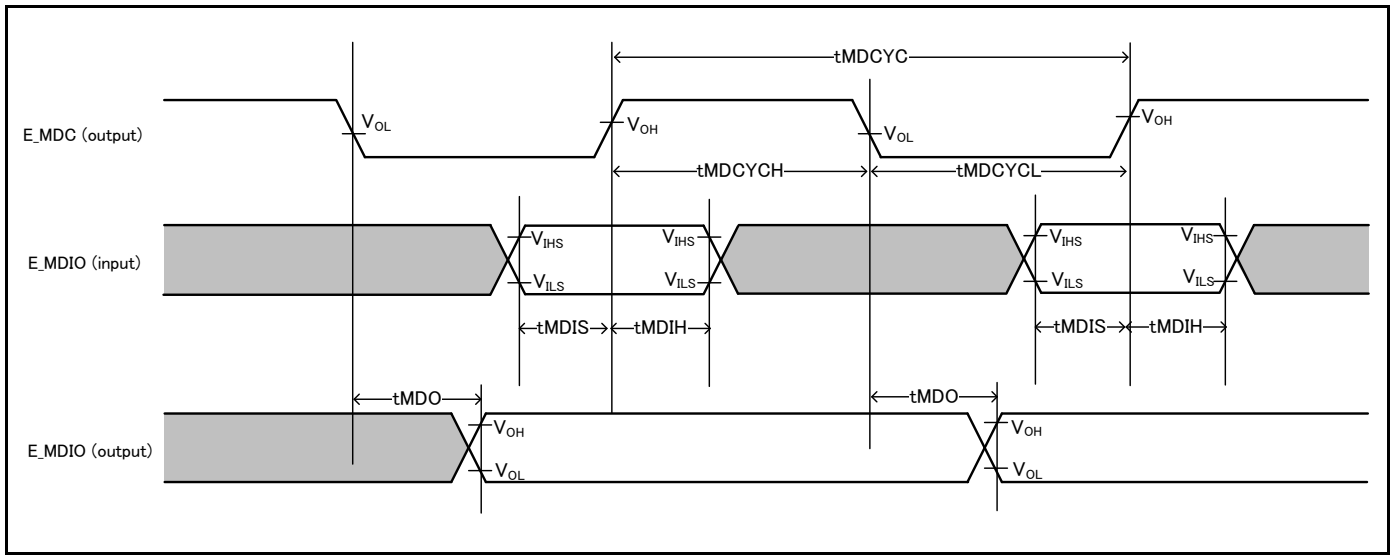
*: In order to satisfy severe timing, host shall drive only one card.

Management Interface

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Management clock cycle time*	t_{MDCYC}	E_MDC	-	400	-	ns
Management clock High pulse width duty cycle	t_{MDCYCH}	E_MDC	t_{MDCYCH}/t_{MDCYC}	35	65	%
Management clock Low pulse width duty cycle	t_{MDCYCL}	E_MDC	t_{MDCYCL}/t_{MDCYC}	35	65	%
MDC ↓ → MDIO Delay time	t_{MDO}	E_MDIO	-	-	60	ns
MDIO → MDC ↑ Setup time	t_{MDIS}	E_MDIO	-	20	-	ns
MDC ↑ → MDIO Hold time	t_{MDIH}	E_MDIO	-	0	-	ns

*: The clock time should be set to a value greater than the minimum value by setting the Ethernet-MAC setting register.



Document History

Document Title: S6E2G Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller
Document Number: 001-98708

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4861788	YOHO	07/27/2015	New Spec.
*A	4945035	HITK	11/20/2015	Changed status from Preliminary to Final. Updated 4 Pin Description: Added “Note” about TAP pins. Updated 12.2 Recommended Operating Conditions: Added the "Smoothing capacitor (C_S)”. Added the “Current Value” in “Maximum leak current at operating”. Updated 12.3.1 Current Rating: Updated Table 12-1 to Table 12-9: Added the “MAX” value. Updated Table 12-11: Updated 12.5 12-bit A/D Converter: Updated “Zero transition” and “Full-scale transition” value. Added “Total error”.
*B	5122844	BOO	03/29/2016	Removed full multiplexed signal names from the Pin Assignments drawing. Consolidated the G Series of Cypress MCUs into one data sheet. Added tables to differentiate parts in 2 Product Lineup and 3 Package-Dependent Features. Expanded 13 Ordering Information. Added hyperlinks to 6 Pin Descriptions. Added circuit type D to 7 I/O Circuit Type and pin state types S and T to 11 Pin Status in Each CPU State. Consolidated 10 Memory Map to two pages.
*C	5448447	YSKA	04/12/2017	Changed to new Cypress logo. Modified typo about the number(from 5 to 4) of powerts.(Page 11) Updated “12.4.8 Power-On Reset Timing”. Changed parameter from “Power Supply rise time(t_{VCCR}) [ms]” to “Power ramp rate(dV/dt) [mV/us]” and add some comments. (Page 107) Modified “12.4.12 CSIO(SPI) Timing”. Deleted “SPI=1, MS=0” in the titles and added MS=0,1 in the schematic (Page 128-135, 144-151) Deleted Baud rate spec for High-Speed Synchronous Serial in “12.4.12 CSIO(SPI) Timing”(Page 136-142) “Modified RTC description in “4. Product Features in Detail, Real-Time Clock(RTC)” Changed starting count value from 01 to 00. Deleted “second , or day of the week” in the Interrupt function (Page 9) Updated “14. Package dimensions”(Page 186-187) Change the name from “USB Function” to “USB Device” (Page 50) Deleted MPNs below from “13. Ordering Information” (Page 185) S6E2G26H0AGV20000, S6E2G26HHAGV20000, S6E2G26J0AGV20000, S6E2G26JHAGV20000, S6E2G28H0AGV20000, S6E2G28HHAGV20000, S6E2G28J0AGV20000, S6E2G28JHAGV20000, S6E2G36H0AGV20000, S6E2G36J0AGV20000, S6E2G38H0AGV20000, S6E2G38J0AGV20000, S6E2GH6H0AGV20000, S6E2GH6J0AGV20000, S6E2GH8H0AGV20000, S6E2GH8J0AGV20000, S6E2GK6H0AGV20000, S6E2GK6HHAGV20000, S6E2GK6J0AGV20000, S6E2GK6JHAGV20000, S6E2GK8H0AGV20000, S6E2GK8HHAGV20000, S6E2GK8J0AGV20000, S6E2GK8JHAGV20000, S6E2GM6H0AGV20000, S6E2GM6HHAGV20000, S6E2GM6J0AGV20000,

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