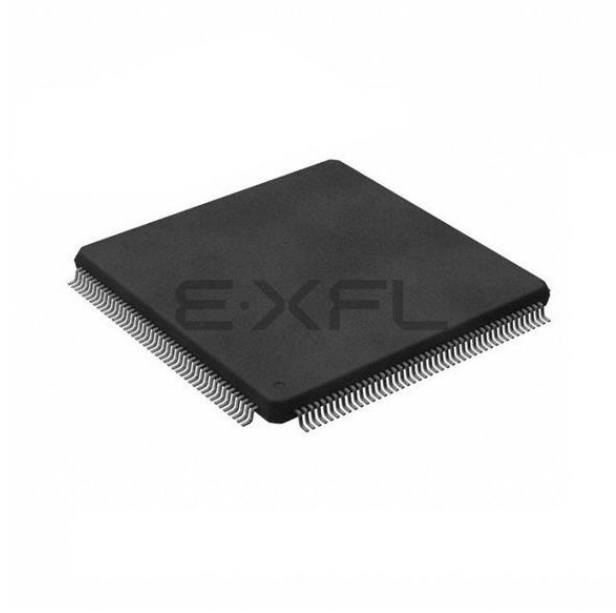

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gm6jhagv2000a

Ecosystem for Cypress FM4 MCUs

Cypress provides a wealth of data at www.cypress.com to help you to select the right MCU for your design, and to help you to quickly and effectively integrate the device into your design. Following is an abbreviated list for FM4 MCUs:

- Overview: Product Portfolio, Product Roadmap
- Product Selectors: FM4 MCUs
- Application notes: Cypress offers a large number of FM4 application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FM4 family of MCUs are:
  - AN204468 - FM4 I²S USB MP3 Player Application 32-Bit Microcontroller FM4 Family: This application note describes the general structure of the I²S USB MP3Player software example, its single modules in detail and how it is used.
  - AN204471 - FM4 S6E2CC Series External Memory Programmer: This document describes use of the MCU Universal Programmer as an off-line programmer for Quad SPI flash memory programming on the S6E2CC Series SK.
  - AN203277 - FM 32-Bit Microcontroller Family Hardware Design Considerations: This application note reviews several topics for designing a hardware system around FM0+, FM3, and FM4 family MCUs. Subjects include power system, reset, crystal, and other pin connections, and programming and debugging interfaces.
  - AN202488 - FM4 MB9BF56x and S6E2HG Series MCU - Servo Motor Speed Control: This document covers servo motor speed control solution on FM4 MCU - MB9BF56x and S6E2HG.
  - AN99235 - FM4 S6E2HG Series MCU - 16-Bit PWM Using a Base Timer: Cypress FM4 Family of 32-bit ARM® Cortex®-M4 Microcontrollers FM4 S6E2H Series Motor Control ARM® Cortex®-M4 MCU
  - AN202487 - Differences Among FM0+, FM3, and FM4 32-Bit Microcontrollers: Highlights the peripheral differences in Cypress's FM family MCUs. It provides dedicated sections for each peripheral and contains lists, tables, and descriptions of peripheral feature and register differences.
  - AN204438 - How to Setup Flash Security for FM0+, FM3 and FM4 Families: This application note describes how to setup the Flash Security for FM0+, FM**3**, and FM4 devices
- Development kits:
  - FM4-U120-9B560 - ARM® Cortex®-M4 MCU Starter Kit with USB and CMSIS-DAP
  - FM4-216-ETHERNET ARM® Cortex®-M4 MCU Development Kit with Ethernet, CAN and USB Host
  - FM4-176L-S6E2CC-ETH - ARM® Cortex®-M4 MCU Starter Kit with Ethernet and USB Host
  - FM4-176L-S6E2GM - ARM® Cortex®-M4 MCU Pioneer Kit with Ethernet and USB Host
- Peripheral Manuals

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detector reset
  - Clock supervisor reset

Clock Supervisor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include two-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, the low-voltage detector function generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Crypto Assist Function

These features are enabled for the crypto assist function.

The dedicated middleware is necessary for this calculator operation.

- PKA (Public Key Accelerator)
  - PKA（Public Key Accelerator）is modular exponentiation calculation accelerator used of RSA Public Key crypto and so on.
  - Available bit length: Up to 2048-bit
- AES calculator
  - AES (Advanced Encryption Standard) calculator is a AES common key crypto accelerator which is compliant with FIPS (Federal Information Processing Standard Publication)197.
  - Available key length: 128/192/256-bit
  - CBC mode and ECB mode support
- External Bus Data Scramble
  - It enables to scramble input/output data of External Bus Interface.

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

Unique value of the device (41-bit) is set.

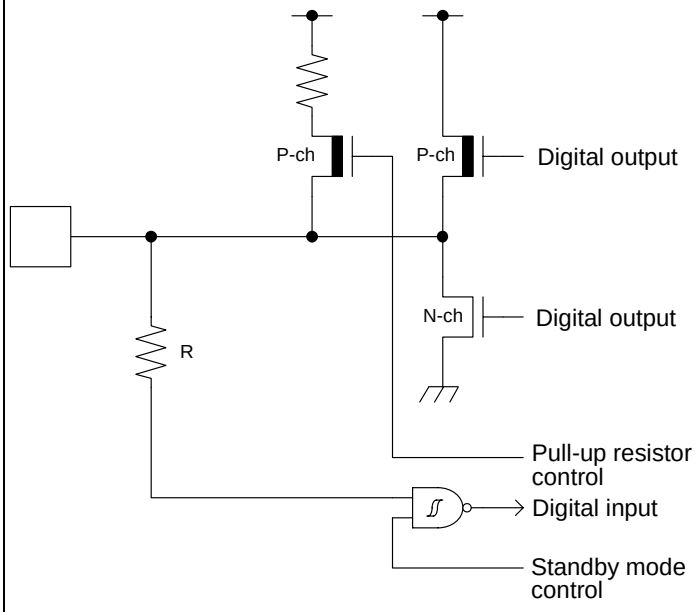
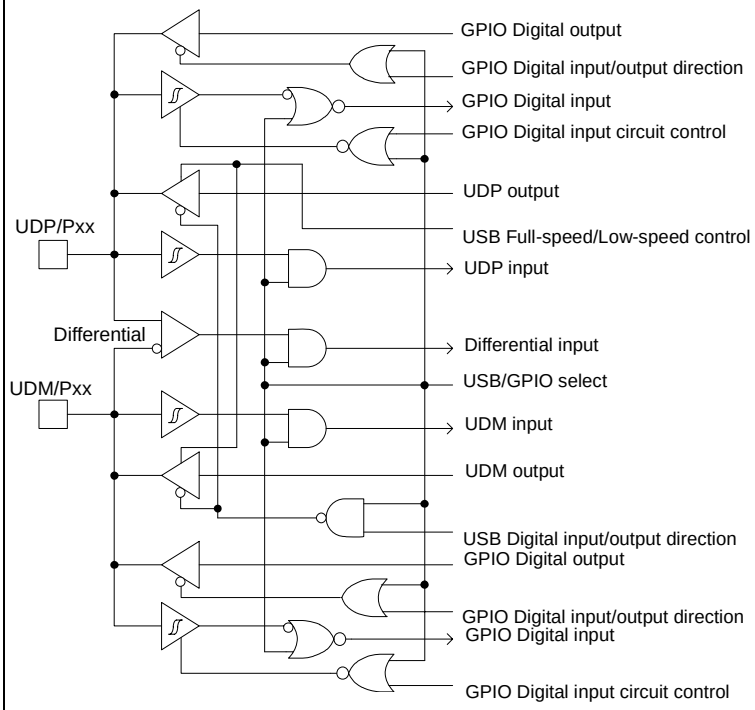
Power Supply

- Four power supplies
  - Wide range voltage: VCC = 2.7 V to 5.5 V
  - Power supply for USB ch 0 I/O: USBVCC0
= 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for USB ch 1 I/O: USBVCC1
= 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for Ethernet-MAC I/O: ETHVCC
= 3.0 V to 5.5 V (when Ethernet is used.)

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
28	23	P34 IC03_0 INT00_1 S_CLK_0	L	K
29	24	VCC	-	-
30	25	VSS	-	-
31	26	P35 IC02_0 INT01_1 S_CMD_0	L	K
32	27	P36 IC01_0 INT02_1 S_DATA3_0	L	K
33	28	P37 IC00_0 INT03_1 S_DATA2_0	L	K
34	29	P38 ADTG_2 DTTI0X_0 S_WP_0	E	I
35	30	P39 RTO00_0 (PPG00_0) TIOA0_1 AIN1_0 INT16_1 S_CD_0 MAD24_0	G	K
36	31	P3A RTO01_0 (PPG01_0) TIOA1_1 BIN1_0 INT17_1 MAD23_0	G	K
37	32	P3B RTO02_0 (PPG02_0) TIOA2_1 ZIN1_0 INT18_1 MAD22_0	G	K

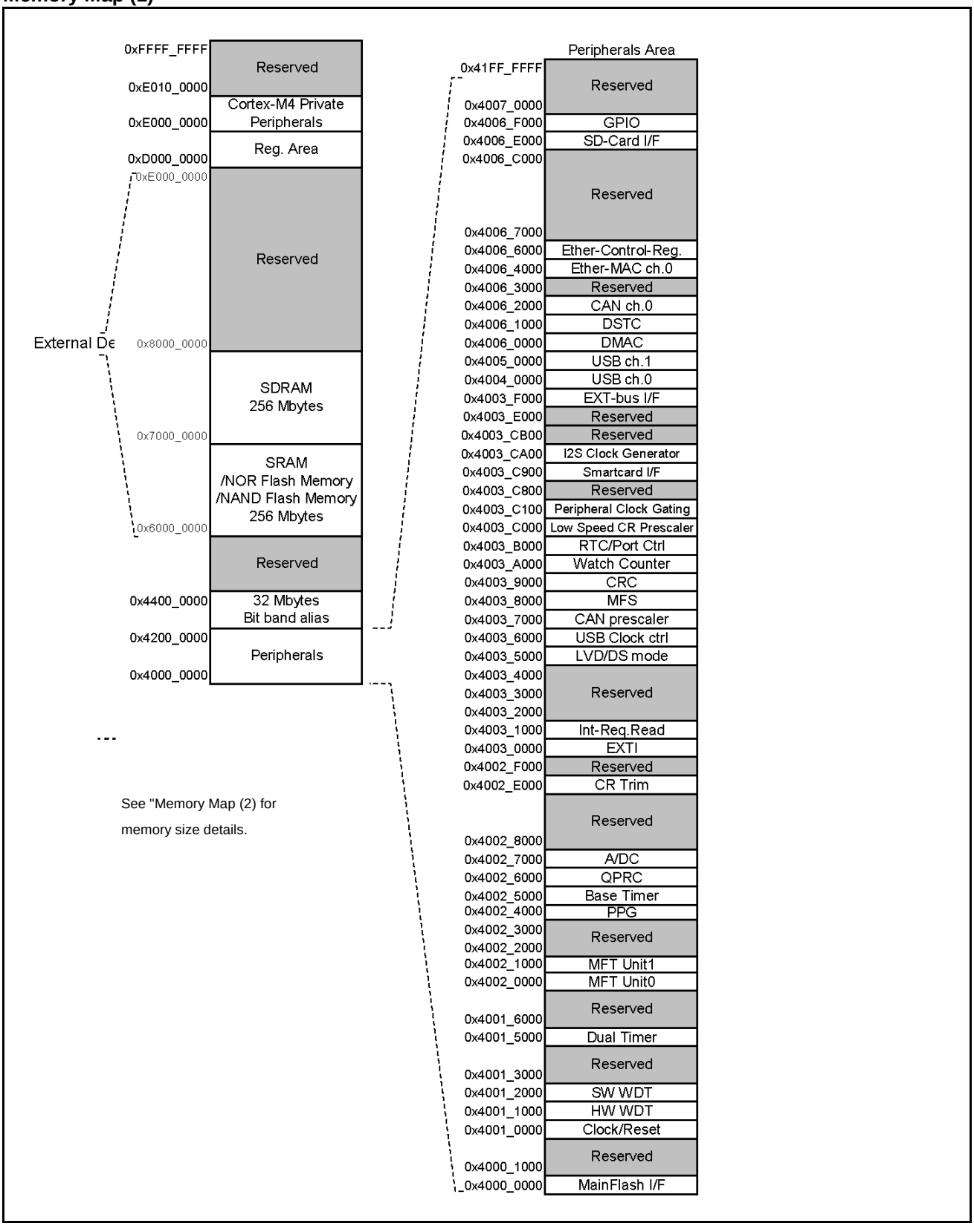
Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External interrupt	INT14_0	External interrupt request 14 input pin	160	130
	INT14_1		141	-
	INT15_0	External interrupt request 15 input pin	161	131
	INT15_1		142	-
	INT16_0	External interrupt request 16 input pin	20	17
	INT16_1		35	30
	INT17_0	External interrupt request 17 input pin	21	18
	INT17_1		36	31
	INT18_0	External interrupt request 18 input pin	22	19
	INT18_1		37	32
	INT19_0	External interrupt request 19 input pin	26	21
	INT19_1		38	33
	INT20_0	External interrupt request 20 input pin	70	60
	INT20_1		82	-
	INT21_0	External interrupt request 21 input pin	73	63
	INT21_1		83	-
	INT22_0	External interrupt request 22 input pin	76	66
	INT22_1		58	-
	INT23_0	External interrupt request 23 input pin	46	38
	INT23_1		59	-
	INT24_0	External interrupt request 24 input pin	121	97
	INT24_1		107	87
	INT25_0	External interrupt request 25 input pin	123	99
	INT25_1		97	81
	INT26_0	External interrupt request 26 input pin	126	102
	INT26_1		116	92
	INT27_0	External interrupt request 27 input pin	127	103
	INT27_1		117	93
	INT28_0	External interrupt request 28 input pin	158	128
	INT28_1		167	-
	INT29_0	External interrupt request 29 input pin	166	136
	INT29_1		168	-
	INT30_0	External interrupt request 30 input pin	169	137
	INT30_1		163	133
	INT31_0	External interrupt request 31 input pin	172	140
	INT31_1		164	134
	NMIX	Non-maskable interrupt input pin	128	104

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P30	General-purpose I/O port 3	24	-
	P31		25	-
	P32		26	21
	P33		27	22
	P34		28	23
	P35		31	26
	P36		32	27
	P37		33	28
	P38		34	29
	P39		35	30
	P3A		36	31
	P3B		37	32
	P3C		38	33
	P3D		39	34
	P3E		40	35
	P40	General-purpose I/O port 4	46	38
	P41		47	39
	P42		48	40
	P43		49	41
	P44		50	42
	P45		51	43
	P46		55	47
	P47		56	48
	P48		60	50
	P49		61	51
	P4A		62	52
	P4B		63	53
	P4C		64	54
	P4D		65	55
	P4E		66	56
	P50	General-purpose I/O port 5	10	-
	P51		11	-
	P52		12	-
	P5D		41	-
	P5E		42	-
	P5F		43	-
	P60	General-purpose I/O port 6	172	140
	P61		171	139
	P62		170	138
	P63		169	137
	P64		168	-
	P65		167	-
	P6E		166	136

Type	Circuit	Remarks
G		・ CMOS level output ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -12 mA, I_{OL} = 12 mA ・ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
H		It is possible to select either USB I/O or GPIO function. When the USB I/O is selected: ・ Full-speed, low-speed control When the GPIO is selected: ・ CMOS level output ・ CMOS level hysteresis input ・ Standby mode control ・ I_{OH} = -20.5 mA, I_{OL} = 18.5 mA

10. Memory Map

Memory Map (1)



11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

- INITX = 0

  This is the period when the INITX pin is at the L level.

- INITX = 1

  This is the period when the INITX pin is at the H level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
W	Ethernet input/output selected*4	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected									
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
S	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Sub crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
T	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enabled	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops*5, it will be Hi-Z/ Internal input fixed at 0					

Ethernet-MAC Pins

Pin Name	Ethernet-MAC Function	Except For Ethernet-MAC Function	Power Supply Type
P6E/ADTG_5/SCK4_1/INT29_0/E_PPS	E_PPS *	P6E/ADTG_5/SCK4_1/INT29_0	V_{CC}
PC0/E_RXER	E_RXER	PC0	$ETHV_{CC}$
PC1/TIOB6_0/E_RX03	E_RX03	PC1/TIOB6_0	
PC2/TIOA6_0/E_RX02	E_RX02	PC2/TIOA6_0	
PC3/TIOB7_0/E_RX01	E_RX01	PC3/TIOB7_0	
PC4/TIOA7_0/E_RX00	E_RX00	PC4/TIOA7_0	
PC5/TIOB14_0/E_RXDV	E_RXDV	PC5/TIOB14_0	
PC6/TIOA14_0/E_MDIO	E_MDIO	PC6/TIOA14_0	
PC7/INT13_0/E_MDC/CROUT_1	E_MDC	PC7/INT13_0/CROUT_1	
PC8/E_RXCK_REFCK	E_RXCK_REFCK	PC8	
PC9/TIOB15_0/E_COL	E_COL	PC9/TIOB15_0	
PCA/TIOA15_0/E_CRS	E_CRS	PCA/TIOA15_0	
PCB/INT28_0/E_COUT	E_COUT	PCB/INT28_0	
PCC/E_TCK	E_TCK	PCC	
PCD/SOT4_1/INT14_0/E_TXER	E_TXER	PCD/SOT4_1/INT14_0	
PCE/SIN4_1/INT15_0/E_TX03	E_TX03	PCE/SIN4_1/INT15_0	
PCF/RTS4_1/INT12_0/E_TX02	E_TX02	PCF/RTS4_1/INT12_0	
PD0/INT30_1/E_TX01	E_TX01	PD0/INT30_1	
PD1/INT31_1/E_TX00	E_TX00	PD1/INT31_1	
PD2/CTS4_1/E_TXEN	E_TXEN	PD2/CTS4_1	

*: It is used to confirm the PTP counter cycle in Ethernet-MAC by waveforms.

Table 12-5 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation*5 (PLL)	180 MHz	58	116	mA	*3 When all peripheral clocks are on
				160 MHz	52	110	mA	
				144 MHz	48	106	mA	
				120 MHz	40	98	mA	
				100 MHz	35	93	mA	
				80 MHz	28	86	mA	
				60 MHz	22	80	mA	
				40 MHz	16	74	mA	
				20 MHz	9.7	67	mA	
				8 MHz	6.2	64	mA	
				4 MHz	5.0	63	mA	
				180 MHz	30	88	mA	*3 When all peripheral clocks are off
				160 MHz	27	85	mA	
				144 MHz	25	83	mA	
				120 MHz	21	79	mA	
				100 MHz	18	76	mA	
				80 MHz	15	73	mA	
				60 MHz	12	70	mA	
				40 MHz	9.3	67	mA	
				20 MHz	6.2	64	mA	
				8 MHz	4.5	62	mA	
				4 MHz	4.0	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-6 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation*5 (PLL)	72 MHz	32	90	mA	*3 When all peripheral clocks are on
				60 MHz	27	85	mA	
				48 MHz	23	81	mA	
				36 MHz	18	76	mA	
				24 MHz	13	71	mA	
				12 MHz	8.5	66	mA	
				8 MHz	6.9	64	mA	
				4 MHz	5.3	63	mA	
				72 MHz	15	73	mA	*3 When all peripheral clocks are off
				60 MHz	13	71	mA	
				48 MHz	11	69	mA	
				36 MHz	9.3	67	mA	
				24 MHz	7.3	65	mA	
				12 MHz	5.4	63	mA	
				8 MHz	4.7	62	mA	
				4 MHz	4.1	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

12.4 AC Characteristics

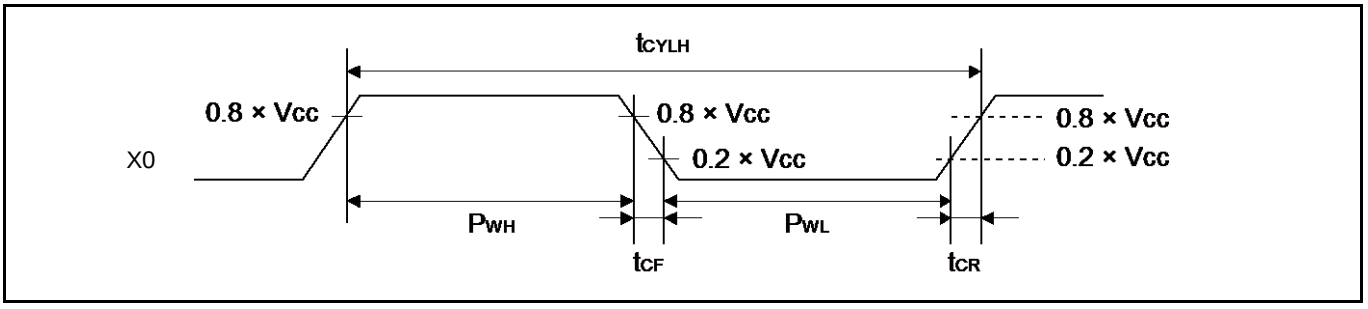
12.4.1 Main Clock Input Characteristics

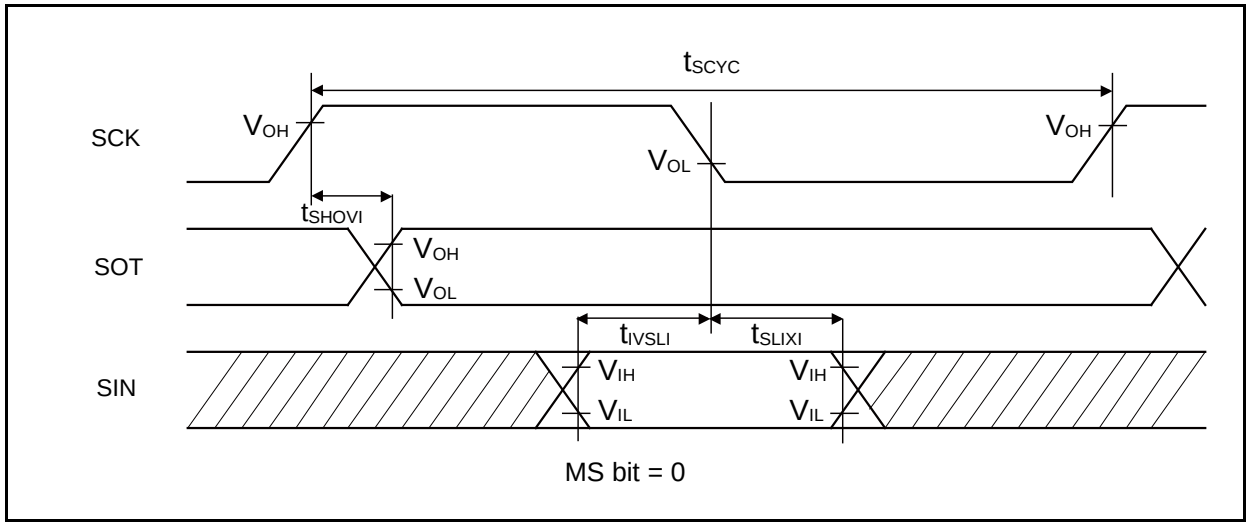
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥4.5 V	4	48	MHz	When crystal oscillator is connected
			V_{CC} < 4.5 V	4	20		
			V_{CC} ≥4.5 V	4	48	MHz	When using external clock
			V_{CC} < 4.5 V	4	20		
Input clock cycle	t_{CYLH}		V_{CC} ≥4.5 V	20.83	250	ns	When using external clock
			V_{CC} < 4.5 V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock *1 frequency	f_{CC}	-	-	-	180	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	90	MHz	APB0bus clock *2
	f_{CP1}	-	-	-	180	MHz	APB1bus clock *2
	f_{CP2}	-	-	-	90	MHz	APB2bus clock *2
Internal operating clock *1 cycle time	t_{CYCC}	-	-	5.56	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	11.1	-	ns	APB0bus clock *2
	t_{CYCP1}	-	-	5.56	-	ns	APB1bus clock *2
	t_{CYCP2}	-	-	11.1	-	ns	APB2bus clock *2

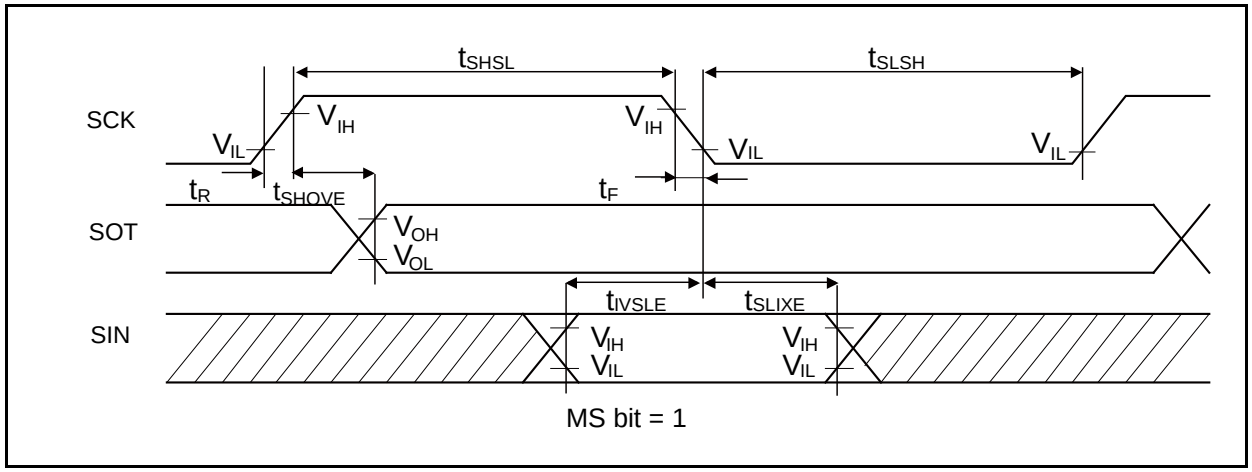
1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

2: For more about each APB bus to which each peripheral is connected, see 1. S6E2G Series Block Diagram in this data sheet.

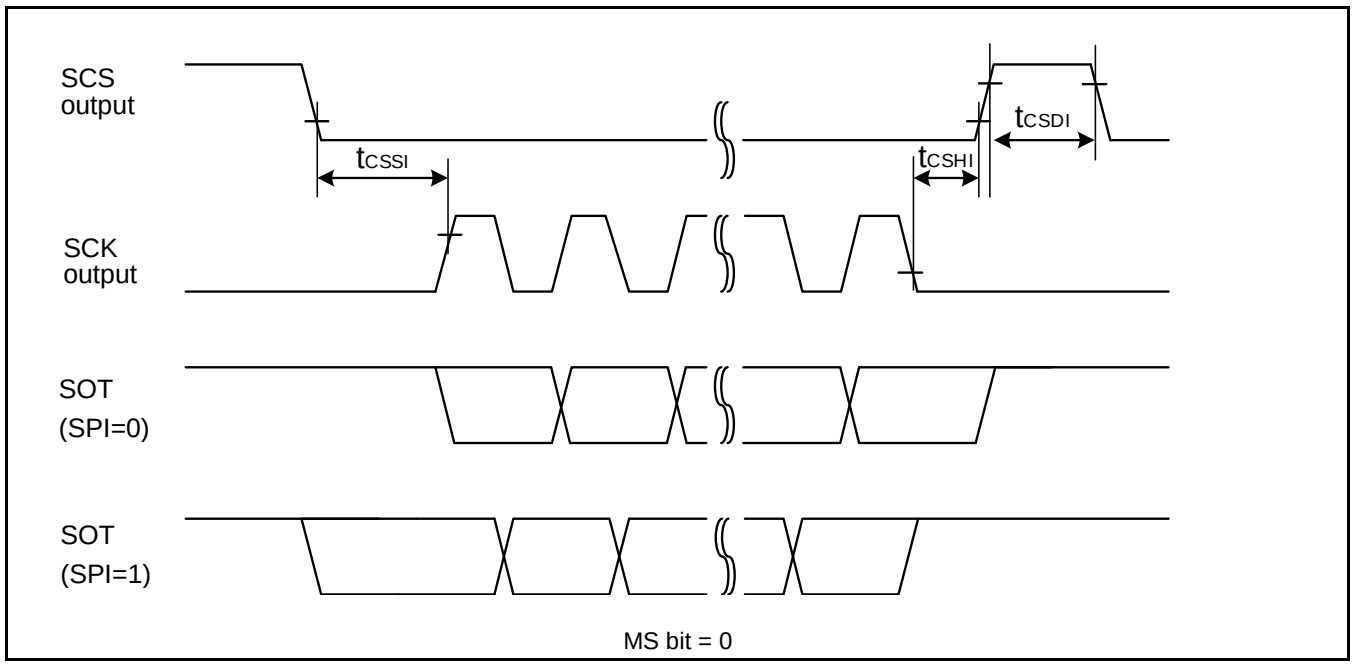




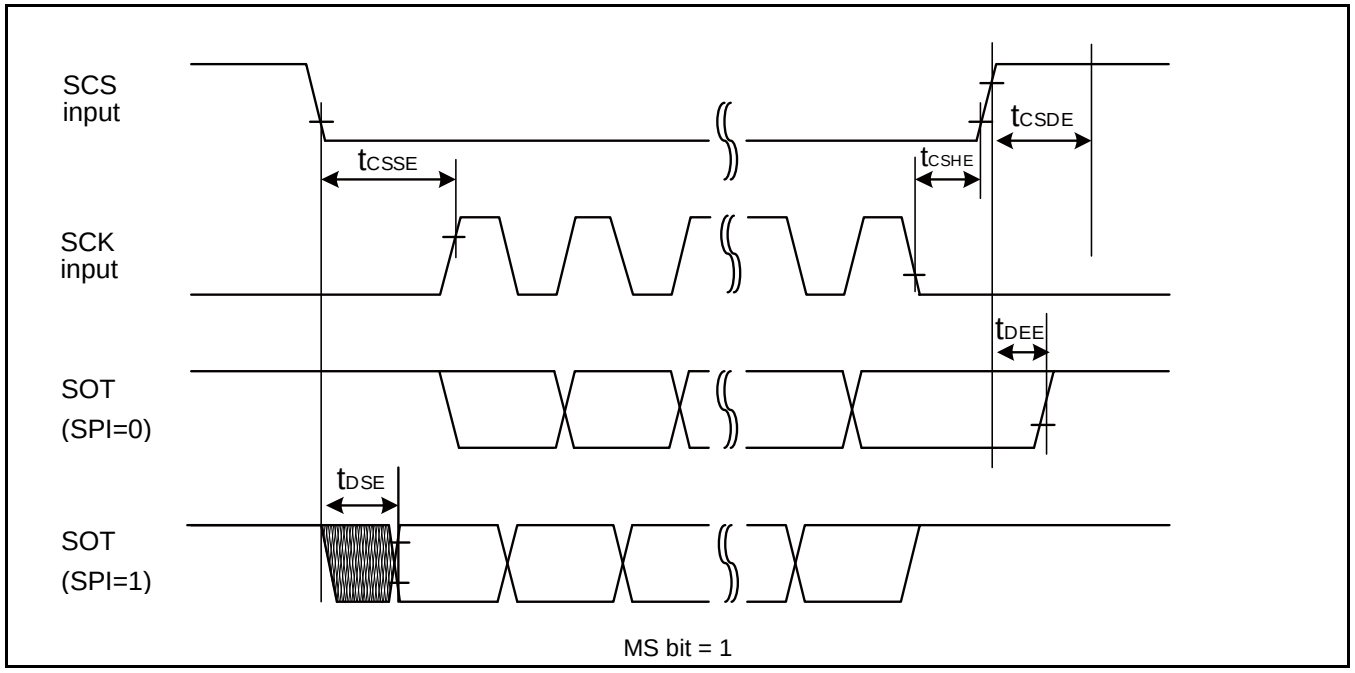
MS bit = 0



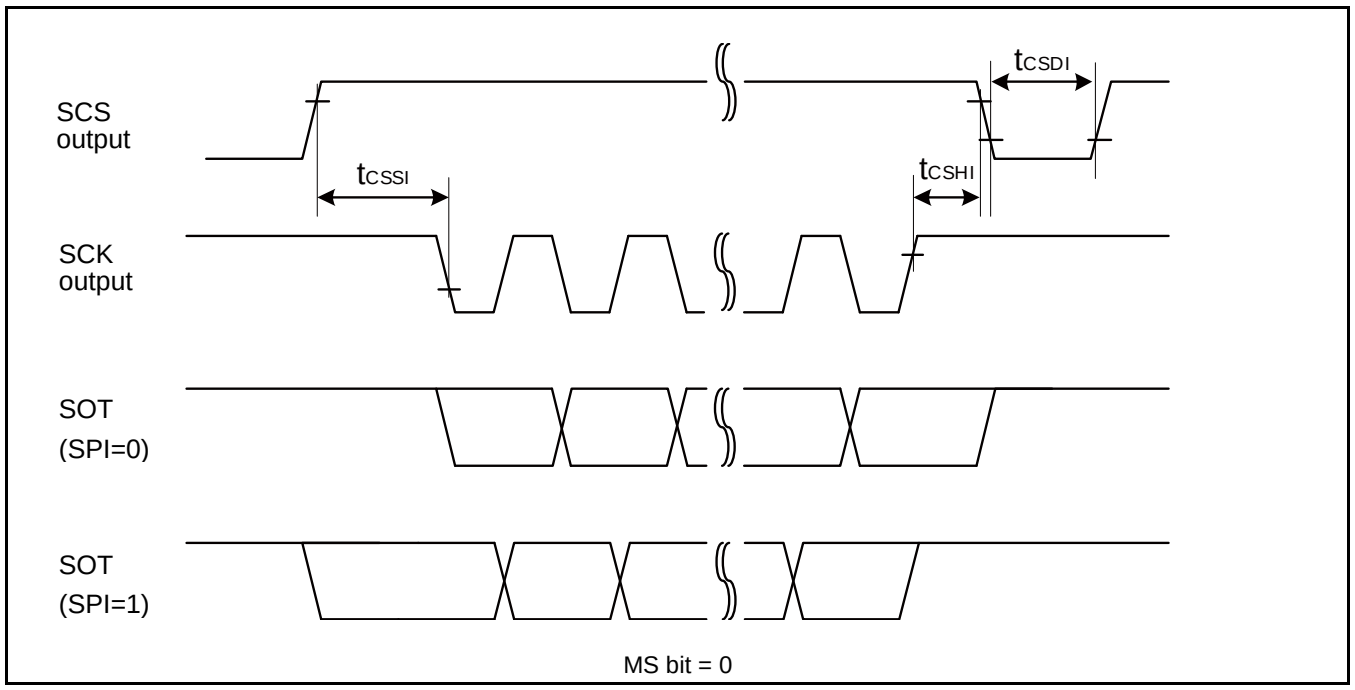
MS bit = 1



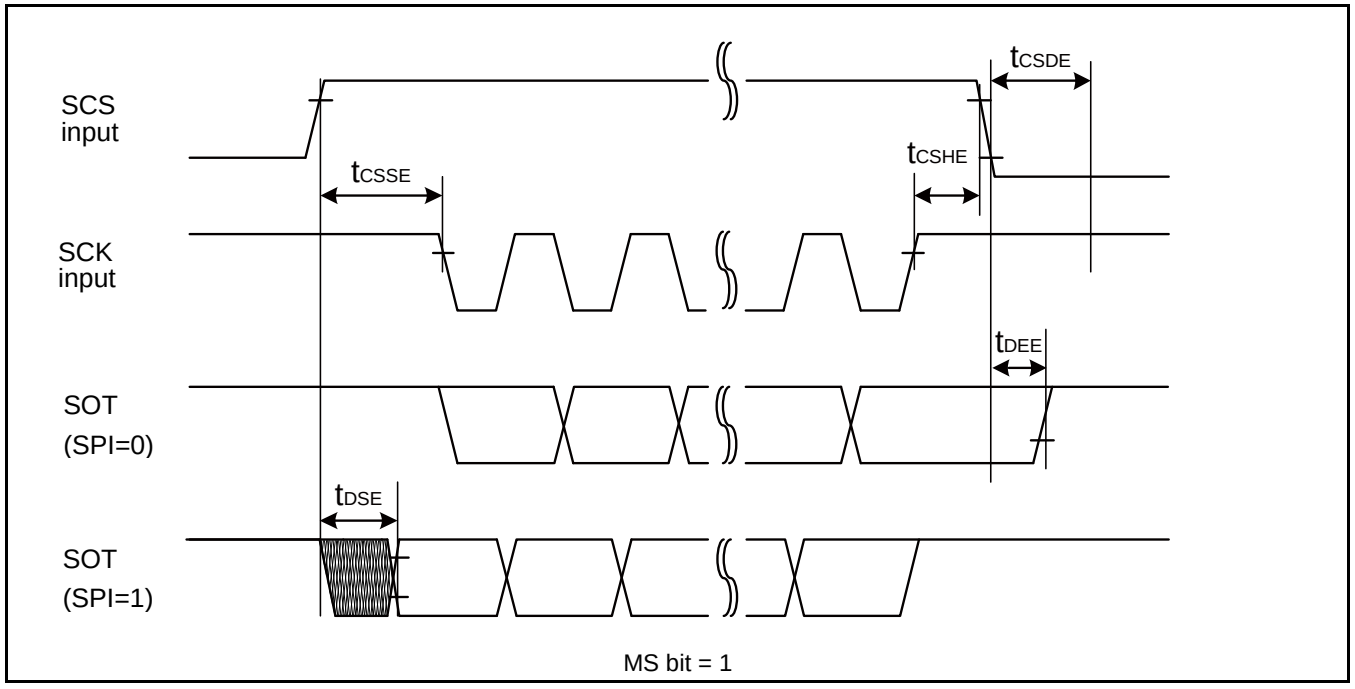
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

Fast mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock L width	t_{LOW}		0.5	-	µs	
SCL clock H width	t_{HIGH}		0.26	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		0.26	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between Stop condition and START condition	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}*4	-	ns	

1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

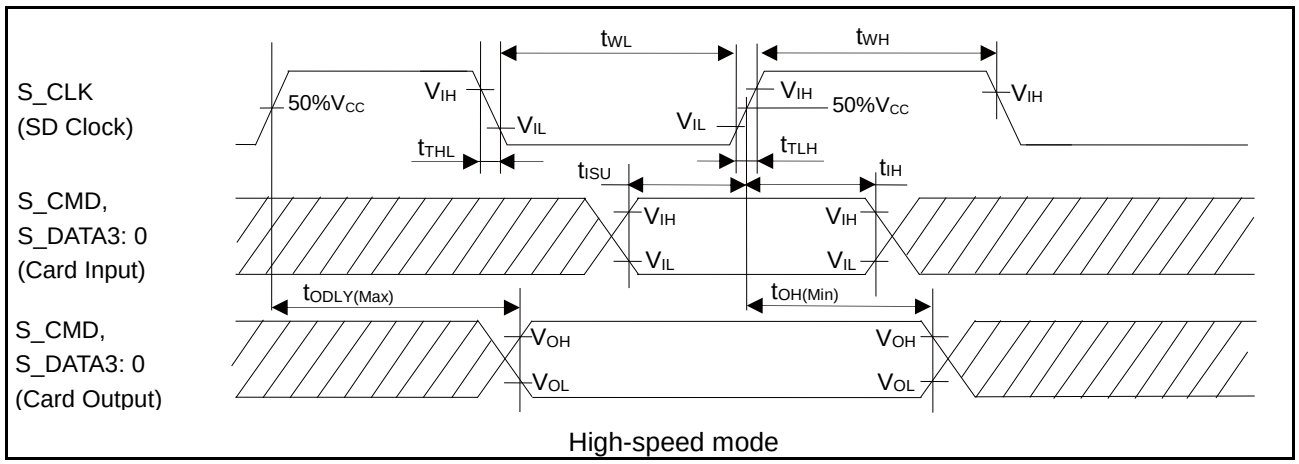
2: The maximum t_{HDDAT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

3: The Fast mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns."

4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I^2C is connected, see 1.S6E2G Series Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register.
See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.



High-speed mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*

12.4.17 ETM/ HTM Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[15: 0]	V_{CC} ≥ 4.5 V	2	9	ns	
			V_{CC} <4.5 V	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	V_{CC} ≥ 4.5 V		50	MHz	
			V_{CC} <4.5 V		32	MHz	
TRACECLK clock cycle	t_{TRACE}		V_{CC} ≥ 4.5 V	20	-	ns	
			V_{CC} <4.5 V	31.25	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*

12.6 USB Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, $USBV_{CC}0$ = $USBV_{CC}1$ = 3.0V to 3.6V, V_{SS} = AV_{SS} = 0V)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0/ UDM0, UDP1/ UDM1	-	2.0	$USBV_{CC}$ + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rise time	t_{FR}		Full-Speed	4	20	ns	*5
	Fall time	t_{FF}		Full-Speed	4	20	ns	*5
	Rise/fall time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rise time	t_{LR}		Low-Speed	75	300	ns	*7
	Fall time	t_{LF}		Low-Speed	75	300	ns	*7
	Rise/fall time matching	t_{LRFM}		Low-Speed	80	125	%	*7

1: The switching threshold voltage of the single-end-receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).

There is some hysteresis applied to lower noise sensitivity.

2: Use differential-receiver to receive USB differential data signal. Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

Above voltage range is the common mode input voltage range.