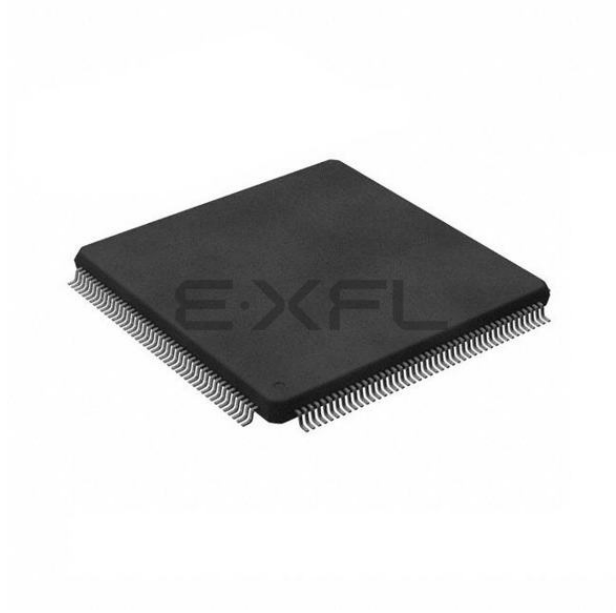

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2gm8jhagv2000a

Signal Descriptions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
A/D converter	ADTG_0	A/D converter external trigger input pin	19	16
	ADTG_1		23	20
	ADTG_2		34	29
	ADTG_3		169	137
	ADTG_4		127	103
	ADTG_5		166	136
	ADTG_6		122	98
	ADTG_7		67	57
	ADTG_8		68	58
	AN00	A/D converter analog input pin. ANxx describes A/D converter ch xx.	94	78
	AN01		95	79
	AN02		96	80
	AN03		97	81
	AN04		98	82
	AN05		99	83
	AN06		100	84
	AN07		101	85
	AN08		106	86
	AN09		107	87
	AN10		108	88
	AN11		109	89
	AN12		114	90
	AN13		115	91
	AN14		116	92
	AN15		117	93
	AN16		102	-
	AN17		103	-
	AN18		104	-
	AN19		105	-
	AN20		110	-
	AN21		111	-
	AN22		112	-
	AN23		113	-
	AN24		118	94
	AN25		119	95
	AN26		120	96
	AN27		121	97
	AN28		123	99
	AN29		124	100
	AN30		125	101
	AN31		126	102

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External bus	MADATA00_0	External bus interface data bus (address/data multiplex bus)	2	2
	MADATA01_0		3	3
	MADATA02_0		4	4
	MADATA03_0		5	5
	MADATA04_0		6	6
	MADATA05_0		7	7
	MADATA06_0		8	8
	MADATA07_0		9	9
	MADATA08_0		13	10
	MADATA09_0		14	11
	MADATA10_0		15	12
	MADATA11_0		16	13
	MADATA12_0		17	14
	MADATA13_0		18	15
	MADATA14_0		19	16
	MADATA15_0		20	17
	MDQM0_0	External bus interface byte mask signal output pin	21	18
	MDQM1_0		22	19
	MALE_0	External bus interface address latch enable output signal for multiplex	171	139
	MRDY_0	External bus interface external RDY input signal	68	58
	MCLKOUT_0	External bus interface external clock output pin	23	20
	MNALE_0	External bus interface ALE signal to control NAND flash output pin	97	81
	MNCLE_0	External bus interface CLE signal to control NAND flash output pin	96	80
	MNREX_0	External bus interface read enable signal to control NAND flash	94	78
	MNWEX_0	External bus interface write enable signal to control NAND flash	95	79
	MOEX_0	External bus interface read enable signal for SRAM	169	137
	MWEX_0	External bus interface write enable signal for SRAM	170	138
	MSDCLK_0	SDRAM interface SDRAM clock output pin	65	55
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	64	54
	MRASX_0	SDRAM interface SDRAM row active strobe pin	60	50
	MCASX_0	SDRAM interface SDRAM column active strobe pin	61	51
	MSDWEX_0	SDRAM interface SDRAM write enable pin	62	52

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 2	SIN2_0	Multi-function serial interface ch 2 input pin	106	86
	SIN2_1		38	33
	SOT2_0 (SDA2_0)	Multi-function serial interface ch 2 output pin This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I²C (operation mode 4).	107	87
	SOT2_1 (SDA2_1)		39	34
	SCK2_0 (SCL2_0)	Multi-function serial interface ch 2 clock I/O pin This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I²C (operation mode 4).	108	88
	SCK2_1 (SCL2_1)		40	35
Multi-Function Serial 3	SIN3_0	Multi-function serial interface ch 3 input pin	20	17
	SIN3_1		81	-
	SOT3_0 (SDA3_0)	Multi-function serial interface ch 3 output pin This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I²C (operation mode 4).	19	16
	SOT3_1 (SDA3_1)		82	-
	SCK3_0 (SCL3_0)	Multi-function serial interface ch 3 clock I/O pin This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I²C (operation mode 4).	18	15
	SCK3_1 (SCL3_1)		83	-
Multi-Function Serial 4	SIN4_0	Multi-function serial interface ch 4 input pin	172	140
	SIN4_1		161	131
	SOT4_0 (SDA4_0)	Multi-function serial interface ch 4 output pin This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I²C (operation mode 4).	171	139
	SOT4_1 (SDA4_1)		160	130
	SCK4_0 (SCL4_0)	Multi-function serial interface ch 4 clock I/O pin This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I²C (operation mode 4).	170	138
	SCK4_1 (SCL4_1)		166	136
	CTS4_0	Multi-function serial interface ch 4 CTS input pin	168	-
	CTS4_1		165	135
	RTS4_0	Multi-function serial interface ch 4 RTS output pin	169	137
	RTS4_1		162	132

List of Pin Behavior by Mode State

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Main crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enabled	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops*[1], it will be Hi-Z/ Internal input fixed at 0					
C	INITX input pin	Pull-up/ input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ input enabled	GPIO selected	Hi-Z/ input enabled	GPIO selected

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/ internal input fixed at 0			GPIO selected
	GPIO selected									
G	JTAG selected	Hi-Z	Pull-up/ input enabled	Pull-up/ input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up/ input enabled	Pull-up/ input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/Internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/Internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) *1,*3	$USBV_{CC}0$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) *1,*3	$USBV_{CC}1$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for Ethernet-MAC) *1, *4	$ETHV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1 ,*5	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1 ,*5	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	Except for USB and Ethernet-MAC pin
		V_{SS} - 0.5	$USBV_{CC}0$ + 0.5 (≤ 6.5 V)	V	USB ch 0 pin
		V_{SS} - 0.5	$USBV_{CC}1$ + 0.5 (≤ 6.5 V)	V	USB ch 1 pin
		V_{SS} - 0.5	$ETHV_{CC}$ + 0.5 (≤ 6.5 V)	V	Ethernet-MAC Pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current *6	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
L level average output current *7	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*8	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current *6	I_{OH}	-	- 10	mA	4 mA type
			-20	mA	8 mA type
			- 20	mA	12 mA type
H level average output current *7	I_{OHAV}	-	- 4	mA	4 mA type
			-8	mA	8 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current *8	$\sum I_{OHAV}$	-	- 50	mA	
Storage temperature	T_{STG}	- 55	+ 150	°C	

1: These parameters are based on the condition that V_{SS} = AV_{SS} = 0.0 V.

12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	180 MHz	73	131	mA	*3 When all peripheral clocks are on
				*6	160 MHz	65	123	mA	
					144 MHz	59	117	mA	
					120 MHz	50	108	mA	
					100 MHz	43	101	mA	
					80 MHz	35	93	mA	
					60 MHz	27	85	mA	
					40 MHz	19	77	mA	
					20 MHz	11	69	mA	
					8 MHz	6.9	64	mA	
					4 MHz	5.3	63	mA	
				*5	180 MHz	44	102	mA	*3 When all peripheral clocks are off
				*6	160 MHz	40	98	mA	
					144 MHz	36	94	mA	
					120 MHz	31	89	mA	
					100 MHz	27	85	mA	
					80 MHz	22	80	mA	
					60 MHz	17	75	mA	
					40 MHz	13	71	mA	
					20 MHz	7.9	65	mA	
					8 MHz	5.2	63	mA	
					4 MHz	4.3	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

6: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory."

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7 (PLL)	*5	72 MHz	54	112	mA	*3 When all peripheral clocks are on
					60 MHz	47	105	mA	
					48 MHz	39	97	mA	
					36 MHz	31	89	mA	
					24 MHz	23	81	mA	
					12 MHz	14	72	mA	
					8 MHz	11	69	mA	
					4 MHz	7.2	65	mA	
				*5	72 MHz	37	95	mA	*3 When all peripheral clocks are off
					60 MHz	33	91	mA	
					48 MHz	28	86	mA	
					36 MHz	23	81	mA	
					24 MHz	17	75	mA	
					12 MHz	11	69	mA	
					8 MHz	8.3	66	mA	
					4 MHz	5.9	63	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

6: With data access to a MainFlash memory.

7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation (Other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation*5 (main oscillation)	4 MHz	2.6	60	mA	*3 When all peripheral clocks are on
					2.0	60	mA	*3 When all peripheral clocks are off
			Sleep operation (built-in High-speed CR)	4 MHz	2.0	60	mA	*3 When all peripheral clocks are on
					1.3	59	mA	*3 When all peripheral clocks are off
			Sleep operation*6 (sub oscillation)	32 kHz	0.46	58	mA	*3 When all peripheral clocks are on
					0.45	58	mA	*3 When all peripheral clocks are off
			Sleep operation (built-in low-speed CR)	100 kHz	0.47	58	mA	*3 When all peripheral clocks are on
					0.46	58	mA	*3 When all peripheral clocks are off

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0.

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	180	MHz	

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

12.4.5 Operating Conditions of USB/Ethernet PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB/Ethernet
USB/Ethernet clock frequency *2	f_{CLKPLL}	-	-	50	MHz	After the M frequency division

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

NAND Flash Mode

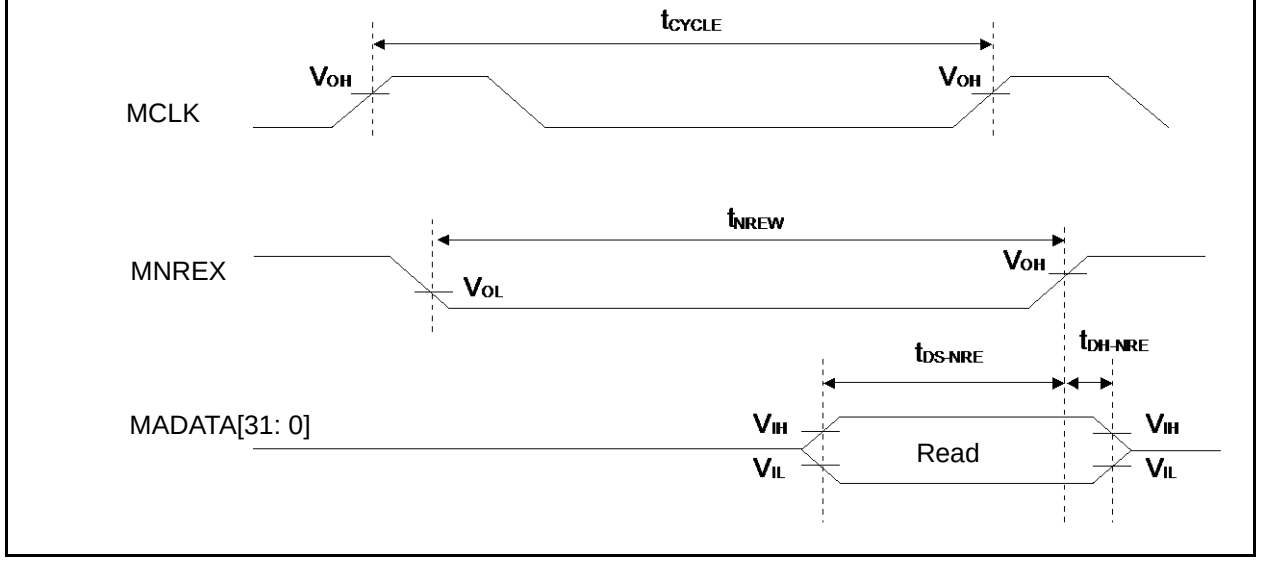
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t_{NREW}	MNREX	-	MCLK×n-3	-	ns	
Data set up →MNREX ↑ time	t_{DS-NRE}	MNREX, MADATA[31: 0]	-	20	-	ns	
MNREX ↑ → Data hold time	t_{DH-NRE}	MNREX, MADATA[31: 0]	-	0	-	ns	
MNALE ↑ → MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNALE ↓ → MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNCLE ↑ → MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNWEX ↑ → MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	-	0	MCLK×m+9	ns	
MNWEX Min pulse width	t_{NWEW}	MNWEX	-	MCLK×n-3	-	ns	
MNWEX ↓ → Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[31: 0]	-	-9	9	ns	
MNWEX ↑ → Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*

NAND Flash Read



12.4.12 CSIO (SPI) Timing

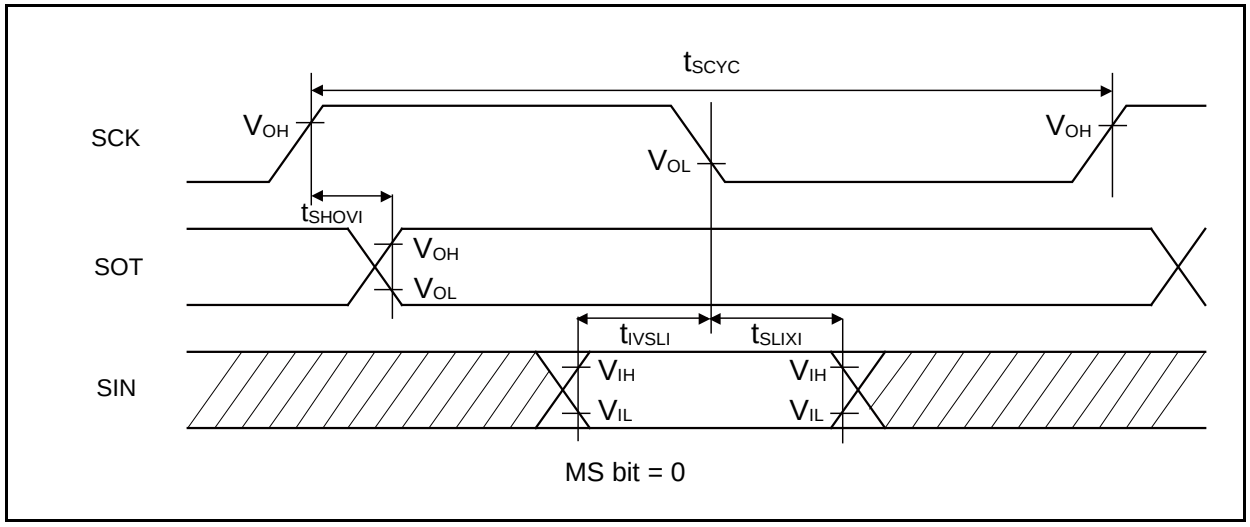
Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

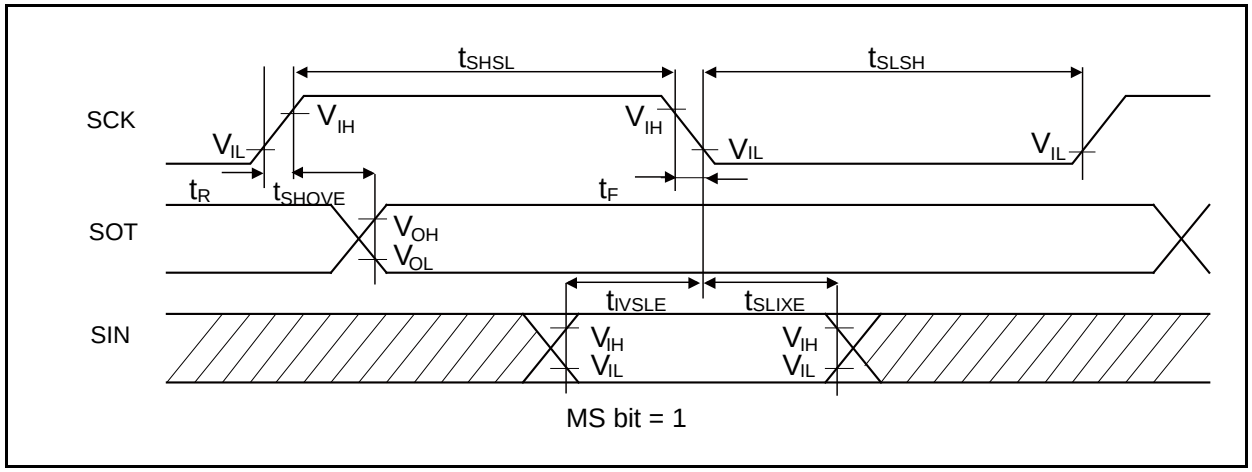
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

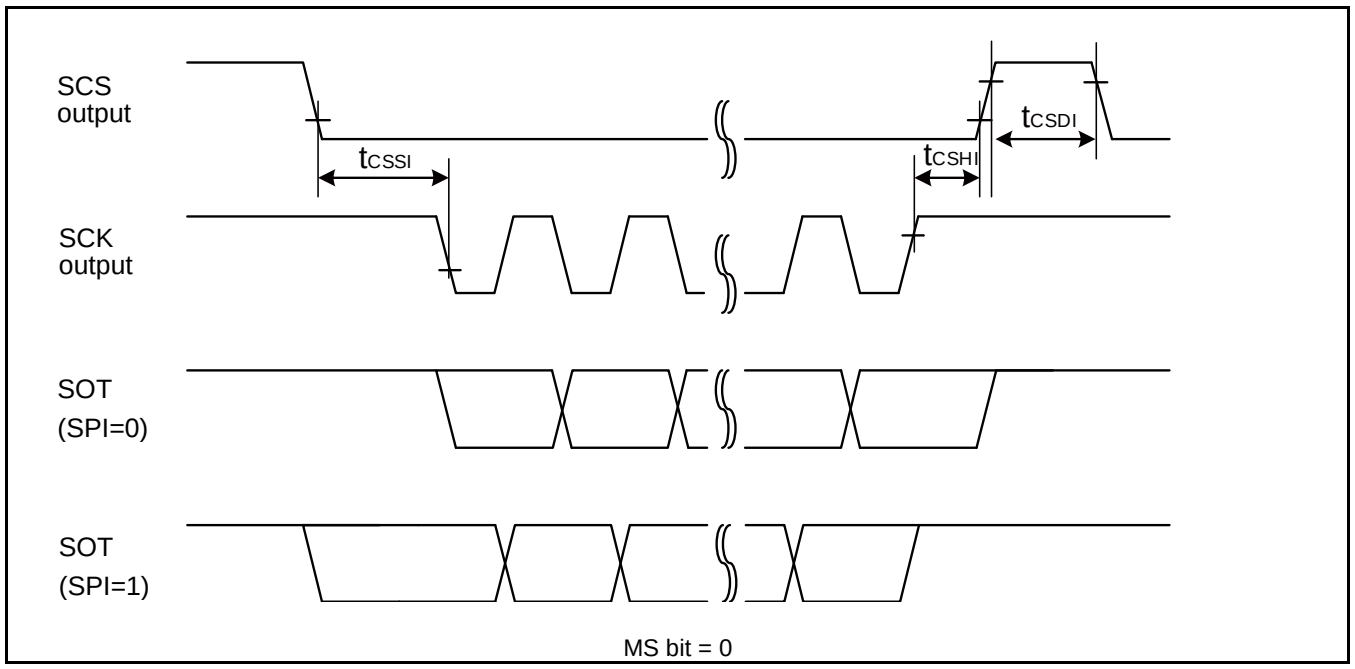
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



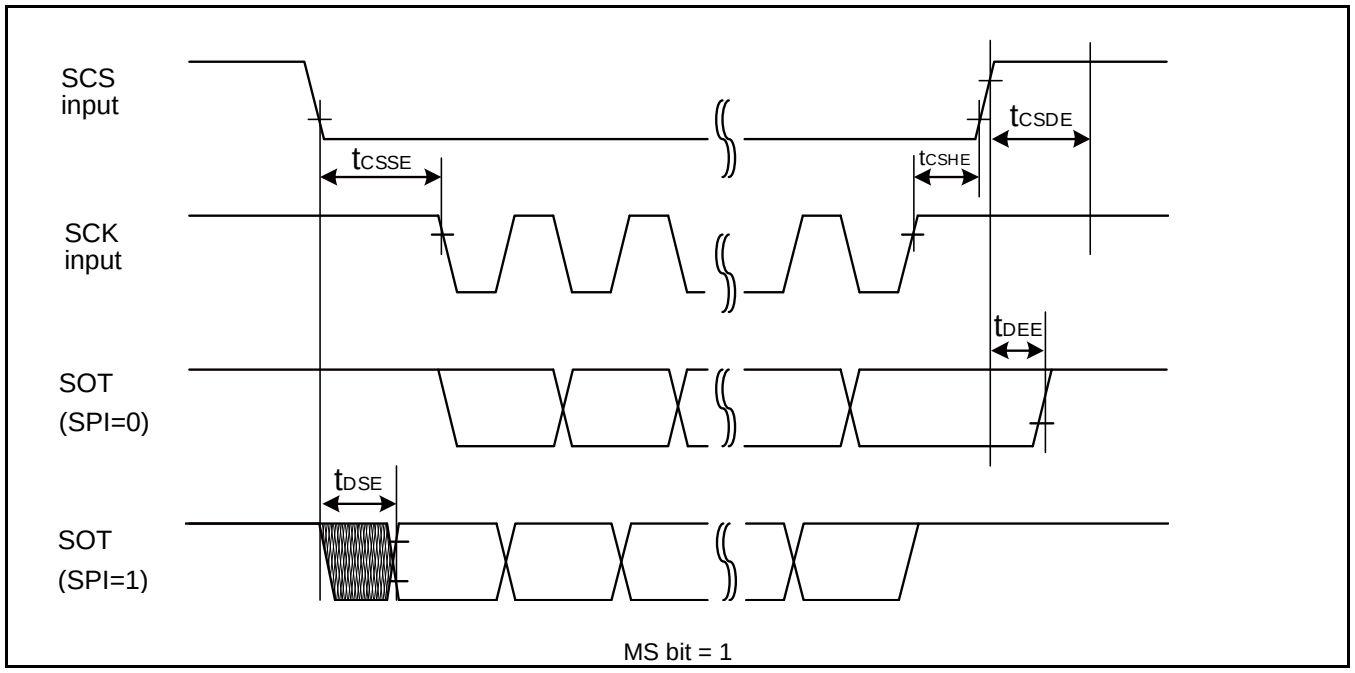
MS bit = 0



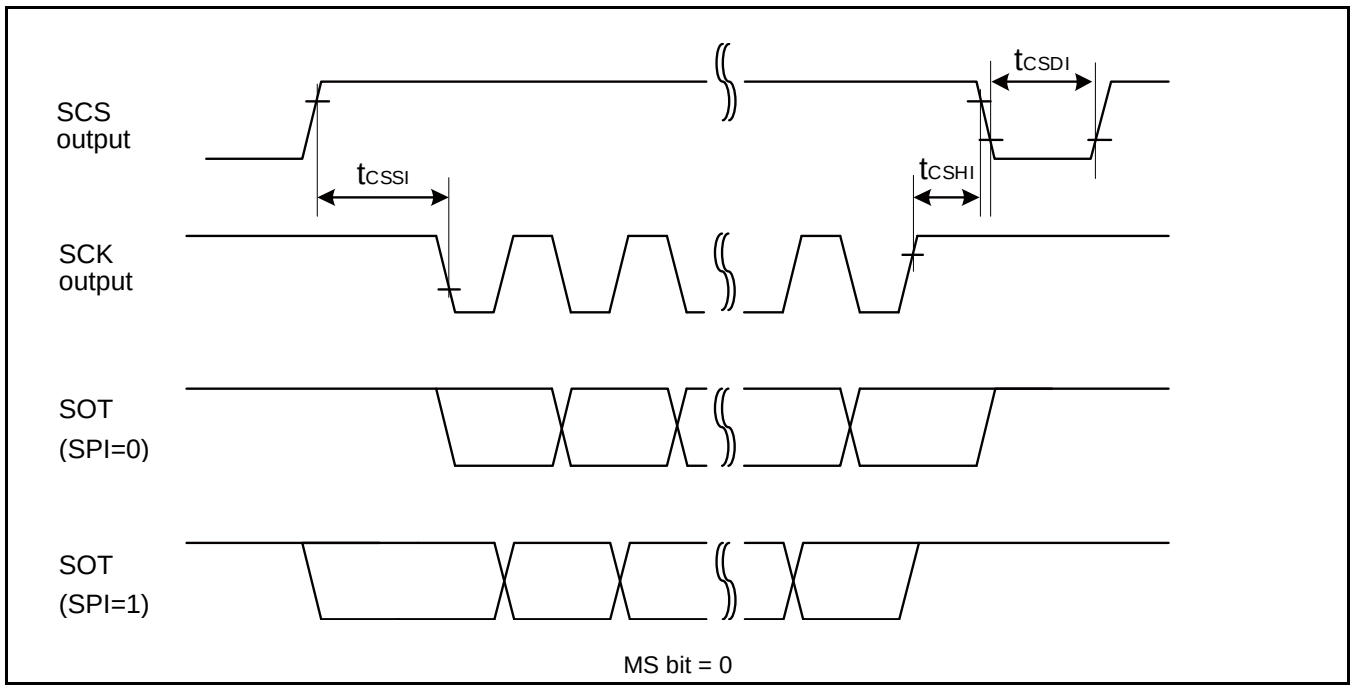
MS bit = 1



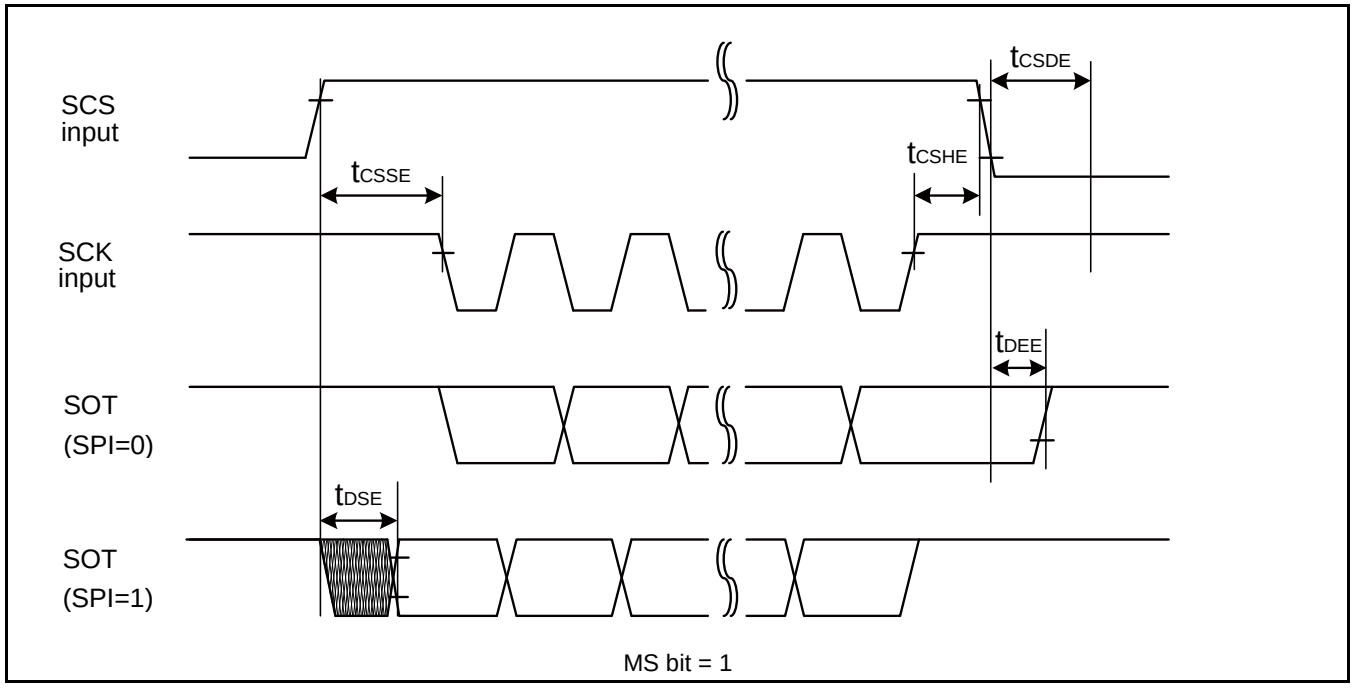
MS bit = 0



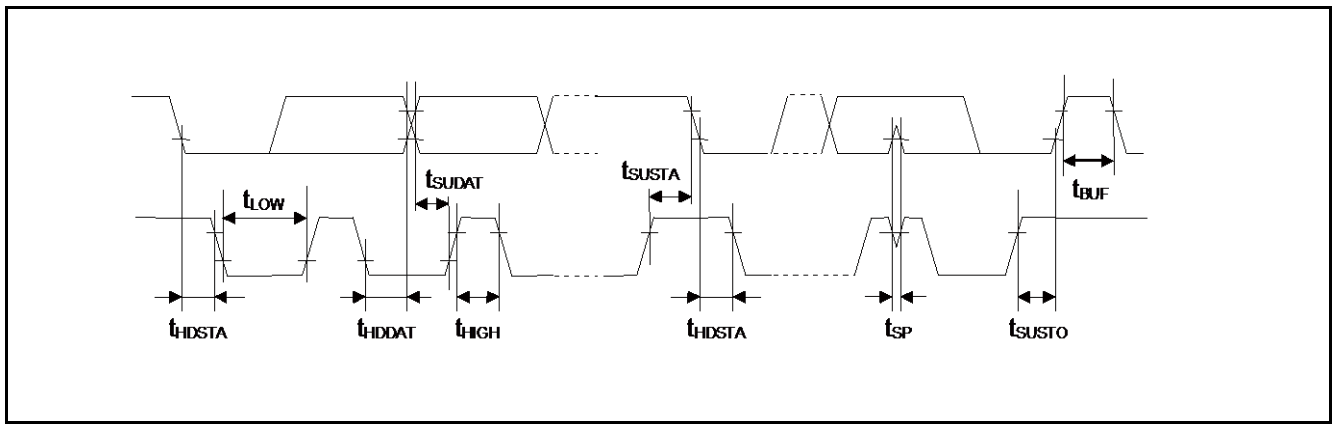
MS bit = 1



MS bit = 0



MS bit = 1


tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

12.6 USB Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, $USBV_{CC}0$ = $USBV_{CC}1$ = 3.0V to 3.6V, V_{SS} = AV_{SS} = 0V)

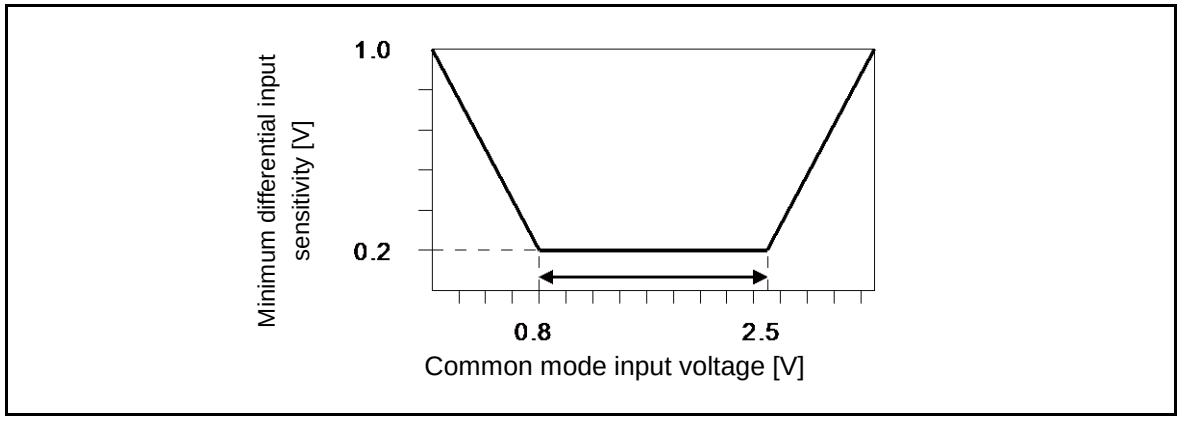
Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0/ UDM0, UDP1/ UDM1	-	2.0	$USBV_{CC}$ + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rise time	t_{FR}		Full-Speed	4	20	ns	*5
	Fall time	t_{FF}		Full-Speed	4	20	ns	*5
	Rise/fall time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rise time	t_{LR}		Low-Speed	75	300	ns	*7
	Fall time	t_{LF}		Low-Speed	75	300	ns	*7
	Rise/fall time matching	t_{LRFM}		Low-Speed	80	125	%	*7

1: The switching threshold voltage of the single-end-receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).

There is some hysteresis applied to lower noise sensitivity.

2: Use differential-receiver to receive USB differential data signal. Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

Above voltage range is the common mode input voltage range.



12.7 Low-Voltage Detection Characteristics

12.7.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

12.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	6000×t_{CYCP}*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.8 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	-	0.3	1.1	s	
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time*		-	13.6	68	s	Includes write time prior to internal erase

*: It indicates the chip erase time of 1MB MainFlash memory

For devices with 1.5 MB or 2 MB of MainFlash memory, two erase cycles are required.

See 3.2.2 Command Operating Explanations and 3.3.3 Flash Erase Operation in this product's Flash Programming Manual for the detail.

Write Cycles and Data Retention Time

Erase/Write Cycles (Cycle)	Data Retention Time (Year)
1,000	20*
10,000	10*
100,000	5*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C).

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				S6E2GM6JHAGV20000, S6E2GM8H0AGV20000, S6E2GM8HHAGV20000, S6E2GM8J0AGV20000, S6E2GM8JHAGV20000 Added MPNs below to “13. Ordering Information” (Page 185) S6E2G26H0AGV2000A, S6E2G26HHAGV2000A, S6E2G26J0AGV2000A, S6E2G26JHAGV2000A, S6E2G28H0AGV2000A, S6E2G28HHAGV2000A, S6E2G28J0AGV2000A, S6E2G28JHAGV2000A, S6E2G36H0AGV2000A, S6E2G36J0AGV2000A, S6E2G38H0AGV2000A, S6E2G38J0AGV2000A, S6E2GH6H0AGV2000A, S6E2GH6J0AGV2000A, S6E2GH8H0AGV2000A, S6E2GH8J0AGV2000A, S6E2GK6H0AGV2000A, S6E2GK6HHAGV2000A, S6E2GK6J0AGV2000A, S6E2GK6JHAGV2000A, S6E2GK8H0AGV2000A, S6E2GK8HHAGV2000A, S6E2GK8J0AGV2000A, S6E2GK8JHAGV2000A, S6E2GM6H0AGV2000A, S6E2GM6HHAGV2000A, S6E2GM6J0AGV2000A, S6E2GM6JHAGV2000A, S6E2GM8H0AGV2000A, S6E2GM8HHAGV2000A, S6E2GM8J0AGV2000A, S6E2GM8JHAGV2000A Modified typo about the munber of QPRC channels(from 4ch to 2ch) (Page 1,6,10) Modified the expression of the “Built-in CR” in “2. Product Lineup”(Page 6).