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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	3.6MHz
Connectivity	Serial Port
Peripherals	LCD, POR, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-QFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w925e625fg

1. GENERAL DESCRIPTION

The W925E/C625 is an all in one single 8-bit micro-controller with widely used Calling Identity Delivery (CID) function. The 8-bit CPU core is based on the 8051 family; therefore, all the instructions are compatible to the Turbo 8051 series. The CID part consisted of FSK decoder, DTMF receiver, CPE* Alert Signal (CAS) detector and Ring detector. Also built-in DTMF generator and FSK generator with baud rate 1200 bps (bits/sec). Using W925E/C625 can easily implement the CID adjunct box and the feature phone or Short Message Service (SMS) phone with CID function. The main features are listed in the next section.

2. FEATURES

- **APPLICATION**: The ***SMS*** phone with CID function and CID adjunct box.
- **CPU**: 8-bit micro-controller is similar to the 8051 family.
  - EEPROM type operating voltage:

    μC: Depend on the operating vol. option. Either 2.4 to 3.6V or 3.0 to 5.5V for operating. If 2.4 to 3.6V be selected, the μC operating range is from 2.4 to 3.6V, else if 3.0 to 5.5V be selected, the μC operating range is from 3.0 to 5.5V.

    CID: 3.0 to 5.5V.
  - MASK type operating voltage:

    μC: 2.2 to 5.5V.

    CID: 3.0 to 5.5V.
- **Dual-clock operation:**
  - Main oscillator: 3.58MHz crystal for CID and DTMF function. And built-in RC oscillator.
  - Sub oscillator: 32768Hz crystal.
  - Main and sub oscillators are enable/disable by bit control individually.
- **ROM**: 64K bytes internal flash EEPROM/MASK ROM type.
  - Up 64K bytes for program ROM.
  - Total 64K bytes for look-up table ROM.
- **RAM**:
  - 256 bytes on chip scratch-pad RAM.
  - 4K bytes on chip RAM for MOVX instruction.
  - 224 bytes on chip LCD RAM.
- **LCD**: dot matrix control method.
  - 1792 dots: 56 Segments x 32 Common, 1/5 bias.
- **CID**:
  - Compatible with Bellcore TR-NWT-000030 & SR-TSV-002476, British Telecom(BT) SIN227, U.K. Cable Communication Association(CCA) specification.
  - FSK modulator/demodulator: for Bell 202 and ITU-T V.23 FSK with 1200-baud rate.
  - CAS detector: for dual tones of Bellcore CAS and BT Idle State and Loop State Dual Tone Alert Signal (DTAS).

- DTMF generator/receiver;
- Ring detector: for line reversal for BT, ring burst for CCA or ring signal for Bellcore.
- Two independent OP amps with adjustable gain for Tip/Ring and Telephone Hybrid connections.

- **I/O**: 40 I/O pins.
  - P0: Bit and byte addressable. I/O mode can be bit controlled. Open drain type.
  - P1~P3: Bit and byte addressable. Pull high and I/O mode can be bit controlled.
  - P4 : Byte addressable. Pull high and I/O mode can be bit controlled.

Note: "CPE*" Customer Premises Equipment

- **Power mode**:
  - **Normal mode**: Normal operation
  - **Dual-clock slow operation mode**: System is operated by the sub-oscillator (Fosc=Fs and Fm is stopped)
  - **Idle mode**: CPU hold. The clock to the CPU is halted, but the interrupt, timer and watchdog timer block work normally but CID function is disabled.
  - **Power down mode**: All activity is completely stopped and power consumption is less than 1 μA.
- **Timer**: 2 13/16-bit timers, or 8-bit auto-reload timers, that are Timer0 and Timer1.
- **Watchdog timer:** WDT can be programmed by the user to serve as a system monitor.
- **Interrupt:** 11 interrupt sources with two levels of priority.
  - 4 interrupts from INT0, INT1, INT2 and INT3.
  - 2 interrupts from Timer0, Timer1.
  - 1 interrupt from Serial port.
  - 1 interrupt from CID.
  - 1 interrupt from 13/14-bit Divider.
  - 1 interrupt from Comparator.
  - 1 interrupt from Watch Dog Timer.
- **Divider:** 13/14 bit divider, clock source from sub-oscillator, therefore, DIVF set every 0.25/0.5 Sec.
- **Comparator:**
  - Comparator:1 analog input from VNEG pin, 2 reference input pins, one is from VPOS pin and another is from internal 1.0v regulator output.
- **Serial port:**
  - An 8-bit serial transceiver with SCLK and SDATA.
- **Package:**
  - 160pin QFP : The part numbers are W925E625 & W925C625
  - Lead free 160pin QFP: The part numbers are W925E625FG & W925G625

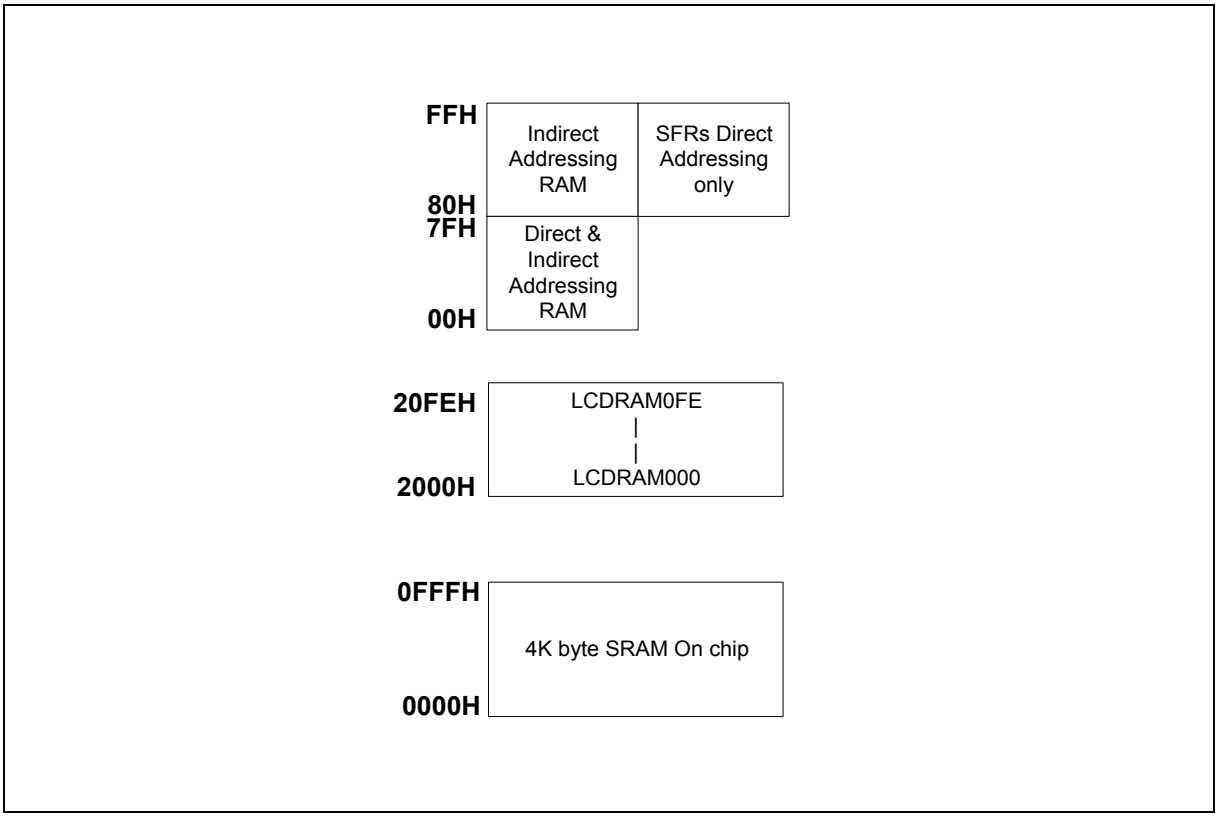


Figure 6-2 Memory Map

6.2 Special Function Registers

The W925E/C625 uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes.

The SFRs reside in the register locations 80-FFh and accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where one wishes to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The list of SFRs is as follows. The table is condensed with eight locations per row. Empty locations indicate that there are no registers at these addresses. The content of reserved bits or registers is not guaranteed.

Table 1 Special Function Register Location Table

F8	EIP	CIDGD	CIDGA					
F0	B							
E8	EIE							
E0	ACC							
D8	WDCON							
D0	PSW							
C8	DIVC							
C0	SCON1	SBUF1	REGVC		PMR	STATUS	FSKTC	FSKTB
B8	IP		DTMFG	COMPR	IRC1	IRC2	CASPT	CASAT
B0	P3	CIDR	CIDFG	CIDPCR	FSKDR	DTMFDR	DTMFPT	DTMFAT
A8	IE						P4IO	
A0	P2	HB	P4H				P4	
98				P1EF		P1H	P2H	P3H
90	P1	EXIF		P1SR	P0IO	P1IO	P2IO	P3IO
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON1	CKCON2
80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON

A brief description of the SFRs now follows.

PORT 0 (initial=FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

P0: P0 can be selected as input or output mode by the P0IO register, at initial reset, P0IO is set to FFH, P0 is used as input mode. When P0IO is set to 0, the P0 is used as CMOS open drain mode.

STACK POINTER (initial=07H)

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

SP: The Stack Pointer stores the scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

DATA POINTER LOW (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

DPL: This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

DPH: This is the high byte of the standard 8052 16-bit data pointer.

DATA POINTER LOW1 (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

Mnemonic: DPL1 Address: 84h

DPL1: This is the low byte of the new additional 16-bit data pointer. That has been added to the W925E/C625. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS.0 = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required, they can be used as conventional register locations by the user.

DATA POINTER HIGH1 (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

Mnemonic: DPH1 Address: 85h

DPH1: This is the high byte of the new additional 16-bit data pointer. That has been added to the W925E/C625. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required, they can be used as conventional register locations by the user.

DATA POINTER SELECT (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS.0

Mnemonic: DPS Address: 86h

DPS.0: This bit is used to select either the DPL,DPH pair or the DPL1,DPH1 pair as the active Data Pointer. When set to 1, DPL1,DPH1 will be selected, otherwise DPL,DPH will be selected.

DPS.1-7:These bits are reserved, but will read 0.

POWER CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	IDLT	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

IDLT: This bit controls the idle mode type. In idle mode when idle mode is released by any interrupt, if IDLT=1 it will not jump to the corresponding interrupt; if IDLT=0 it will jump to the corresponding interrupt.

GF1-0: These two bits are general-purpose user flags.

PD: Setting this bit causes the W925E/C625 to go into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen. Power down mode can be released by INT0~INT3 and ring detection of CID interrupt.

IDL: Setting this bit causes the W925E/C625 to go into the IDLE mode. The type of idle mode is selected by IDLT. In this mode the clocks to the CPU are stopped, so program execution is frozen. However, the clock path to the timers blocks and interrupt blocks is not stopped, and these blocks continue operating.

TIMER 0 LOW BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 low byte register.

TIMER 1 LOW BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 low byte register.

TIMER 0 HIGH BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0: Timer 0 high byte register.

TIMER 1 HIGH BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 high byte register.

CLOCK CONTROL1 (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T1S1	T1S0	T0S1	T0S0	DIVS	$\overline{M}$/S

Mnemonic: CKCON1 Address: 8Eh

WD1-0: Watchdog timer mode select bits: These bits determine the time-out period for the watchdog timer. In all four time-out options, the reset time-out is 512 clocks more than the interrupt time-out period.

WD1	WD0	Interrupt time-out	Reset time-out
0	0	Fosc/2^{12}	Fosc/2^{12} + 512
0	1	Fosc/2^{15}	Fosc/2^{15} + 512
1	0	Fosc/2^{18}	Fosc/2^{18} + 512
1	1	Fosc/2^{21}	Fosc/2^{21} + 512

P2 PULL-HIGH CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	P2.7H	P2.6H	P2.5H	P2.4H	P2.3H	P2.2H	P2.1H	P2.0H

Mnemonic: P2H Address: 9Eh

P2H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

P3 PULL-HIGH CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	P3.7H	P3.6H	P3.5H	P3.4H	P3.3H	P3.2H	P3.1H	P3.0H

Mnemonic: P3H Address: 9Fh

P3H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

PORT 2 (initial=FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is an I/O port with internal pull-high resistor. P2 can be selected as input or output mode by the P2IO register. At initial reset, P2 is used as input mode. When P2IO is set to 0, P2 is used as CMOS output mode.

HIGH BYTE REGISTER (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	HB.7	HB.6	HB.5	HB.4	HB.3	HB.2	HB.1	HB.0

Mnemonic: HB Address: A1h

This register contains the high byte address during execution of " MOVX @Ri, " instructions.

P4 PULL-HIGH CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	P4.7H	P4.6H	P4.5H	P4.4H	P4.3H	P4.2H	P4.1H	P4.0H

Mnemonic: P4H Address: A2h

P4H: Port4 pins pull-high resistor enable/disable

1: enable

0: disable

PORT 4 (initial=FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A6h

P4.7-0: Port 4 is a I/O port with internal pull-high resistor. P4 can be selected as input or output mode by the P4IO register, at initial reset, P4IO is set to 0FFh, P4 is used as input mode. When P4IO is set to 00h, P4 is used as CMOS output mode. Special function of P4 is described below.

P4.4	VPOS	Positive input of the comparator
P4.2	VNEG	Negative input of the comparator
P4.1	SDATA	Serial port data I/O
P4.0	SCLK	Serial port clock I/O

INTERRUPT ENABLE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	EA	ES1	-	-	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

EA: Global enable. Enable/disable all interrupts.

ES1: Enable Serial port interrupt

ET1: Enable Timer 1 interrupt

EX1: Enable external interrupt 1

ET0: Enable Timer 0 interrupt

EX0: Enable external interrupt 0

P4 I/O PORT CONTROL (initial=FFH)

Bit:	7	6	5	4	3	2	1	0
	P4.7IO	P4.6IO	P4.5IO	P4.4IO	P4.3IO	P4.2IO	P4.1IO	P4.0IO

Mnemonic: P4IO Address: Aeh

P4IO: P4 pins I/O control.

1: input mode

0: output mode

PORT 3 (initial=FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: P3 can be selected as input or output mode by the P3IO register, at initial reset, P3IO is set to 0FFH, P3 is used as input mode. When P3IO is set to 00h, the P3 is used as CMOS output mode. Special function of P3 is described below.

P3.5	T1	Timer/Counter 1 external count input
P3.4	T0	Timer/Counter 0 external count input
P3.3	$\overline{INT1}$	External interrupt 1
P3.2	$\overline{INT0}$	External interrupt 0

CID REGISTER (initial=00H,**read only**)

Bit:	7	6	5	4	3	2	1	0
	-	FCLK	FDATA	FCD	DTMFD	FDR	ALGO	RNG

Mnemonic: CIDR Address: B1h

This SFR indicates the CID signal immediately. Register data is set or cleared by hardware only.

FCLK: FSK serial clock with the baud rate of 1200Hz.

FDATA: FSK serial bit data.

FCD: Set when FSK carrier is detected. Cleared when FSK carrier is disappeared.

DTMFD: Set when DTMF decoded data is ready. Cleared when DTMF signal ends.

FDR: Set when FSK 8 bits data is ready. Cleared before next FSK start bit comes

ALGO: Dual tone Alert signal Guard time detect signal. Set when a guard time qualified dual tone alert signal has been detected. Cleared when the guard time qualified dual tone alert signal is absent.

RNG: Ring detection bit. High to indicate the detection of line reversal and/or ringing.

CID FLAG GENERATOR (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	FSF	DTMFDF	FDRF	ALGOF	RNGF

Mnemonic: CIDFG Address: B2h

FSF: Set when FSK Latch clock low to high. Cleared by software

DTMFDF: Set when DTMFD low to high. Cleared by software

FDRF: Set when FDR low to high. Cleared by software.

ALGOF: Set when ALGO low to high. Cleared by software.

RNGF: Set when RNG low to high. Cleared by software.

CID POWER CONTROL REGISTER (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	CIDE	-	FSKE	CASE	DTMFE

Mnemonic: CIDPCR Address: B3h

CAS TONE PRESENT TIME REGISTER (initial=0FH)

Bit:	7	6	5	4	3	2	1	0
	CASPT7	CASPT6	CASPT5	CASPT4	CASPT3	CASPT2	CASPT1	CASPT0

Mnemonic: CASPT Address: Beh

The clock period of guard-time timer is 0.8582Ms. The default alert tone present time is 12.87Ms.

CASPT7-0: The pre-set data register for counting CAS tone present time. When CAS tone is detected (ALGR low to high), the guard timer starts to up-count from 00H. As the guard timer is equal to the value of CASPT, the exist of the CAS tone is accepted. ALGR changes to low state to stop and reset the counter.

CAS TONE ABSENT TIME REGISTER (initial=0FH)

Bit:	7	6	5	4	3	2	1	0
	CASAT7	CASAT6	CASAT5	CASAT4	CASAT3	CASAT2	CASAT1	CASAT0

Mnemonic: CASAT Address: BFh

The clock period of guard-time timer is 0.8582Ms. The default alert tone absent time is 12.87Ms.

CASAT7-0: The pre-set data register for counting CAS tone absent time. When CAS tone is absent (ALGR high to low), the guard timer starts to up-count from 00H. As the guard timer is equal to the value of CASAT, the finish of CAS tone is recognized. ALGR changes to high state to stop and reset the counter.

SERIAL PORT CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	SF1	LCDON	REGON	REN1	SFQ	SEDG	CLKIO	SIO

Mnemonic: SCON1 Address: C0h

SF1: Serial port interrupt flag. When 8-bits data transited completely, SF1 is set by hardware. SF1 is cleared when serial interrupt routine is executed or cleared by software.

LCDON: LCD waveform enable control. 0 to Disable LCD display, 1 to Enable LCD display.

REGON: Regulator on/off control. 0 to disable regulator, 1 to regulator.

REN1: Set REN1 from 0 to 1 to start the serial port1 to receive 8-bit serial data.

SFQ: SFQ=0 Serial clock output frequency is equal to f_{OSC} /2

SFQ=1 Serial clock output frequency is equal to f_{OSC} /256

SEDG: SEDG=0 Serial data latched at falling edge of clock, SCLK=Low initially.

SEDG=1 Serial data latched at rising edge of clock, SCLK=High initially.

CLKIO: CLKIO=0 P4.0(SCLK) work as output mode

CLKIO=1 P4.0(SCLK) work as input mode

SIO: SIO=0 P4.0 & P4.1 work as normal I/O pin

SIO=1 P4.0 & P4.1 work as Serial port1 function

Table 3. Instruction Timing for W925E/C625, continued

INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES	INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES
ADDC A, R4	3C	1	1	CJNE A, #data, rel	B4	3	4
ADDC A, R5	3D	1	1	CJNE @R0, #data, rel	B6	3	4
ADDC A, R6	3E	1	1	CJNE @R1, #data, rel	B7	3	4
ADDC A, R7	3F	1	1	CJNE R0, #data, rel	B8	3	4
ADDC A, @R0	36	1	1	CJNE R1, #data, rel	B9	3	4
ADDC A, @R1	37	1	1	CJNE R2, #data, rel	BA	3	4
ADDC A, direct	35	2	2	CJNE R3, #data, rel	BB	3	4
ADDC A, #data	34	2	2	CJNE R4, #data, rel	BC	3	4
ACALL addr11	71,91,B1, 11,31,51, D1,F1	2	3	CJNE R5, #data, rel	BD	3	4
AJMP ADDR11	01,21,41, 61,81,A1, C1,E1	2	3	CJNE R6, #data, rel	BE	3	4
CJNE R7, #data, rel	BF	3	4	JC rel	40	2	3
CLR A	E4	1	1	JNC rel	50	2	3
CPL A	F4	1	1	JB bit, rel	20	3	4
CLR C	C3	1	1	JNB bit, rel	30	3	4
CLR bit	C2	2	2	JBC bit, rel	10	3	4
CPL C	B3	1	1	LCALL addr16	12	3	4
CPL bit	B2	2	2	LJMP addr16	02	3	4
DEC A	14	1	1	MUL AB	A4	1	5
DEC R0	18	1	1	MOV A, R0	E8	1	1
DEC R1	19	1	1	MOV A, R1	E9	1	1
DEC R2	1A	1	1	MOV A, R2	EA	1	1
DEC R3	1B	1	1	MOV A, R3	EB	1	1
DEC R4	1C	1	1	MOV A, R4	EC	1	1
DEC R5	1D	1	1	MOV A, R5	ED	1	1
DEC R6	1E	1	1	MOV A, R6	EE	1	1
DEC R7	1F	1	1	MOV A, R7	EF	1	1
DEC @R0	16	1	1	MOV A, @R0	E6	1	1
DEC @R1	17	1	1	MOV A, @R1	E7	1	1
DEC direct	15	2	2	MOV A, direct	E5	2	2
DEC DPTR	A5	1	2	MOV A, #data	74	2	2
DIV AB	84	1	5	MOV R0, A	F8	1	1
DA A	D4	1	1	MOV R1, A	F9	1	1
DJNZ R0, rel	D8	2	3	MOV R2, A	FA	1	1
DJNZ R1, rel	D9	2	3	MOV R3, A	FB	1	1
DJNZ R2, rel	DA	2	3	MOV R4, A	FC	1	1
DJNZ R3, rel	DB	2	3	MOV R5, A	FD	1	1
DJNZ R4, rel	DC	2	3	MOV R6, A	FE	1	1

service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts INT2 to INT3 are edge triggered only.

The TF0, TF1 flags generate the Timer 0, 1 Interrupts. These flags are set by the overflow in the Timer 0, Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog timer interrupt flag WDIF (WDCON.3) is set. If the enable bit EIE.5 enables the interrupt, then an interrupt will occur.

The Serial block can generate interrupts on reception or transmission. There are one interrupt sources from the Serial block, which are obtained by SF1 in the SCON1. SF1 is cleared automatically when the serial port interrupt is serviced.

The divider interrupt is generated by DIVF that is set when divider overflows. DIVF is set by hardware and cleared when divider interrupt is serviced. The divider interrupt is enable/disable if the bit EDIV is high/low.

The comparator interrupt is produced by COMPF, which is set when the RESC bit is changed from low to high. RESC, which is the real-time result of comparator, set when the voltage of reference input is higher than the voltage of analog input.

The CID interrupt is generated by CIDF. The CIDF is a logic OR output of all CID flags which are set by hardware and cleared by software. The structure of the CID flags is shown in Figure 6-4.

Each of the individual interrupts can be enabled or disabled by setting or clearing the corresponding bits in the IE and EIE SFR. A bit EA, which is located in IE.7, is a global control bit to enable/disable the all interrupt. When bit EA is zero all interrupts are disable and when bit EA is high each interrupt is enable individually by the corresponding bit.

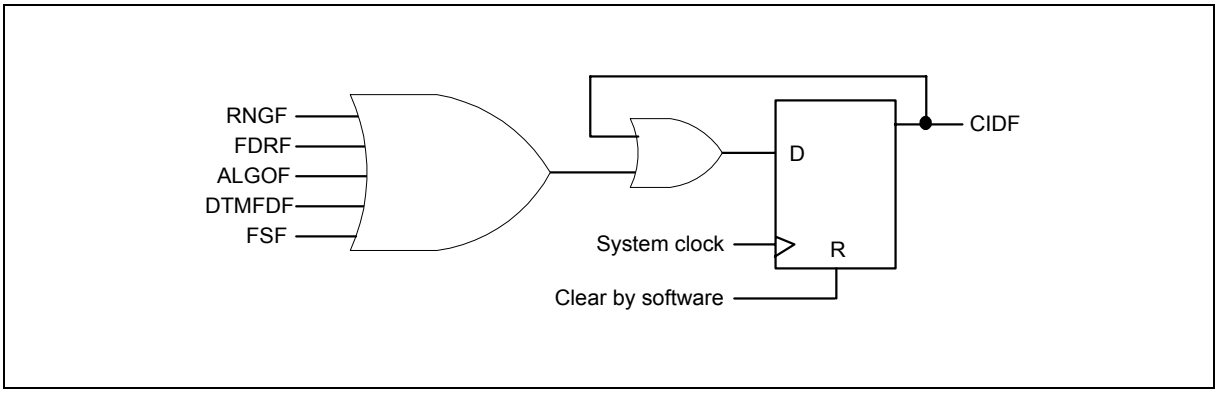


Figure 6-4 The Structure of CID Flags

Priority Level Structure

There are two priority levels for the interrupts, high and low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.

Table 4 Interrupt table.

INTERRUPT	FLAG NAME	FLAG LOCATION	EN BIT	EN BIT LOCATION	PRIORITY	FLAG CLEARED BY	INTERRUPT VECTOR
External interrupt 0	IE0	TCON.1	EX0	IE.0			

Bit:	7	6	5	4	3	2	1	0
	-	DTGE	HE	LE	L1	L0	H1	H0

Mnemonic: DTMFGR Address: Bah

L1	L0	H1	H0	SELECTED TONE
x	x	0	0	1209Hz
x	x	0	1	1336Hz
x	x	1	0	1477Hz
x	x	1	1	1633Hz
0	0	x	x	697Hz
0	1	x	x	770Hz
1	0	x	x	852Hz
1	1	x	x	941Hz

LE: Enable low group frequency output.

HE: Enable high group frequency output.

DTGE: Enable dual tone output to DTMF pin.

6.12 FSK Generator

W925E/C625 provides a FSK generator which outputs the FSK signal to the DTMF pin. The FSK output share with DTMF output pin. It can out FSK signal with 1200Hz baud rate of ITU-T V.23 or Bellcore 202 signal. A FSK transmit data register (FSKTB) specifies the desired output data. The FSK Transmit Control Register (FSKTC) can control whether the FSK signal will be output or not. The relation timing is shown in Figure 6-12.

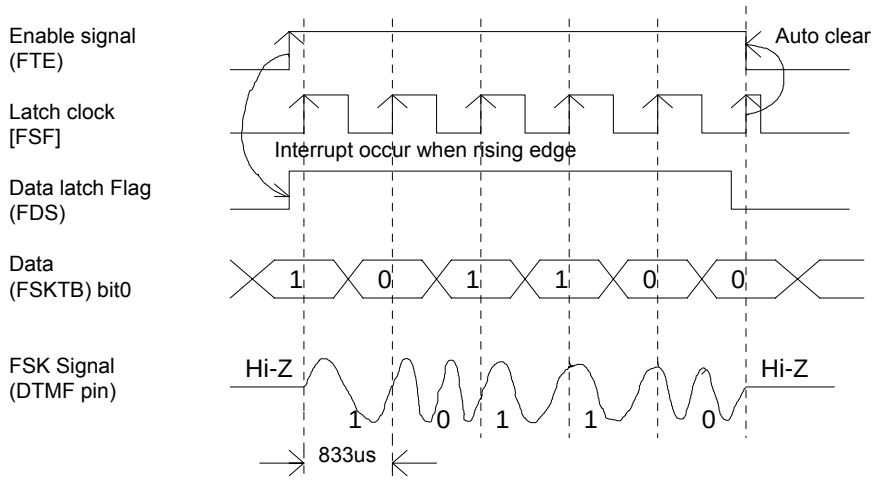


Figure 6-12 FSK Modulator

LCD Power Connection

The LCD power connection of bias is shown in Figure 6-15

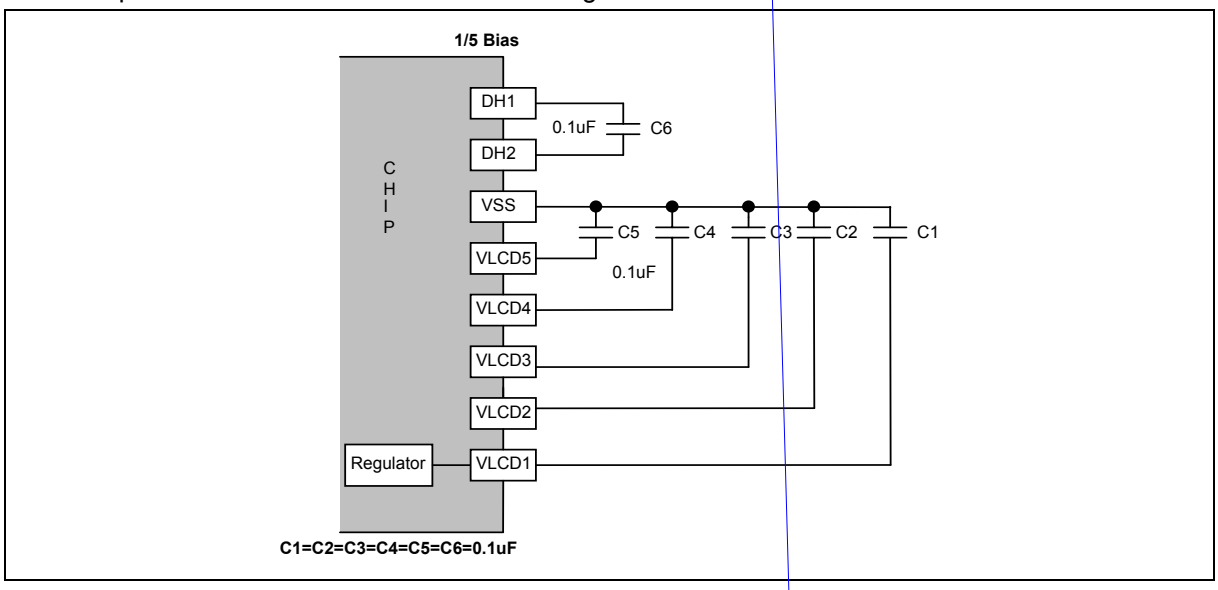
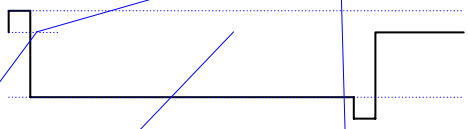


Figure 6-15 1/5 Bias LCD Power Connection

LCD Waveform

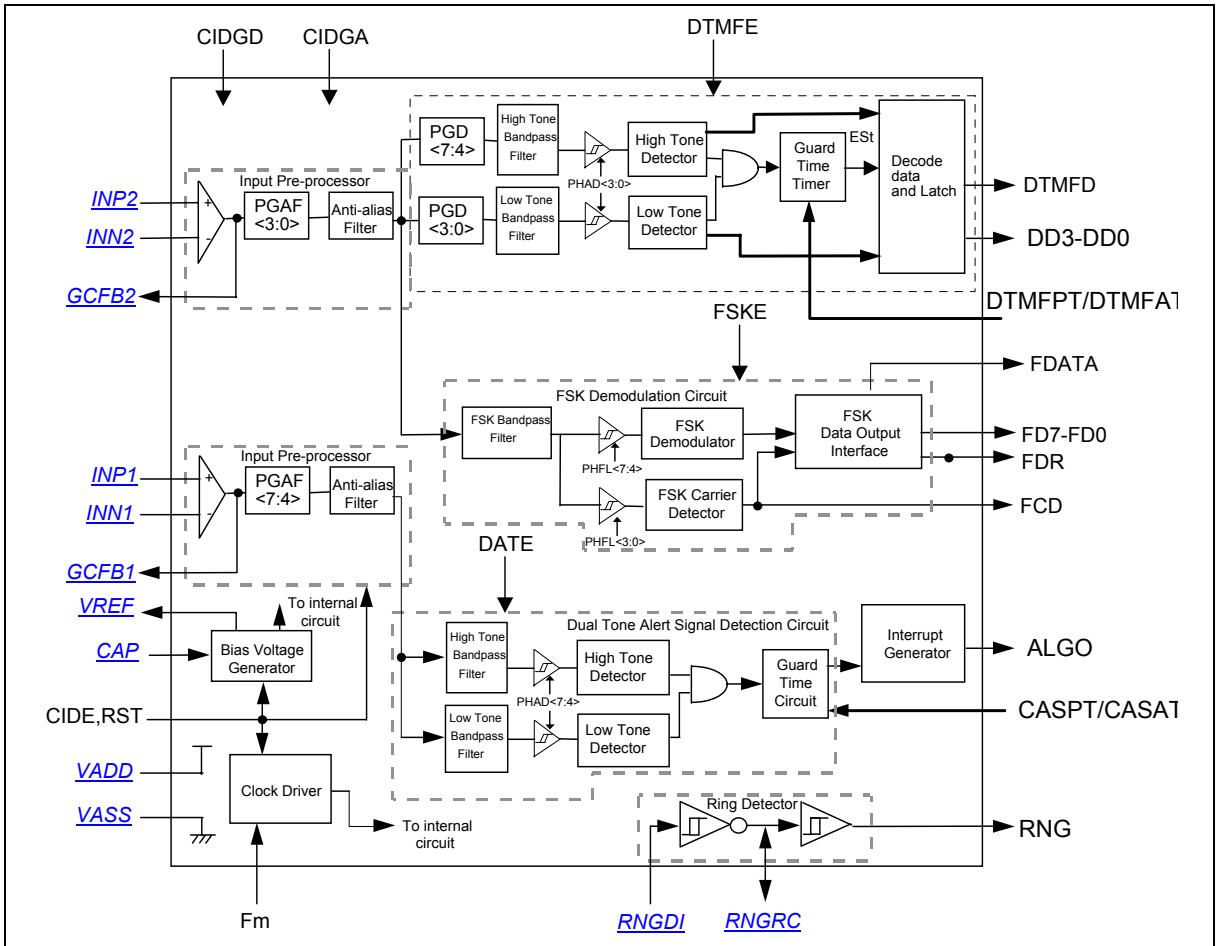
The LCD waveform is B type. Figure 6-16 is an example for 1/5 bias LCD waveform.



6.16 Calling Identity Delivery (CID)

W925E/C625 provides type I and type II of CID system. Type I is on-hook calling with CID message and type II is off-hook call on waiting. The CID function includes FSK decoder, dual tone alert signal detector, ring detector and DTMF receiver. The FSK demodulation function can demodulate Bell 202 and ITU-T V.23 Frequency Shift keying (FSK) with 1200 baud rate. The Tone Alert Signal detect function can detect dual tones of Bellcore Customer Premises Equipment(CPE) Tone Alerting Signal(CAS) and BT Idle State and Loop State Tone Alert Signal. The line reversal for BT, ring burst for CCA or ring signal for Bellcore can be detected by ring detector. It is compatible with Bellcore TR-NWT-000030 & ST-TSV-002476, British Telecom(BT) SIN227, U.K. Cable Communications Association(CCA) specification. The DTMF receiver can be programmed as DTMF decoder to decode 16 DTMF signals or tone detector to detect the signal which frequency is in DTMF band. The tone detector can be an auxiliary detector to improve the performance of detecting tone alerting signal(CAS), said as talk down-off, in type II system.

The FSK decoder, alert tone detector and DTMF receiver can be enable/disable individually by the bits of FSKE, CASE and DTMFE in FSK DATA REGISTER(FSKDR). CIDE is the global control bit to enable/disable FSK decoder, alert tone detector and DTMF receiver. However, the ring detector is always active.



PS: The signals noted in italic and underline type are CID pins on the chip.

Figure 6-17 The CID Block Diagram