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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	3.6MHz
Connectivity	Serial Port
Peripherals	LCD, POR, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-QFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w925g625

3. PIN CONFIGURATION

Figure 3-1 shows the pin assignment. The package type is 160pin QFP.

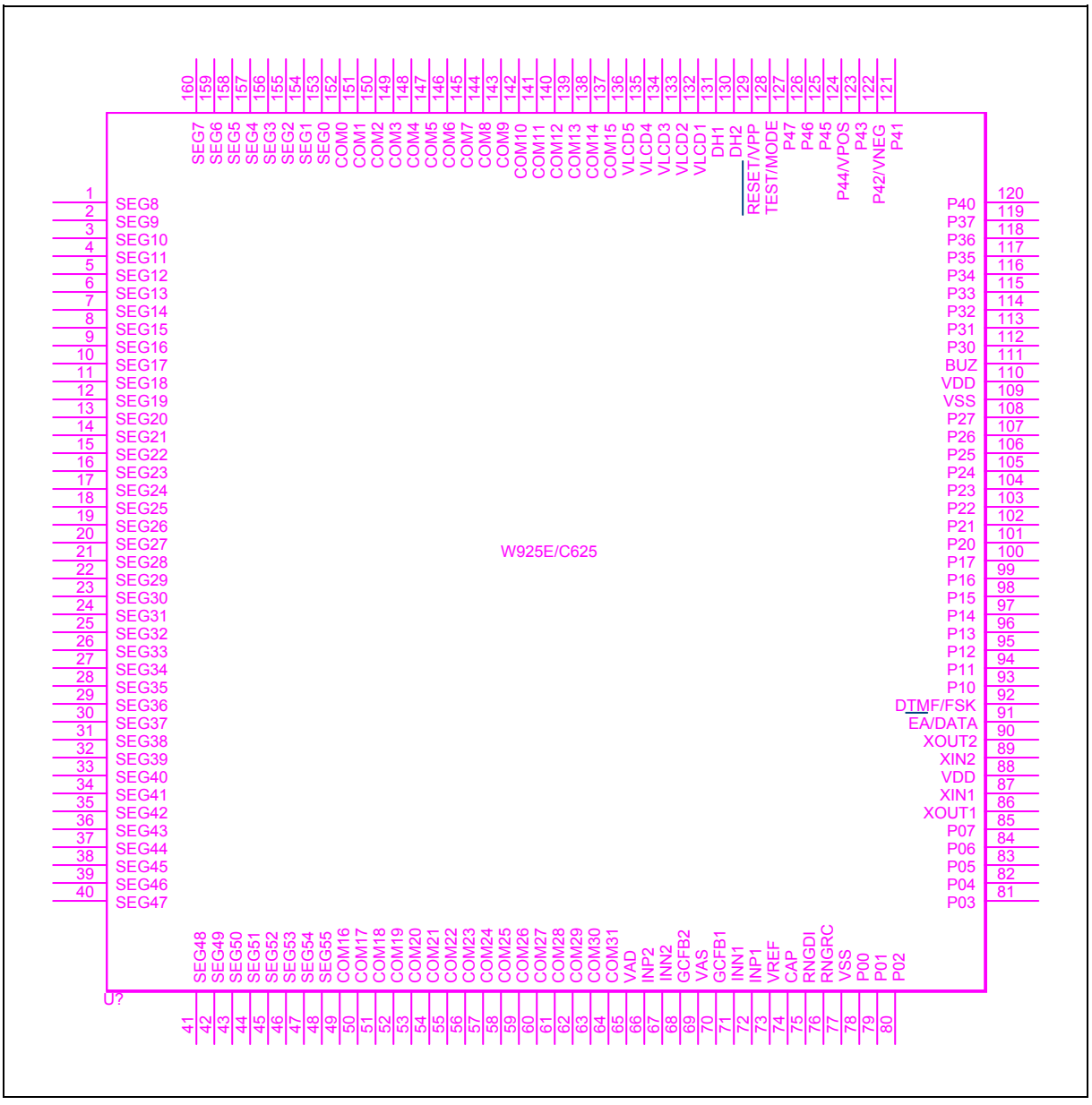


Figure 3-1 W925E/C625 Pin Configuration

6. FUNCTIONAL DESCRIPTION

The W925E/C625 is an 8-bit micro-controller with CID function. The 8-bit micro-control has the same instruction set as the 8051 family, with one addition: DEC DPTR (op-code A5H, the DPTR is decreased by 1). In addition, the W925E/C625 contains on-chip 4K + 224 bytes MOVX RAM.

ROM:

There are 64K bytes EEPROM/MASK ROM. The total 64K bytes EEPROM/MASK ROM is used for program code. The completely 64K bytes EEPROM/MASK ROM can be used for the look-up table memory.

On-chip Data RAM:

The W925E/C625 has 4K normal RAM + 224 Bytes of discontinuity LCD RAM which address is from 0000H to 0FFFH + 2000H to 20FEH. It only can be accessed by MOVX instruction; this on-chip RAM is optional under software control. The 224 bytes of RAM, which no appends to the 4K bytes RAM, are used for LCD RAM. The on-chip data RAM is not used for executable program memory. There is no conflict or overlap among the 256 bytes scratchpad RAM and the 4K Bytes MOVX RAM as they use different addressing modes and separate instructions.

CID:

The CID functions include the FSK decoder, CAS detector, and DTMF decoder and ring detector.

FSK modulator:

Support ITU-T V.23 and Bellcore 202 FSK transmit modulate signal

DTMF modulator:

The W925E/C625 built-in Dual tone multi-frequency generator.

I/O Ports:

The W925E/C625 has five 8-bit I/O ports giving 40 lines. Port0 to Port3 can be used as an 8-bit general I/O port with bit-addressable. The I/O mode of each port are controlled by PxIO registers. Port 1 to Port 4 have internal pull high resistors enabled/disabled by PxH registers. Port0 is open-drain type in output mode.

Serial I/O port:

The serial port, through P4.0 (SCLK) and P4.1 (SDATA), is an 8-bit synchronous serial I/O interface.

Timers:

The W925E/C625 has two 13/16-bit timers or 8 bits auto-reload timers. An independent watchdog timer is used as a System Monitor or as a very long time period timer. A divider can produce the divider interrupt in every period of 0.5S or 0.25S.

Comparator:

The W925E/C625 has an internal comparator with one external analog signal input path VNEG and an external path VPOS or a regulator voltage for the reference input REF1.

LCD:

The LCD display of 1792 dots is 1/5 bias with 56 segments and 32 commons. The LCD display of The LCD voltage is from internal regulator or external voltage source.

TIMER CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

TF1: Timer 1 overflows flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.

TR1: Timer 1 runs control. This bit is set or cleared by software to turn timer on or off.

TF0: Timer 0 overflows flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.

TR0: Timer 0 runs control. This bit is set or cleared by software to turn timer on or off.

IE1: Interrupt 1 edge detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise, it follows the pin.

IT1: Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

IE0: Interrupt 0 edge detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise, it follows the pin.

IT0: Interrupt 0 type control. Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

Bit7~4 control timer 1, bit3~0 control timer0

GATE: Gating control. When this bit is set, Timer x is enabled only while $\overline{INTx}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.

C/$\overline{T}$: Timer or Counter Select. When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin.

Note: X is either 0 or 1.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 13-bits timer
0	1	Mode 1: 16-bits timer
1	0	Mode 2: 8-bits with auto-reload from Thx
1	1	Reserved

T0S0-1&T1S0-1: Timer0 & Timer1 clock source mode select bits. These bits determine the timer0 & timer1 clock source.

T0S1 (T1S1)	T0S0 (T1S0)	Prescale clock source
0	0	$Fosc/2^2$
0	1	$Fosc/2^6$
1	0	$Fosc/2^{10}$
1	1	Fs

DIVS: Divider clock source control bit 1:
DIVS = 0 : $Fs/2^{13}$
DIVS= 1 : $Fs/2^{14}$

$\overline{M}$/S: System clock source control bit : $\overline{M}$/S = 0 : Fosc = XIN1 (F_M)
$\overline{M}$/S = 1 : Fosc = XIN2 (Fs)

CLOCK CONTROL2 (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	ENBUZ	BUZSL	KT1	KT0	-	-	-	-

Mnemonic: CKCON2 Address: 8Fh

ENBUZ: When ENBUZ=1 the BUZ pin works as buzzer output, otherwise BUZ pin is in floating state.

BUZSL: Buzzer output selection. When BUZSL=0 BUZ is the output of octave tone. When BUZZL=1, BUZ is the output of key tone.

KT1-0: Key tone frequency sources from divider. When divider is enable, KT1 and KT0 determines the key tone frequency.

KT1	KT0	KEY TONE FREQUENCY
0	0	Low
0	1	512Hz
1	0	1024Hz
1	1	2048Hz

PORT 1 (initial=FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: P1 can be selected as input or output mode by the P1IO register, at initial reset, P1IO is set to 1, so P1 is used as input mode . When P1IO is set to 0, the P1 is used as CMOS output mode. When P1EF are set and P1IO are set as input mode, P1 can be used as external interrupt source. The functions are listed below.

P2 PULL-HIGH CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	P2.7H	P2.6H	P2.5H	P2.4H	P2.3H	P2.2H	P2.1H	P2.0H

Mnemonic: P2H Address: 9Eh

P2H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

P3 PULL-HIGH CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	P3.7H	P3.6H	P3.5H	P3.4H	P3.3H	P3.2H	P3.1H	P3.0H

Mnemonic: P3H Address: 9Fh

P3H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

PORT 2 (initial=FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is an I/O port with internal pull-high resistor. P2 can be selected as input or output mode by the P2IO register. At initial reset, P2 is used as input mode. When P2IO is set to 0, P2 is used as CMOS output mode.

HIGH BYTE REGISTER (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	HB.7	HB.6	HB.5	HB.4	HB.3	HB.2	HB.1	HB.0

Mnemonic: HB Address: A1h

This register contains the high byte address during execution of " MOVX @Ri, " instructions.

P4 PULL-HIGH CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	P4.7H	P4.6H	P4.5H	P4.4H	P4.3H	P4.2H	P4.1H	P4.0H

Mnemonic: P4H Address: A2h

P4H: Port4 pins pull-high resistor enable/disable

1: enable

0: disable

CAS TONE PRESENT TIME REGISTER (initial=0FH)

Bit:	7	6	5	4	3	2	1	0
	CASPT7	CASPT6	CASPT5	CASPT4	CASPT3	CASPT2	CASPT1	CASPT0

Mnemonic: CASPT Address: Beh

The clock period of guard-time timer is 0.8582Ms. The default alert tone present time is 12.87Ms.

CASPT7-0: The pre-set data register for counting CAS tone present time. When CAS tone is detected (ALGR low to high), the guard timer starts to up-count from 00H. As the guard timer is equal to the value of CASPT, the exist of the CAS tone is accepted. ALGR changes to low state to stop and reset the counter.

CAS TONE ABSENT TIME REGISTER (initial=0FH)

Bit:	7	6	5	4	3	2	1	0
	CASAT7	CASAT6	CASAT5	CASAT4	CASAT3	CASAT2	CASAT1	CASAT0

Mnemonic: CASAT Address: BFh

The clock period of guard-time timer is 0.8582Ms. The default alert tone absent time is 12.87Ms.

CASAT7-0: The pre-set data register for counting CAS tone absent time. When CAS tone is absent (ALGR high to low), the guard timer starts to up-count from 00H. As the guard timer is equal to the value of CASAT, the finish of CAS tone is recognized. ALGR changes to high state to stop and reset the counter.

SERIAL PORT CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	SF1	LCDON	REGON	REN1	SFQ	SEDG	CLKIO	SIO

Mnemonic: SCON1 Address: C0h

SF1: Serial port interrupt flag. When 8-bits data transited completely, SF1 is set by hardware. SF1 is cleared when serial interrupt routine is executed or cleared by software.

LCDON: LCD waveform enable control. 0 to Disable LCD display, 1 to Enable LCD display.

REGON: Regulator on/off control. 0 to disable regulator, 1 to regulator.

REN1: Set REN1 from 0 to 1 to start the serial port1 to receive 8-bit serial data.

SFQ: SFQ=0 Serial clock output frequency is equal to f_{OSC} /2

SFQ=1 Serial clock output frequency is equal to f_{OSC} /256

SEDG: SEDG=0 Serial data latched at falling edge of clock, SCLK=Low initially.

SEDG=1 Serial data latched at rising edge of clock, SCLK=High initially.

CLKIO: CLKIO=0 P4.0(SCLK) work as output mode

CLKIO=1 P4.0(SCLK) work as input mode

SIO: SIO=0 P4.0 & P4.1 work as normal I/O pin

SIO=1 P4.0 & P4.1 work as Serial port1 function

WATCHDOG CONTROL (initial: note)

Bit:	7	6	5	4	3	2	1	0
	-	POR	-	WFS	WDIF	WTRF	EWT	RWT

Mnemonic: WDCON Address: D8h

POR: Power-on reset flag. Hardware will set this flag when system is powered on and this flag is cleared only by software.

WFS: Watchdog Timer Frequency Select. Set to select F_S as WDT clock input. Clear to select F_{OSC} as WDT clock input.

WDIF: Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the watchdog timer. If the Watchdog interrupt is enabled (EIE.5), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WTRF: Watchdog Timer Reset Flag. Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no effect on this bit.

EWT: Enable Watchdog timer Reset. Setting this bit will enable the Watchdog timer Reset function.

RWT: Reset Watchdog Timer. This bit helps in putting the watchdog timer into a known state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.5) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing by hardware.

Note: The WDCON SFR is set to a 0x000xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is set to 0 on a Power-on reset and unaffected by other resets.

ACCUMULATOR (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0: The ACC register.

EXTENDED INTERRUPT ENABLE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	EWDI	ECOMP	EDIV	ECID	EX3	EX2

Mnemonic: EIE Address: E8h

EIE.7-6:Reserved bits.

EWDI: Enable Watchdog timer interrupt.

ECOMP: Enable comparator interrupt.

EDIV: Enable Divider interrupt.

ECID: Enable CID interrupt.

Table 3. Instruction Timing for W925E/C625, continued

INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES	INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES
DJNZ R5, rel	DD	2	3	MOV R7, A	FF	1	1
DJNZ R6, rel	DE	2	3	MOV R0, direct	A8	2	2
DJNZ R7, rel	DF	2	3	MOV R1, direct	A9	2	2
DJNZ direct, rel	D5	3	4	MOV R2, direct	AA	2	2
INC A	04	1	1	MOV R3, direct	AB	2	2
INC R0	08	1	1	MOV R4, direct	AC	2	2
INC R1	09	1	1	MOV R5, direct	AD	2	2
INC R2	0A	1	1	MOV R6, direct	AE	2	2
INC R3	0B	1	1	MOV R7, direct	AF	2	2
INC R4	0C	1	1	MOV R0, #data	78	2	2
INC R5	0D	1	1	MOV R1, #data	79	2	2
INC R6	0E	1	1	MOV R2, #data	7A	2	2
INC R7	0F	1	1	MOV R3, #data	7B	2	2
INC @R0	06	1	1	MOV R4, #data	7C	2	2
INC @R1	07	1	1	MOV R5, #data	7D	2	2
INC direct	05	2	2	MOV R6, #data	7E	2	2
INC DPTR	A3	1	2	MOV R7, #data	7F	2	2
JMP @A+DPTR	73	1	2	MOV @R0, A	F6	1	1
JZ rel	60	2	3	MOV @R1, A	F7	1	1
JNZ rel	70	2	3	MOV @R0, direct	A6	2	2
MOV @R1, direct	A7	2	2	RL A	23	1	1
MOV @R0, #data	76	2	2	RLC A	33	1	1
MOV @R1, #data	77	2	2	RR A	03	1	1
MOV direct, A	F5	2	2	RRC A	13	1	1
MOV direct, R0	88	2	2	SETB C	D3	1	1
MOV direct, R1	89	2	2	SETB bit	D2	2	2
MOV direct, R2	8A	2	2	SWAP A	C4	1	1
MOV direct, R3	8B	2	2	SJMP rel	80	2	3
MOV direct, R4	8C	2	2	SUBB A, R0	98	1	1
MOV direct, R5	8D	2	2	SUBB A, R1	99	1	1
MOV direct, R6	8E	2	2	SUBB A, R2	9A	1	1
MOV direct, R7	8F	2	2	SUBB A, R3	9B	1	1
MOV direct, @R0	86	2	2	SUBB A, R4	9C	1	1
MOV direct, @R1	87	2	2	SUBB A, R5	9D	1	1
MOV direct, direct	85	3	3	SUBB A, R6	9E	1	1
MOV direct, #data	75	3	3	SUBB A, R7	9F	1	1
MOV DPTR, #data 16	90	3	3	SUBB A, @R0	96	1	1
The CPE designer may choose to set	93	1	2	SUBB A, @R1	97	1	1
The CPE designer may choose to set	83	1	2	SUBB A, direct	95	2	2

service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts INT2 to INT3 are edge triggered only.

The TF0, TF1 flags generate the Timer 0, 1 Interrupts. These flags are set by the overflow in the Timer 0, Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog timer interrupt flag WDIF (WDCON.3) is set. If the enable bit EIE.5 enables the interrupt, then an interrupt will occur.

The Serial block can generate interrupts on reception or transmission. There are one interrupt sources from the Serial block, which are obtained by SF1 in the SCON1. SF1 is cleared automatically when the serial port interrupt is serviced.

The divider interrupt is generated by DIVF that is set when divider overflows. DIVF is set by hardware and cleared when divider interrupt is serviced. The divider interrupt is enable/disable if the bit EDIV is high/low.

The comparator interrupt is produced by COMPF, which is set when the RESC bit is changed from low to high. RESC, which is the real-time result of comparator, set when the voltage of reference input is higher than the voltage of analog input.

The CID interrupt is generated by CIDF. The CIDF is a logic OR output of all CID flags which are set by hardware and cleared by software. The structure of the CID flags is shown in Figure 6-4.

Each of the individual interrupts can be enabled or disabled by setting or clearing the corresponding bits in the IE and EIE SFR. A bit EA, which is located in IE.7, is a global control bit to enable/disable the all interrupt. When bit EA is zero all interrupts are disable and when bit EA is high each interrupt is enable individually by the corresponding bit.

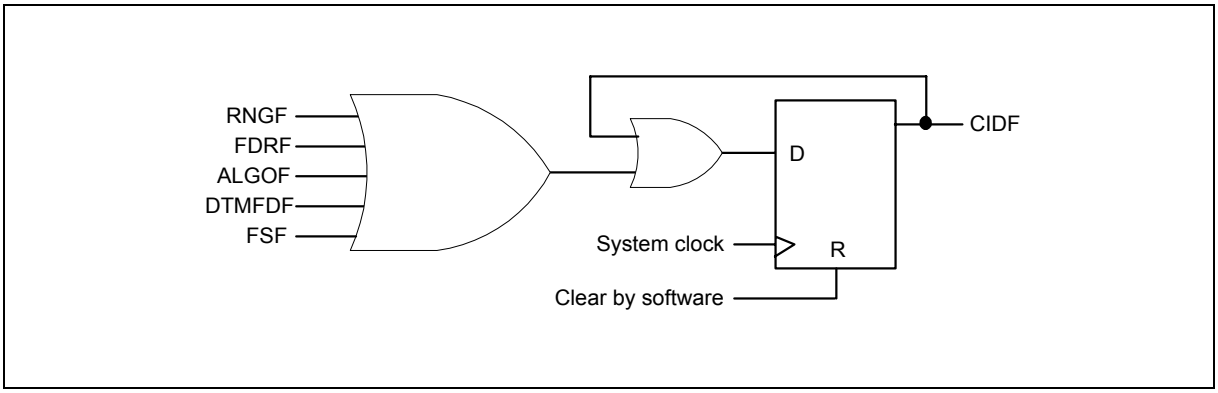


Figure 6-4 The Structure of CID Flags

Priority Level Structure

There are two priority levels for the interrupts, high and low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.

6.10 Comparator

A built-in comparator to compare the analog signal. There is a analog input paths from pin VNEG. Two reference inputs, one is from pin VPOS and other is from regulator output. When the voltage of positive input is higher than the negative input, the comparator output will be high. The RESEC(COMPR.3) is the result of the comparison. An internal rising signal on RESC produces interrupt flag of COMPF (EXIF.4). The flag COMPF is cleared when comparator interrupt routine is executed or cleared by software. Set COMPEN to enable the comparator function.

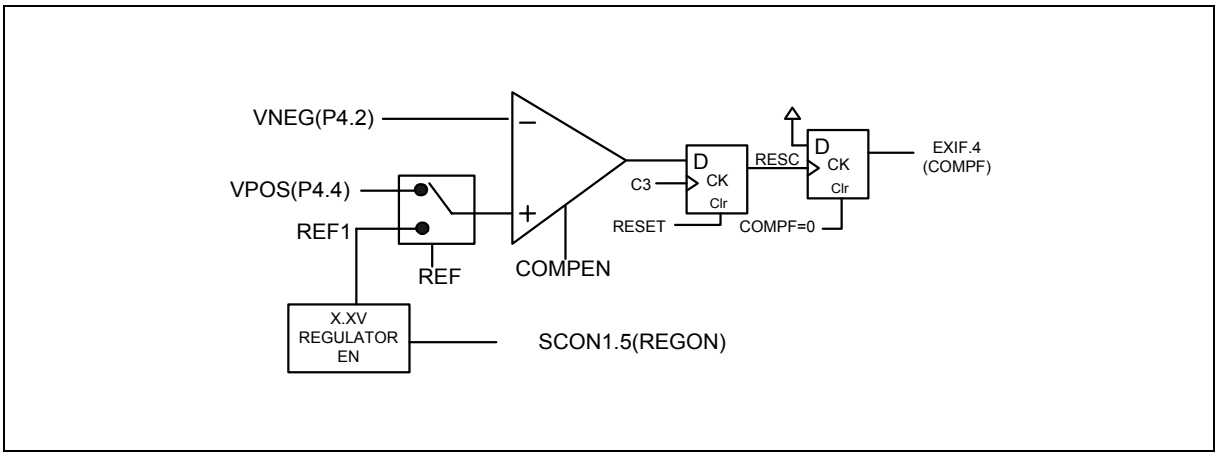
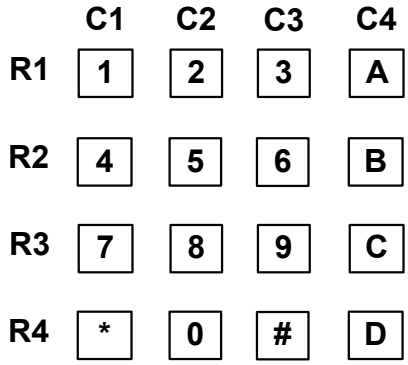


Figure 6-10 The Configuration of Comparator

6.11 DTMF Generator

W925E/C625 provides a DTMF generator which outputs the dual tone multi-frequency signal to the DTMF pin. The DTMF generator can work well at the operating frequency of 3.58MHz. A DTMF generator register DTMFG controls the DTMF output and specifies the desired low/high frequency. The tones are divided into two groups (low group and high group). When the generator is disable, the DTMF pin is in tri-state. The relation between the DTMF signal and the corresponding touch tone keypad is shown in Figure 6-11.



Row/Col	Frequency
R1	697 Hz
R2	770 Hz
R3	852 Hz
R4	941 Hz
C1	1209 Hz
C2	1336 Hz
C3	1477 Hz
C4	1633 Hz

Figure 6-11 The Relation Between DTMF and Keypad

P1: I/O mode is controlled by P1IO. Pull high is controlled by P1H. **P1.0~P1.3 work as INT2**, **P1.4~P1.7 work as INT3**. **Falling edge** on P1 pins to produce INT2 and INT3 flag. P1 is configured as INT2/INT3 by P1EF register.

P2: I/O mode is controlled by P2IO. Pull high is controlled by P2H.

P3: I/O mode is controlled by P3IO. Pull high is controlled by P3H.

P3.5	T1	Timer/counter 1 external count input
P3.4	T0	Timer/counter 0 external count input
P3.3	$\overline{INT1}$	External interrupt 1
P3.2	$\overline{INT0}$	External interrupt 0

P4: I/O mode is controlled by P4IO. Pull high is controlled by P4H.

Special function of P4 is described below.

P4.4	Vpos	Positive input of the comparator
P4.2	Vneg	Negative input of the comparator
P4.1	SDATA	Serial port output
P4.0	SCLK	Serial port input

6.14 Divider

A built-in 13/14-bit binary up-counter designed to generate periodic interrupt. The clock source is from sub-oscillator. When the frequency of sub-crystal is 32768Hz, it provides the divider interrupt in the period of 0.25/0.5 second. Bit DIVS controls the degree of divider. When DIVA is high to enable the divided counter, when DIVA is low to reset divider and stop counting. As the divider overflows, the divider interrupt flag DIVF is set. DIVF is clear by software or serving divider interrupt routine.

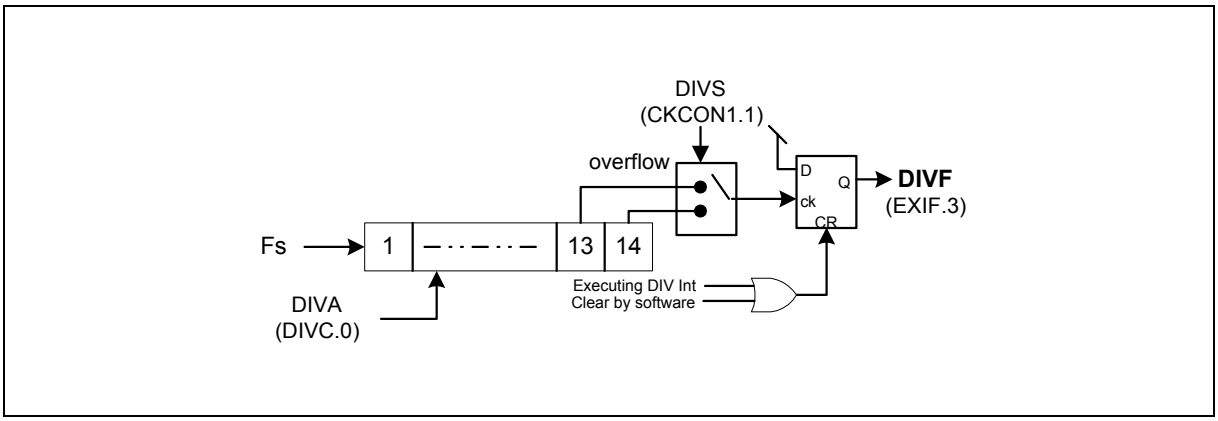


Figure 6-13 13/14-bit Divider

Table7 The relationship between the F_{LCD} and the 2 bits option code

Option Code	00	01	10	11
F_{LCD}	16Hz	32Hz	64Hz	128Hz

LCD RAM MAP

The LCD memory address is list as below. Each dot is controlled by the corresponding bit and the content high to light the LCD dot and low to off the LCD dot.

OUTPUT	S55-S48	S47-S40	S39-S32	S31-S24	S23-S16	S15-S08	S07-S00
	BIT7-0	BIT7-0	BIT7-0	BIT7-0	BIT7-0	BIT7-0	BIT7-0
COM0	2006H	2005H	2004H	2003H	2002H	2001H	2000H
COM1	200EH	200DH	200CH	200BH	200AH	2009H	2008H
COM2	2016H	2015H	2014H	2013H	2012H	2011H	2010H
COM3	201EH	201DH	201CH	201BH	201AH	2019H	2018H
COM4	2026H	2025H	2024H	2023H	2022H	2021H	2020H
COM5	202EH	202DH	202CH	202BH	202AH	2029H	2028H
COM6	2036H	2035H	2034H	2033H	2032H	2031H	2030H
COM7	203EH	203DH	203CH	203BH	203AH	2039H	2038H
COM8	2046H	2045H	2044H	2043H	2042H	2041H	2040H
COM9	204EH	204DH	204CH	204BH	204AH	2049H	2048H
COM10	2056H	2055H	2054H	2053H	2052H	2051H	2050H
COM11	205EH	205DH	205CH	205BH	205AH	2059H	2058H
COM12	2066H	2065H	2064H	2063H	2062H	2061H	2060H
COM13	206EH	206DH	206CH	206BH	206AH	2069H	2068H
COM14	2076H	2075H	2074H	2073H	2072H	2071H	2070H
COM15	207EH	207DH	207CH	207BH	207AH	2079H	2078H
COM16	2086H	2085H	2084H	2083H	2082H	2081H	2080H
COM17	208EH	208DH	208CH	208BH	208AH	2089H	2088H
COM18	2096H	2095H	2094H	2093H	2092H	2091H	2090H
COM19	209EH	209DH	209CH	209BH	209AH	2099H	2098H
COM20	20A6H	20A5H	20A4H	20A3H	20A2H	20A1H	20A0H
COM21	20AEH	20ADH	20ACH	20ABH	20AAH	20A9H	20A8H
COM22	20B6H	20B5H	20B4H	20B3H	20B2H	20B1H	20B0H
COM23	20BEH	20BDH	20BCH	20BBH	20BAH	20B9H	20B8H
COM24	20C6H	20C5H	20C4H	20C3H	20C2H	20C1H	20C0H
COM25	20CEH	20CDH	20CCH	20CBH	20CAH	20C9H	20C8H
COM26	20D6H	20D5H	20D4H	20D3H	20D2H	20D1H	20D0H
COM27	20DEH	20DDH	20DCH	20DBH	20DAH	20D9H	20D8H
COM28	20E6H	20E5H	20E4H	20E3H	20E2H	20E1H	20E0H
COM29	20EEH	20EDH	20ECH	20EBH	20EAH	20E9H	20E8H
COM30	20F6H	20F5H	20F4H	20F3H	20F2H	20F1H	20F0H
COM31	20FEH	20FDH	20FCH	20FBH	20FAH	20F9H	20F8H

LCD Power Connection

The LCD power connection of bias is shown in Figure 6-15

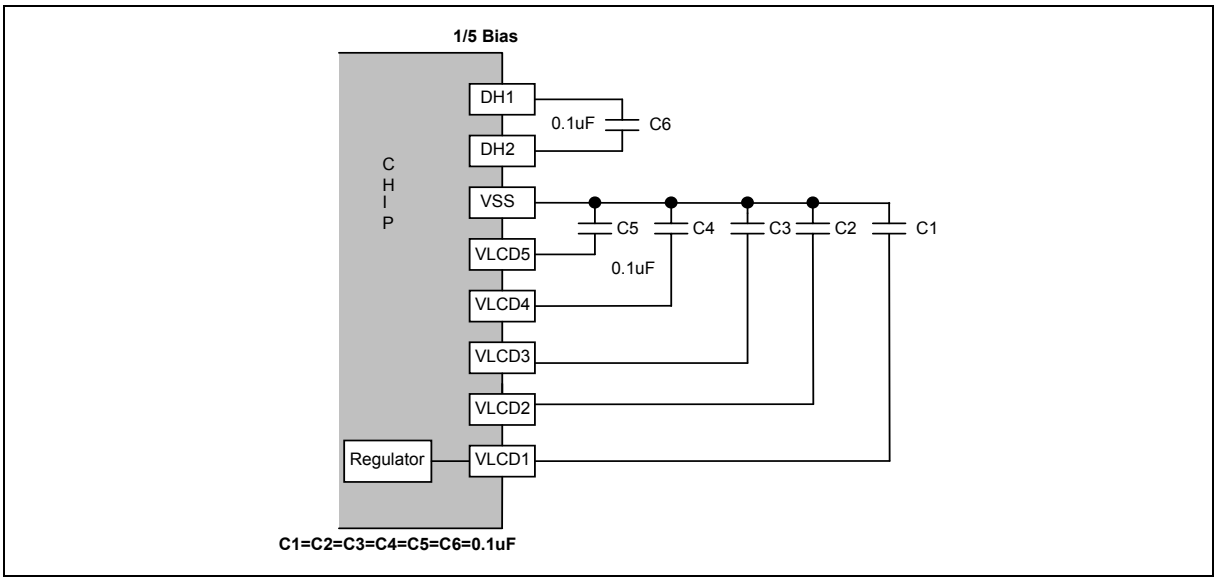


Figure 6-15 1/5 Bias LCD Power Connection

LCD Waveform

The LCD waveform is B type. Figure 6-16 is an example for 1/5 bias LCD waveform.

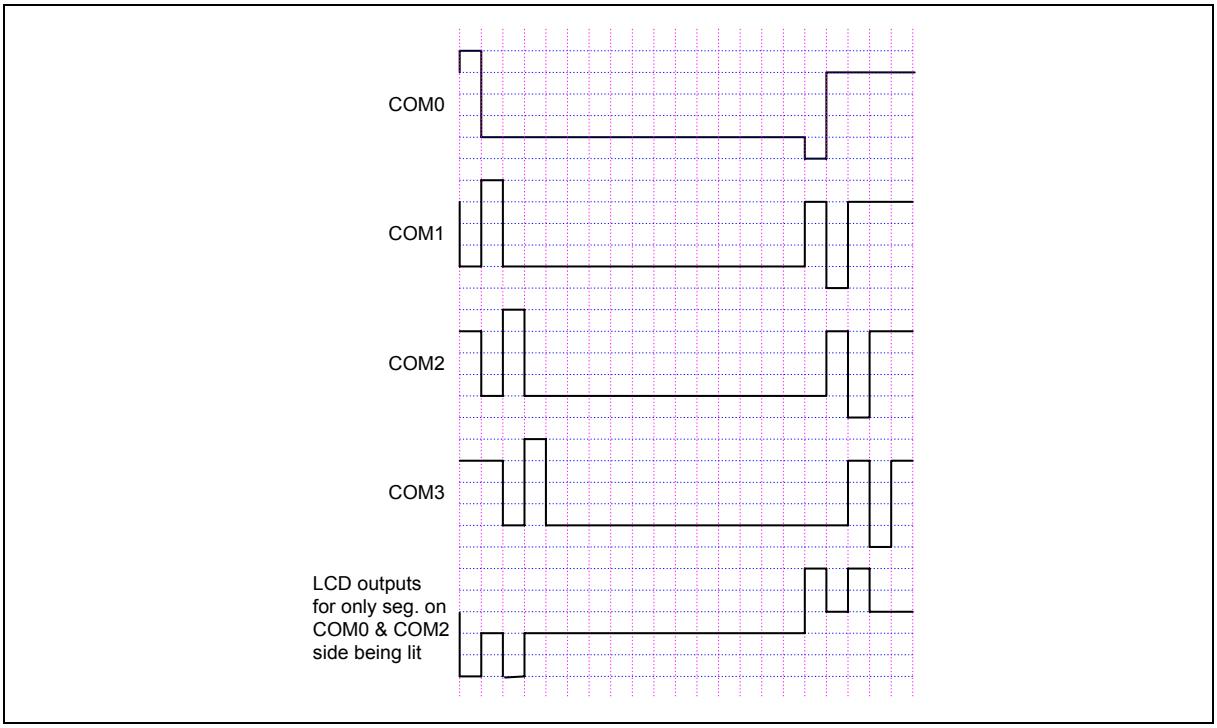


Figure 6-16 LCD waveform for 1/5 bias

Input Pre-Processor

The input signal is processed by Input Pre-Processor, which is comprised of two OP amps and a bias source(VREF). The gain OP-amps are used to bias the input voltage with the VREF signal voltage. VREF is $V_{AD}/2$ typically, this pin is recommended to connect a 0.1 Uf capacitor to V_{AS}. The gain adjustable OP amps are sued to select the input gain by connecting a feedback resistor between GCFB and INN pins. Figure 6-19 shows the differential input configuration and Figure 6-20 shows the single-ended configuration.

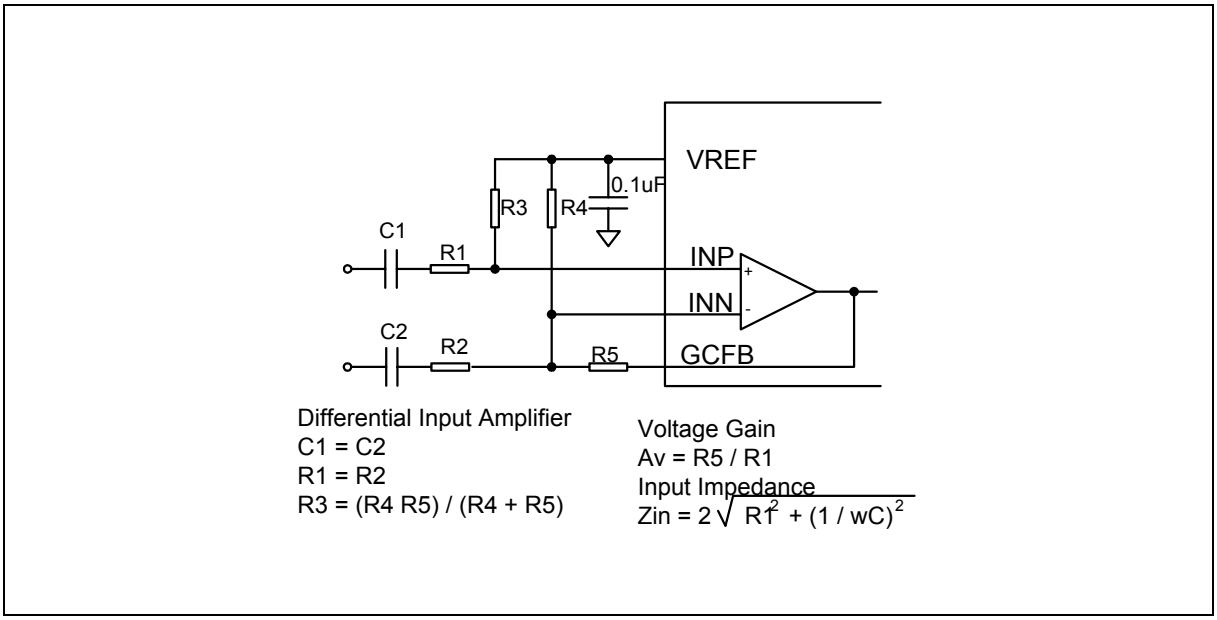


Figure 6-19 Differential Input Gain Control Circuit

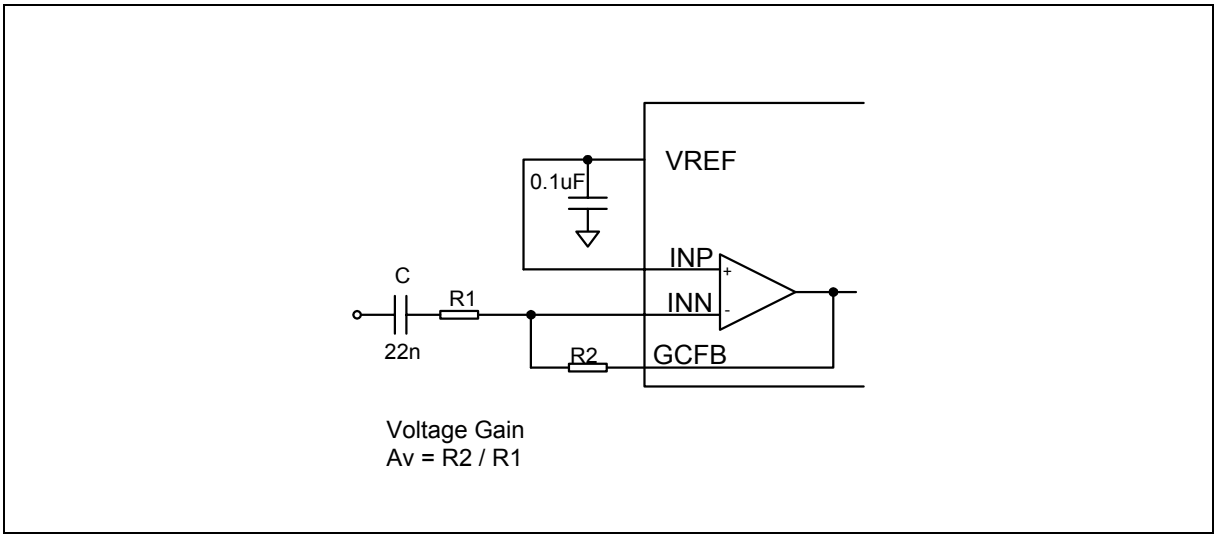


Figure 6-20 Single-Ended Input Gain Control Circuit

IFX OPC-9

DTMFR1

DTMFR1[7:4] are reserved bits and must be 0000b.

BIT3~BIT0	ACCEPTABLE ERROR PERCENTAGE TO SAMPLE 4 PERIOD OF ROW FREQ.
0000	0.6% (default)
0001	2.5%
001X	3.5%
01XX	Reserved
1XXX	Reserved

DTMFR2

BIT3~BIT0	ACCEPTABLE ERROR PERCENTAGE TO SAMPLE 4 PERIOD OF COL FREQ.
0000	0.5% (default)
0001	1.5%
001X	2.5%
01XX	Reserved
1XXX	Reserved

The acceptable error percentage may have small variation by different test environments.

DTMFR2.4=0	DTMF receiver works as a DTMF receiver
DTMFR2.4=1	DTMF receiver works as a tone detector
DTMFR2.5=0	DTMF PT counter is up counter type, change of detected frequency does not effect counter
DTMFR2.5=1	DTMF PT counter is up counter type, change of detected frequency resets DTMF PT counter
DTMFR2.6=0	DTMF AT counter is up-down counter type, up counting when no DTMF detected, down counting if DTMF detected again.
DTMFR2.6=1	DTMF AT counter is up counter type, up counting when no DTMF detected, pause counting if DTMF detected again.
DTMFR2.7: reserved	

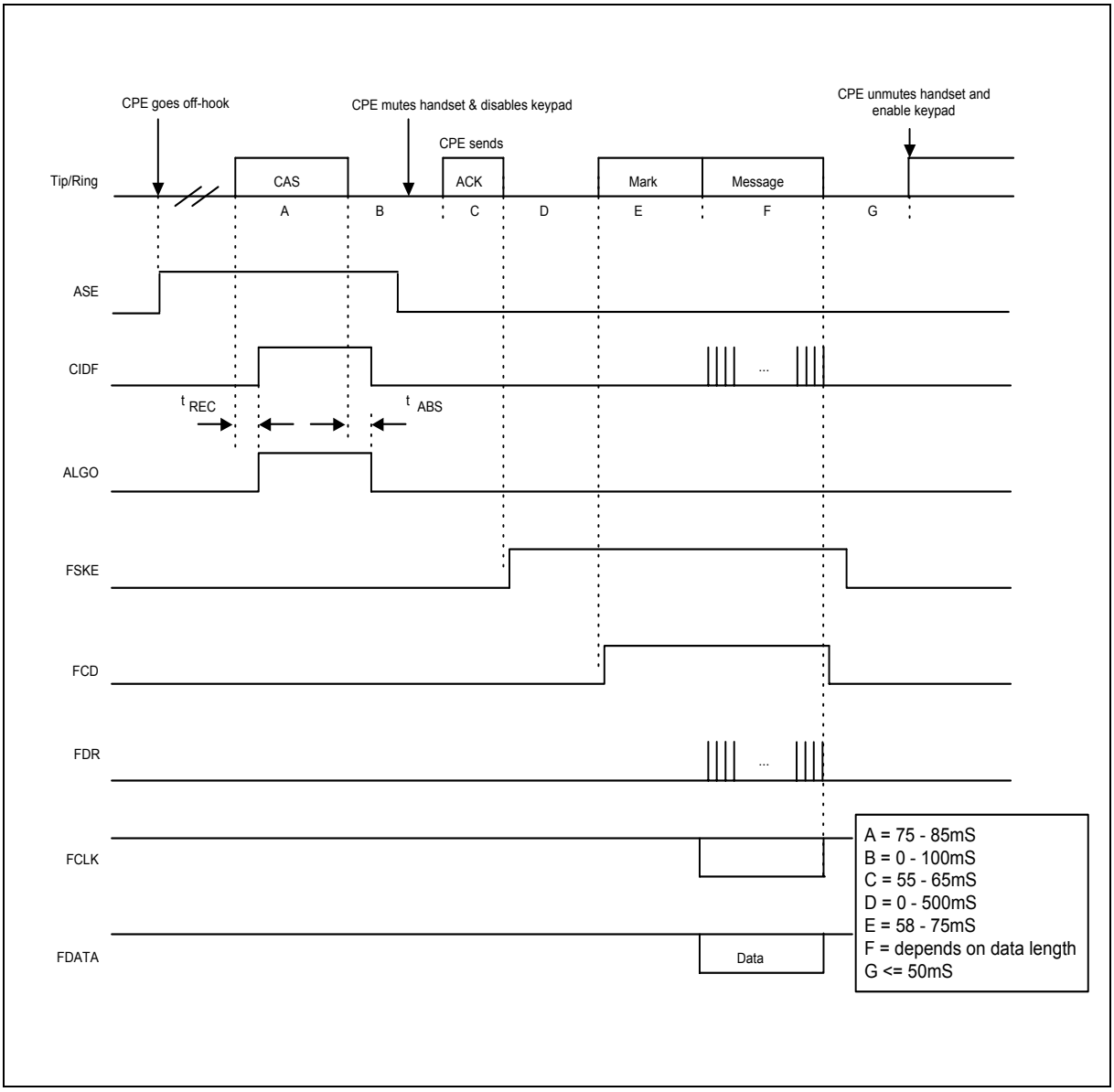


Figure 6-28 Input and Output Timing of Bellcore Off-hook Data Transmission

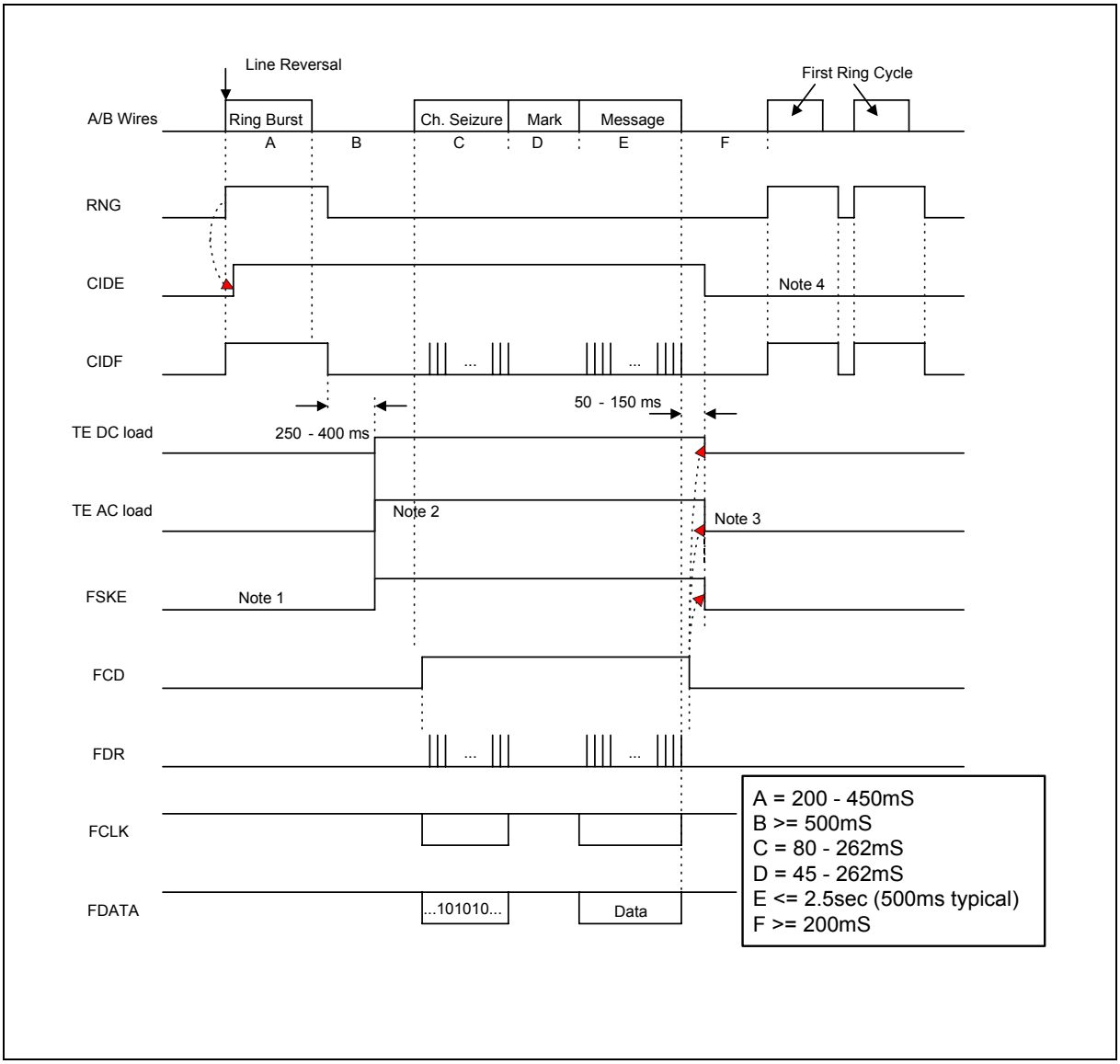


Figure 6-31 Input and Output Timing of CCA Caller Display Service Data Transmission

Notes:

1. The CPE designer may choose to set FSKE always high while the CPE is on-hook and the FSK signal is expected.
2. TW/P & E/312 specifies that the AC and DC loads should be applied between 250 – 400 Ms after the end of the ring burst.
3. TW/P & E/312 specifies that the AC and DC loads should be removed between 50 – 150 ms after the end of the FSK signal.
4. The CID may not be enable up at the first ring cycle after the FSK data had been processed.

7. ELECTRICAL CHARACTERISTICS

7.1 Maximum Ratings*

(Voltage referenced to VSS pin)

	PARAMETER	SYMBOL	RATING	UNITS
1	Supply Voltage with respect to V_{SS}	V_{DD}	-0.3 to 6	V
2	Voltage on any pin other than supplies (note 1)		-0.7 to V_{DD} + 0.7	V
3	Current at any pin other than supplies		0 to 10	MA
4	Storage Temperature	Tst	-65 to 150	℃

Note:

*. Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the lift and reliability of the device.

1. V_{DD} + 0.7 should not excess maximum rating of supply voltage.

7.2 Recommended Operating Conditions

CHARACTERISTICS	SYMBOL	RATING	UNIT
Power Supplies (Analog)	V_{AD}	3.0 to 6.0	V
Power Supplies (Digital) EEPROM(E) type(Depend on option) MASKI type	V_{DD}	 2.4 to 3.6 or 3.0 to 5.5 2.2 to 6.0	V
Main Clock Frequency	f_{OSC}	3.579545	MHz
Sub Clock Frequency	f_{SUB}	32768	Hz
Tolerance on Clock Frequency	Δf_C	-0.1 to +0.1	%
Operation Temperature	T_{op}	0 to 75	°C

7.5 AC Characteristics

(AC timing characteristics supersede the recommended operating conditions unless otherwise stated.)

Dual Tone Alert Signal Detection Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
LOW TONE FREQUENCY	f_L		2130		Hz	
High Tone Frequency	f_H		2750		Hz	
Frequency Deviation accept		1.1			%	3
Frequency Deviation reject		3.5			%	4
Maximum Input Signal Level				0.22	dBm[a]	
INPUT SENSITIVITY PER TONE		-40	-38		dBm	5
Reject Signal Level per tone				-48	dBm	5
Positive and negative twist[b] accept		7			Db	
Noise Tolerance	SNR_{TONE}	20			Db	1, 2

Notes:

a. dBm = decibels with a reference power of 1 Mw into 600 ohms, 0 dBm = 0.7746 Vrms.

b. Twist = 20 log (F_h amplitude / F_l amplitude).

1. Both tones have the same amplitude. Both tones are at the nominal frequencies.
2. Band limited random noise 300 – 3400 Hz. Present only when tone is present.
3. Range within which tones are accepted.
4. Ranges outside of which tones are rejected.
5. These characteristics are at V_{DD} = 5V and temperature = 25 ℃.

Dual Tone Alert Signal Detection

PARAMETER	CONDITION	SYMBOL	MIN.	TYP‡	MAX.	UNITS	NOTES
Alert Signal present detect time	ALGR	t_{DP}	0.5		10	MS	
Alert Signal absent detect time		t_{DA}	0.1		8	MS	

"‡" Typical figure are at V_{DD} = 5V and temperature = 25 ℃ are design aids only, not guaranteed and not subject to production testing.

9. REVISION HISTORY

REVISION	DATE	MODIFICATION
A6	-	1. Add initial state of registers 2. Modify description of WDCON.0 3. Modify Fig6-22
A7	-	1. Modify the μC's operating volt. In Features and Operating Conditions. 2. Modify the PMR initial data 3. Modify the LCD circuit diagram
A8	May 20, 2003	1. Add Fsys Low-speed-clock switch as High-speed-clock application note. Page-27
A9	Mar 1, 2005	1. Modify MOVX instruction machine cycles data.
A10	July 4, 2005	1. Add Lead free package part number. 2. Modify EIF to EXIF.

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