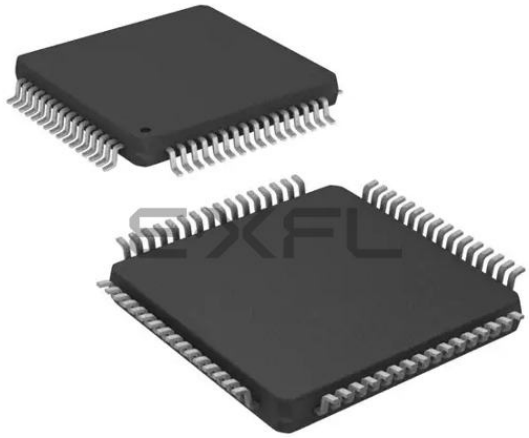
Microchip Technology - PIC18F66J93T-I/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3923 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f66j93t-i-pt

PIC18F87J93 FAMILY

64/80-Pin, High-Performance Microcontrollers with LCD Driver, 12-Bit A/D and nanoWatt Technology

LCD Driver and Keypad Interface Features:

- Direct LCD Panel Drive Capability:
  - Can drive LCD panel while in Sleep mode
- Up to 48 Segments and 192 Pixels, Software Selectable
- Programmable LCD Timing module:
  - Multiple LCD timing sources available
  - Up to four commons: static, 1/2, 1/3 or 1/4 multiplex
  - Static, 1/2 or 1/3 bias configuration
- On-Chip LCD Boost Voltage Regulator for Contrast Control
- Charge Time Measurement Unit (CTMU) for Capacitive Touch Sensing
- ADC for Resistive Touch Sensing

Low-Power Features:

- Power-Managed modes:
  - Run: CPU On, Peripherals On
  - Idle: CPU Off, Peripherals On
  - Sleep: CPU Off, Peripherals Off
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Two Crystal modes, 4-25 MHz
- Two External Clock modes, up to 48 MHz
- 4x Phase Lock Loop (PLL)
- Internal Oscillator Block with PLL:
  - Eight user-selectable frequencies from 31.25 kHz to 8 MHz
- Secondary Oscillator using Timer1 at 32 kHz
- Fail-Safe Clock Monitor (FSCM):
  - Allows for safe shutdown if peripheral clock fails

Peripheral Highlights:

- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)
- Up to Four External Interrupts
- Four 8-Bit/16-Bit Timer/Counter modules
- Two Capture/Compare/PWM (CCP) modules
- Master Synchronous Serial Port (MSSP) module with Two Modes of Operation:
  - 3-Wire/4-Wire SPI (supports all four SPI modes)
  - I^2C™ Master and Slave mode
- One Addressable USART module
- One Enhanced Addressable USART module:
  - LIN/J2602 support
  - Auto-wake-up on Start bit and Break character
  - Auto-Baud Detect (ABD)
- 12-Bit, up to 12-Channel A/D Converter:
  - Auto-acquisition
  - Conversion available during Sleep
- Two Analog Comparators
- Programmable Reference Voltage for Comparators
- Hardware Real-Time Clock and Calendar (RTCC) with Clock, Calendar and Alarm Functions
- Charge Time Measurement Unit (CTMU):
  - Capacitance measurement
  - Time measurement with 1 ns typical resolution

Note: This document is supplemented by the *"PIC18F87J90 Family Data Sheet"* (DS39933). See **Section 1.0 "Device Overview"**.

Device	Flash Program Memory (Bytes)	SRAM Data Memory (Bytes)	I/O	LCD (Pixels)	Timers 8/16-Bit	CCP	MSSP		EUSART AUSART	12-Bit A/D (Channels)	Comparators	BOR/LVD	RTCC	CTMU
							SPI	Master I^2C™						
PIC18F66J93	64K	3,923	51	132	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F67J93	128K	3,923	51	132	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F86J93	64K	3,923	67	192	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F87J93	128K	3,923	67	192	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes

Special Microcontroller Features:

- 10,000 Erase/Write Cycle Flash Program Memory, Typical
- Flash Retention 20 Years, Minimum
- Self-Programmable under Software Control
- Flash Program Memory has Word Write Capability for Data EEPROM Emulators
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug via Two Pins
- Operating Voltage Range: 2.0V to 3.6V
- 5.5V Tolerant Input (digital pins only)
- Selectable Open-Drain Configuration for Serial Communication and CCP Pins for Driving Outputs up to 5V
- On-Chip 2.5V Regulator

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F66J93
- PIC18F67J93
- PIC18F86J93
- PIC18F87J93

Note: This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F87J90 family devices. For information on the features and specifications shared by the PIC18F87J93 family and PIC18F87J90 family devices, see the *"PIC18F87J90 Family Data Sheet"* (DS39933).

The PIC18F87J93 family of devices offers the advantages of all PIC18 microcontrollers – high computational performance, a rich feature set and economical price – with the addition of a versatile, on-chip LCD driver. These features make the PIC18F87J93 family a logical choice for many high-performance applications where price is a primary consideration.

1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F87J93 family implements a 12-bit A/D converter. A/D converters in both families incorporate programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.
- **Data RAM:** The PIC18F87J93 family devices have 3,923 bytes of RAM.

1.2 Details on Individual Family Members

Devices in the PIC18F87J93 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

- Flash Program Memory (64 Kbytes for PIC18FX6J93 devices and 128 Kbytes for PIC18FX7J93).
- LCD Pixels:
  - 64-pin devices – 132 pixels (33 SEGs x 4 COMs)
  - 80-pin devices – 192 pixels (48 SEGs x 4 COMs)
- I/O Ports (seven bidirectional ports on PIC18F6XJ93 devices and nine bidirectional ports on PIC18F8XJ93 devices).

All other features for devices in this family are identical and are summarized in Table 1-1 and Table 1-2.

The devices' block diagrams are given in Figure 1-1 and Figure 1-2.

The pinouts for all devices are listed in Table 1-3 and Table 1-4.

TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
$\overline{MCLR}$	7	I	ST	Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device.
OSC1/CLKI/RA7	39			Oscillator crystal or external clock input.
OSC1		I	CMOS	Oscillator crystal input.
CLKI		I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7		I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	40			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In EC modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.
				PORTA is a bidirectional I/O port.
RA0/AN0	24			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog Input 0.
RA1/AN1/SEG18	23			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog Input 1.
SEG18		O	Analog	SEG18 output for LCD.
RA2/AN2/V_{REF-}	22			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog Input 2.
V_{REF-}		I	Analog	A/D reference voltage (low) input.
RA3/AN3/V_{REF+}	21			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog Input 3.
V_{REF+}		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/SEG14	28			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
SEG14		O	Analog	SEG14 output for LCD.
RA5/AN4/SEG15	27			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog Input 4.
SEG15		O	Analog	SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTE is a bidirectional I/O port.
RE0/LCDBIAS1	2			
RE0		I/O	ST	Digital I/O.
LCDBIAS1		I	Analog	BIAS1 input for LCD.
RE1/LCDBIAS2	1			
RE1		I/O	ST	Digital I/O.
LCDBIAS2		I	Analog	BIAS2 input for LCD.
LCDBIAS3	64	I	Analog	BIAS3 input for LCD.
RE3/COM0	63			
RE3		I/O	ST	Digital I/O.
COM0		O	Analog	COM0 output for LCD.
RE4/COM1	62			
RE4		I/O	ST	Digital I/O.
COM1		O	Analog	COM1 output for LCD.
RE5/COM2	61			
RE5		I/O	ST	Digital I/O.
COM2		O	Analog	COM2 output for LCD.
RE6/COM3	60			
RE6		I/O	ST	Digital I/O.
COM3		O	Analog	COM3 output for LCD.
RE7/CCP2/SEG31	59			
RE7		I/O	ST	Digital I/O.
CCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
SEG31		O	Analog	SEG31 output for LCD.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
$\overline{MCLR}$	9	I	ST	Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device.
OSC1/CLKI/RA7	49			Oscillator crystal or external clock input.
OSC1		I	CMOS	Oscillator crystal input.
CLKI		I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7		I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	50			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In EC modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.
				PORTA is a bidirectional I/O port.
RA0/AN0	30			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog Input 0.
RA1/AN1/SEG18	29			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog Input 1.
SEG18		O	Analog	SEG18 output for LCD.
RA2/AN2/V_{REF-}	28			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog Input 2.
V_{REF-}		I	Analog	A/D reference voltage (low) input.
RA3/AN3/V_{REF+}	27			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog Input 3.
V_{REF+}		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/SEG14	34			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
SEG14		O	Analog	SEG14 output for LCD.
RA5/AN4/SEG15	33			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog Input 4.
SEG15		O	Analog	SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTE is a bidirectional I/O port.
RE0/LCDBIAS1	4			
RE0		I/O	ST	Digital I/O.
LCDBIAS1		I	Analog	BIAS1 input for LCD.
RE1/LCDBIAS2	3			
RE1		I/O	ST	Digital I/O.
LCDBIAS2		I	Analog	BIAS2 input for LCD.
LCDBIAS3	78	I	Analog	BIAS3 input for LCD.
RE3/COM0	77			
RE3		I/O	ST	Digital I/O.
COM0		O	Analog	COM0 output for LCD.
RE4/COM1	76			
RE4		I/O	ST	Digital I/O.
COM1		O	Analog	COM1 output for LCD.
RE5/COM2	75			
RE5		I/O	ST	Digital I/O.
COM2		O	Analog	COM2 output for LCD.
RE6/COM3	74			
RE6		I/O	ST	Digital I/O.
COM3		O	Analog	COM3 output for LCD.
RE7/CCP2/SEG31	73			
RE7		I/O	ST	Digital I/O.
CCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
SEG31		O	Analog	SEG31 output for LCD.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTF is a bidirectional I/O port.
RF1/AN6/C2OUT/SEG19	23			
RF1		I/O	ST	Digital I/O.
AN6		I	Analog	Analog Input 6.
C2OUT		O	—	Comparator 2 output.
SEG19		O	Analog	SEG19 output for LCD.
RF2/AN7/C1OUT/SEG20	18			
RF2		I/O	ST	Digital I/O.
AN7		I	Analog	Analog Input 7.
C1OUT		O	—	Comparator 1 output.
SEG20		O	Analog	SEG20 output for LCD.
RF3/AN8/SEG21/C2INB	17			
RF3		I/O	ST	Digital I/O.
AN8		I	Analog	Analog Input 8.
SEG21		O	Analog	SEG21 output for LCD.
C2INB		I	Analog	Comparator 2 input B.
RF4/AN9/SEG22/C2INA	16			
RF4		I/O	ST	Digital I/O.
AN9		I	Analog	Analog Input 9.
SEG22		O	Analog	SEG22 output for LCD.
C2INA		I	Analog	Comparator 2 input A.
RF5/AN10/CV$_{REF}$/ SEG23/C1INB	15			
RF5		I/O	ST	Digital I/O.
AN10		I	Analog	Analog Input 10.
CV$_{REF}$		O	Analog	Comparator reference voltage output.
SEG23		O	Analog	SEG23 output for LCD.
C1INB		I	Analog	Comparator 1 input B.
RF6/AN11/SEG24/C1INA	14			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog Input 11.
SEG24		O	Analog	SEG24 output for LCD.
C1INA		I	Analog	Comparator 1 input A.
RF7/AN5/$\overline{SS}$/SEG25	13			
RF7		I/O	ST	Digital I/O.
AN5		O	Analog	Analog Input 5.
$\overline{SS}$		I	TTL	SPI slave select input.
SEG25		O	Analog	SEG25 output for LCD.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V$_{DD}$)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTH is a bidirectional I/O port.
RH0/SEG47	79			
RH0		I/O	ST	Digital I/O.
SEG47		O	Analog	SEG47 output for LCD.
RH1/SEG46	80			
RH1		I/O	ST	Digital I/O.
SEG46		O	Analog	SEG46 output for LCD.
RH2/SEG45	1			
RH2		I/O	ST	Digital I/O.
SEG45		O	Analog	SEG45 output for LCD.
RH3/SEG44	2			
RH3		I/O	ST	Digital I/O.
SEG44		O	Analog	SEG44 output for LCD.
RH4/SEG40	22			
RH4		I/O	ST	Digital I/O.
SEG40		O	Analog	SEG40 output for LCD.
RH5/SEG41	21			
RH5		I/O	ST	Digital I/O.
SEG41		O	Analog	SEG41 output for LCD.
RH6/SEG42	20			
RH6		I/O	ST	Digital I/O.
SEG42		O	Analog	SEG42 output for LCD.
RH7/SEG43	19			
RH7		I/O	ST	Digital I/O.
SEG43		O	Analog	SEG43 output for LCD.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

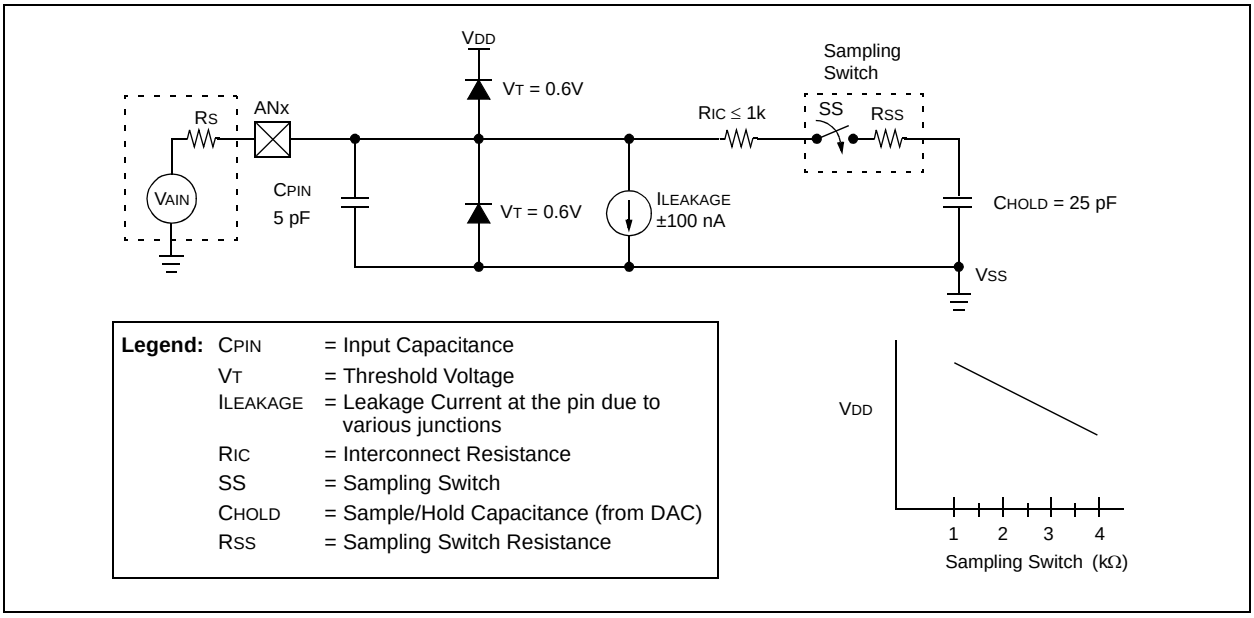
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to do an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins, voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D acquisition time (ADCON2)
   - Select A/D conversion clock (ADCON2)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
   - Set GO/DONE bit (ADCON0<1>)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/DONE bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear ADIF bit, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before next acquisition starts.

FIGURE 2-2: ANALOG INPUT MODEL



2.2 Selecting and Configuring Automatic Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set.

When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This occurs when the ACQT<2:0> bits (ADCON2<5:3>) remain in their Reset state ('000') and is compatible with devices that do not offer programmable acquisition times.

If desired, the ACQT bits can be set to select a programmable acquisition time for the A/D module. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 11 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible but greater than the minimum TAD.

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-1: TAD VS. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Maximum Device Frequency
Operation	ADCS<2:0>	
2 TOSC	000	2.86 MHz
4 TOSC	100	5.71 MHz
8 TOSC	001	11.43 MHz
16 TOSC	101	22.86 MHz
32 TOSC	010	40.0 MHz
64 TOSC	110	40.0 MHz
RC(2)	x11	1.00 MHz(1)

Note 1: The RC source has a typical TAD time of 4 μs.

2: For device frequencies above 1 MHz, the device must be in Sleep mode for the entire conversion or the A/D accuracy may be out of specification.

2.4 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

Note 1: When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will be accurately converted.

2: Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

2.7 A/D Converter Calibration

The A/D converter in the PIC18F87J93 family of devices includes a self-calibration feature which compensates for any offset generated within the module. The calibration process is automated and is initiated by setting the ADCAL bit (ADCON0<7>). The next time the GO/$\overline{\text{DONE}}$ bit is set, the module will perform a "dummy" conversion (which means it is reading none of the input channels) and store the resulting value internally to compensate for offset. Thus, subsequent offsets will be compensated.

The calibration process assumes that the device is in a relatively steady-state operating condition. If A/D calibration is used, it should be performed after each device Reset or if there are other major changes in operating conditions.

2.8 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ACQT<2:0> and ADCS<2:0> bits in ADCON2 should be updated in accordance with the power-managed mode clock that will be used. After the power-managed mode is entered (either of the power-managed Run modes), an A/D acquisition or conversion may be started. Once an acquisition or conversion is started, the device should continue to be clocked by the same power-managed mode clock source until the conversion has been completed. If desired, the device may be placed into the corresponding power-managed Idle mode during the conversion.

If the power-managed mode clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D RC clock to be selected. If bits, ACQT<2:0>, are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN and SCSx bits in the OSCCON register must have already been cleared prior to starting the conversion.

TABLE 2-2: SUMMARY OF A/D REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	**2**
PIR1	—	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	**2**
PIE1	—	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	**2**
IPR1	—	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	**2**
PIR3	—	LCDIF	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	RTCCIF	**2**
PIE3	—	LCDIE	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE	**2**
IPR3	—	LCDIP	RC2IP	TX2IP	CTMUIP	CCP2IP	CCP1IP	RTCCIP	**2**
ADRESH	A/D Result Register High Byte								**2**
ADRESL	A/D Result Register Low Byte								**2**
ADCON0	ADCAL	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	**2**
ADCON1	TRIGSEL	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	**2**
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	**2**
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	**2**
PORTA	RA7**(1)**	RA6**(1)**	RA5	RA4	RA3	RA2	RA1	RA0	**2**
TRISA	TRISA7**(1)**	TRISA6**(1)**	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	**2**
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	—	**2**
TRISF	TRISF5	TRISF4	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	—	**2**

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: RA<7:6> and their associated latch and direction bits are configured as port pins only when the internal oscillator is selected as the default clock source (FOSC2 Configuration bit = 0); otherwise, they are disabled and these bits read as '0'.

2: For these Reset values, see **Section 4.0 "Reset"** of the *"PIC18F87J90 Family Data Sheet"* (DS39933).

REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F87J93 FAMILY DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:
R = Read-only bit

bit 7-5 **DEV<2:0>:** Device ID bits

111 = PIC18F87J93
110 = PIC18F86J93
011 = PIC18F67J93
010 = PIC18F66J93

bit 4-0 **REV<4:0>:** Revision ID bits

These bits are used to indicate the device revision.

REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F87J93 FAMILY DEVICES

R	R	R	R	R	R	R	R
DEV10(1)	DEV9(1)	DEV8(1)	DEV7(1)	DEV6(1)	DEV5(1)	DEV4(1)	DEV3(1)
bit 7							bit 0

Legend:
R = Read-only bit

bit 7-0 **DEV<10:3>:** Device ID bits(1)

These bits are used with the DEV<2:0> bits in the Device ID Register 1 to identify the part number.

0101 0000 = PIC18F87J93 family devices

Note 1: The values for DEV<10:3> may be shared with other device families. The specific device is always identified by using the entire DEV<10:0> bit sequence.

4.0 ELECTRICAL CHARACTERISTICS

Note: Other than some basic data, this section documents only the PIC18F87J93 family devices' specifications that differ from those of the PIC18F87J90 family devices. For detailed information on the electrical specifications shared by the PIC18F87J93 family and PIC18F87J90 family devices, see the *"PIC18F87J90 Family Data Sheet"* (DS39933).

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +100°C
Storage temperature ..... -65°C to +150°C
Voltage on any digital only I/O pin or $\overline{MCLR}$ with respect to V_{SS} (except V_{DD}) ..... -0.3V to 6.0V
Voltage on any combined digital and analog pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on V_{DDCORE} with respect to V_{SS} ..... -0.3V to 2.75V
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to 3.6V
Total power dissipation **(Note 1)** 1.0W
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin ..... 250 mA
Maximum output current sunk by PORTA<7:6> and any PORTB and PORTC I/O pins ..... 25 mA
Maximum output current sunk by any PORTD, PORTE and PORTJ I/O pins ..... 8 mA
Maximum output current sunk by PORTA<5:0> and any PORTF, PORTG and PORTH I/O pins ..... 2 mA
Maximum output current sourced by PORTA<7:6> and any PORTB and PORTC I/O pins ..... 25 mA
Maximum output current sourced by any PORTD, PORTE and PORTJ I/O pins ..... 8 mA
Maximum output current sourced by PORTA<5:0> and any PORTF, PORTG and PORTH I/O pins ..... 2 mA
Maximum current sunk by all ports combined ..... 200 mA

Note 1: Power dissipation is calculated as follows:
$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.0 PACKAGING INFORMATION

For packaging information, see the *"PIC18F87J93 Family Data Sheet"* (DS39933).

NOTES:

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (such as the PIC16C5X) to an Enhanced MCU device (such as the PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Local Sales Office
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- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

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Device: PIC18F87J93 Family Literature Number: DS39948A

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain purchasing information such as pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device[1,2]	PIC18F66J93, PIC18F66J93T PIC18F67J93, PIC18F67J93T PIC18F86J93, PIC18F86J93T PIC18F87J93, PIC18F87J93T
Temperature Range	I = -40°C to +85°C (Industrial)
Package	PT = TQFP (Thin Quad Flatpack)
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18F87J93-I/PT 301 = Industrial temperature, TQFP package, QTP pattern #301.

b) PIC18F87J93T-I/PT = Tape and reel, Industrial temperature, TQFP package.

Note 1: F = Standard Voltage Range
2: T = In Tape and Reel