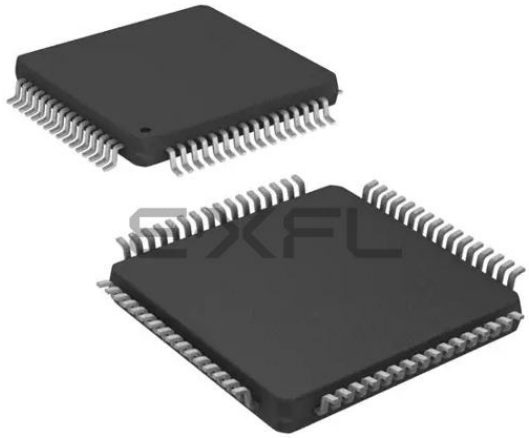


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 128KB (64K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 3923 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f67j93t-i-pt |

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE**.** Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

**Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, nanoWatt XLP, Omniscient Code Generation, PICC, PICC-18, PICkit, PICDEM, PICDEM.net, PICtail, PIC$^{32}$ logo, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

### Special Microcontroller Features:

- 10,000 Erase/Write Cycle Flash Program Memory, Typical
- Flash Retention 20 Years, Minimum
- Self-Programmable under Software Control
- Flash Program Memory has Word Write Capability for Data EEPROM Emulators
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug via Two Pins
- Operating Voltage Range: 2.0V to 3.6V
- 5.5V Tolerant Input (digital pins only)
- Selectable Open-Drain Configuration for Serial Communication and CCP Pins for Driving Outputs up to 5V
- On-Chip 2.5V Regulator

 © 2009 Microchip Technology Inc.

## Table of Contents

**TABLE 1-1: DEVICE FEATURES FOR THE PIC18F6XJ93 (64-PIN DEVICES)**

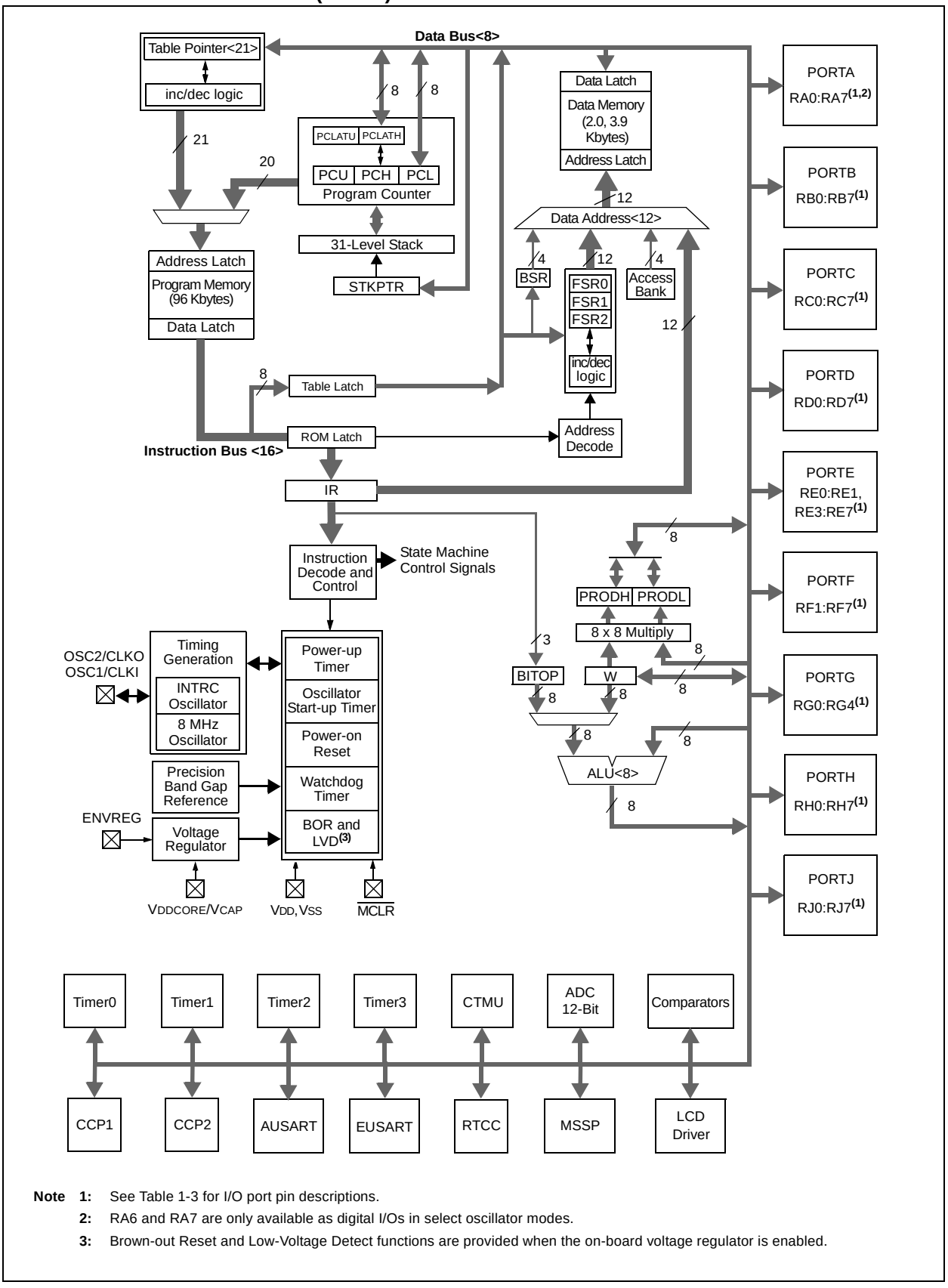
| Features | PIC18F66J93 | PIC18F67J93 |
|---|---|---|
| Operating Frequency | DC – 48 MHz | |
| Program Memory (Bytes) | 64K | 128K |
| Program Memory (Instructions) | 32,768 | 65,536 |
| Data Memory (Bytes) | 3,923 | 3,923 |
| Interrupt Sources | 29 | |
| I/O Ports | Ports A, B, C, D, E, F, G | |
| LCD Driver (available pixels to drive) | 132 (33 SEGs x 4 COMs) | |
| Timers | 4 | |
| Comparators | 2 | |
| CTMU | Yes | |
| RTCC | Yes | |
| Capture/Compare/PWM Modules | 2 | |
| Serial Communications | MSSP, Addressable USART, Enhanced USART | |
| 12-Bit Analog-to-Digital Module | 12 Input Channels | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST) | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set Enabled | |
| Packages | 64-Pin TQFP | |

**TABLE 1-2: DEVICE FEATURES FOR THE PIC18F8XJ93 (80-PIN DEVICES)**

| Features | PIC18F86J93 | PIC18F87J93 |
|---|---|---|
| Operating Frequency | DC – 48 MHz | |
| Program Memory (Bytes) | 64K | 128K |
| Program Memory (Instructions) | 32,768 | 65,536 |
| Data Memory (Bytes) | 3,923 | 3,923 |
| Interrupt Sources | 29 | |
| I/O Ports | Ports A, B, C, D, E, F, G, H, J | |
| LCD Driver (available pixels to drive) | 192 (48 SEGs x 4 COMs) | |
| Timers | 4 | |
| Comparators | 2 | |
| CTMU | Yes | |
| RTCC | Yes | |
| Capture/Compare/PWM Modules | 2 | |
| Serial Communications | MSSP, Addressable USART, Enhanced USART | |
| 12-Bit Analog-to-Digital Module | 12 Input Channels | |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST) | |
| Instruction Set | 75 Instructions, 83 with Extended Instruction Set Enabled | |
| Packages | 80-Pin TQFP | |

 © 2009 Microchip Technology Inc.

**FIGURE 1-2: PIC18F8XJ93 (80-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-3 for I/O port pin descriptions.

**2:** RA6 and RA7 are only available as digital I/Os in select oscillator modes.

**3:** Brown-out Reset and Low-Voltage Detect functions are provided when the on-board voltage regulator is enabled.

 © 2009 Microchip Technology Inc.

**TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0/SEG30 | 48 | | | |
| RB0 | | I/O | TTL | Digital I/O. |
| INT0 | | I | ST | External Interrupt 0. |
| SEG30 | | O | Analog | SEG30 output for LCD. |
| RB1/INT1/SEG8 | 47 | | | |
| RB1 | | I/O | TTL | Digital I/O. |
| INT1 | | I | ST | External Interrupt 1. |
| SEG8 | | O | Analog | SEG8 output for LCD. |
| RB2/INT2/SEG9/CTED1 | 46 | | | |
| RB2 | | I/O | TTL | Digital I/O. |
| INT2 | | I | ST | External Interrupt 2. |
| SEG9 | | O | Analog | SEG9 output for LCD. |
| CTED1 | | I | ST | CTMU Edge 1 input. |
| RB3/INT3/SEG10/CTED2 | 45 | | | |
| RB3 | | I/O | TTL | Digital I/O. |
| INT3 | | I | ST | External Interrupt 3. |
| SEG10 | | O | Analog | SEG10 output for LCD. |
| CTED2 | | I | ST | CTMU Edge 2 input. |
| RB4/KBI0/SEG11 | 44 | | | |
| RB4 | | I/O | TTL | Digital I/O. |
| KBI0 | | I | TTL | Interrupt-on-change pin. |
| SEG11 | | O | Analog | SEG11 output for LCD. |
| RB5/KBI1/SEG29 | 43 | | | |
| RB5 | | I/O | TTL | Digital I/O. |
| KBI1 | | I | TTL | Interrupt-on-change pin. |
| SEG29 | | O | Analog | SEG29 output for LCD. |
| RB6/KBI2/PGC | 42 | | | |
| RB6 | | I/O | TTL | Digital I/O. |
| KBI2 | | I | TTL | Interrupt-on-change pin. |
| PGC | | I/O | ST | In-Circuit Debugger and ICSP™ programming clock pin. |
| RB7/KBI3/PGD | 37 | | | |
| RB7 | | I/O | TTL | Digital I/O. |
| KBI3 | | I | TTL | Interrupt-on-change pin. |
| PGD | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$)

**Note 1:** Default assignment for CCP2 when the CCP2MX Configuration bit is set.

**2:** Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

 © 2009 Microchip Technology Inc.

**TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 30 | | | |
| RC0 | | I/O | ST | Digital I/O. |
| T1OSO | | O | — | Timer1 oscillator output. |
| T13CKI | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/CCP2/SEG32 | 29 | | | |
| RC1 | | I/O | ST | Digital I/O. |
| T1OSI | | I | CMOS | Timer1 oscillator input. |
| CCP2(1) | | I/O | ST | Capture 2 input/Compare 2 output/PWM2 output. |
| SEG32 | | O | Analog | SEG32 output for LCD. |
| RC2/CCP1/SEG13 | 33 | | | |
| RC2 | | I/O | ST | Digital I/O. |
| CCP1 | | I/O | ST | Capture 1 input/Compare 1 output/PWM1 output. |
| SEG13 | | O | Analog | SEG13 output for LCD. |
| RC3/SCK/SCL/SEG17 | 34 | | | |
| RC3 | | I/O | ST | Digital I/O. |
| SCK | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL | | I/O | ST | Synchronous serial clock input/output for $I^2C$™ mode. |
| SEG17 | | O | Analog | SEG17 output for LCD. |
| RC4/SDI/SDA/SEG16 | 35 | | | |
| RC4 | | I/O | ST | Digital I/O. |
| SDI | | I | ST | SPI data in. |
| SDA | | I/O | ST | $I^2C$ data I/O. |
| SEG16 | | O | Analog | SEG16 output for LCD. |
| RC5/SDO/SEG12 | 36 | | | |
| RC5 | | I/O | ST | Digital I/O. |
| SDO | | O | — | SPI data out. |
| SEG12 | | O | Analog | SEG12 output for LCD. |
| RC6/TX1/CK1/SEG27 | 31 | | | |
| RC6 | | I/O | ST | Digital I/O. |
| TX1 | | O | — | EUSART asynchronous transmit. |
| CK1 | | I/O | ST | EUSART synchronous clock (see related RX1/DT1). |
| SEG27 | | O | Analog | SEG27 output for LCD. |
| RC7/RX1/DT1/SEG28 | 32 | | | |
| RC7 | | I/O | ST | Digital I/O. |
| RX1 | | I | ST | EUSART asynchronous receive. |
| DT1 | | I/O | ST | EUSART synchronous data (see related TX1/CK1). |
| SEG28 | | O | Analog | SEG28 output for LCD. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$)

**Note 1:** Default assignment for CCP2 when the CCP2MX Configuration bit is set.

**2:** Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

**TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTG is a bidirectional I/O port. |
| RG0/LCDBIAS0 | 3 | | | |
| RG0 | | I/O | ST | Digital I/O. |
| LCDBIAS0 | | I | Analog | BIAS0 input for LCD. |
| RG1/TX2/CK2 | 4 | | | |
| RG1 | | I/O | ST | Digital I/O. |
| TX2 | | O | — | AUSART asynchronous transmit. |
| CK2 | | I/O | ST | AUSART synchronous clock (see related RX2/DT2). |
| RG2/RX2/DT2/VLCAP1 | 5 | | | |
| RG2 | | I/O | ST | Digital I/O. |
| RX2 | | I | ST | AUSART asynchronous receive. |
| DT2 | | I/O | ST | AUSART synchronous data (see related TX2/CK2). |
| VLCAP1 | | I | Analog | LCD charge pump capacitor input. |
| RG3/VLCAP2 | 6 | | | |
| RG3 | | I/O | ST | Digital I/O. |
| VLCAP2 | | I | Analog | LCD charge pump capacitor input. |
| RG4/SEG26/RTCC | 8 | | | |
| RG4 | | I/O | ST | Digital I/O. |
| SEG26 | | O | Analog | SEG26 output for LCD. |
| RTCC | | O | — | RTCC output |
| VSS | 9, 25, 41, 56 | P | — | Ground reference for logic and I/O pins. |
| VDD | 26, 38, 57 | P | — | Positive supply for logic and I/O pins. |
| AVSS | 20 | P | — | Ground reference for analog modules. |
| AVDD | 19 | P | — | Positive supply for analog modules. |
| ENVREG | 18 | I | ST | Enable for on-chip voltage regulator. |
| VDDCORE/VCAP | 10 | | | Core logic power or external filter capacitor connection. |
| VDDCORE | | P | — | Positive supply for microcontroller core logic (regulator disabled). |
| VCAP | | P | — | External filter capacitor connection (regulator enabled). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

**Note 1:** Default assignment for CCP2 when the CCP2MX Configuration bit is set.

**2:** Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

**TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| $\overline{MCLR}$ | 9 | I | ST | Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device. |
| OSC1/CLKI/RA7 | 49 | | | Oscillator crystal or external clock input. |
| OSC1 | | I | CMOS | Oscillator crystal input. |
| CLKI | | I | CMOS | External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| RA7 | | I/O | TTL | General purpose I/O pin. |
| OSC2/CLKO/RA6 | 50 | | | Oscillator crystal or clock output. |
| OSC2 | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | O | — | In EC modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| RA6 | | I/O | TTL | General purpose I/O pin. |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 30 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| AN0 | | I | Analog | Analog Input 0. |
| RA1/AN1/SEG18 | 29 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| AN1 | | I | Analog | Analog Input 1. |
| SEG18 | | O | Analog | SEG18 output for LCD. |
| RA2/AN2/$V_{REF-}$ | 28 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog Input 2. |
| $V_{REF-}$ | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/$V_{REF+}$ | 27 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog Input 3. |
| $V_{REF+}$ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI/SEG14 | 34 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| SEG14 | | O | Analog | SEG14 output for LCD. |
| RA5/AN4/SEG15 | 33 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog Input 4. |
| SEG15 | | O | Analog | SEG15 output for LCD. |
| RA6 | | | | See the OSC2/CLKO/RA6 pin. |
| RA7 | | | | See the OSC1/CLKI/RA7 pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$)

**Note 1:** Default assignment for CCP2 when the CCP2MX Configuration bit is set.

**2:** Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

 © 2009 Microchip Technology Inc.

**TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTF is a bidirectional I/O port. |
| RF1/AN6/C2OUT/SEG19 | 23 | | | |
| RF1 | | I/O | ST | Digital I/O. |
| AN6 | | I | Analog | Analog Input 6. |
| C2OUT | | O | — | Comparator 2 output. |
| SEG19 | | O | Analog | SEG19 output for LCD. |
| RF2/AN7/C1OUT/SEG20 | 18 | | | |
| RF2 | | I/O | ST | Digital I/O. |
| AN7 | | I | Analog | Analog Input 7. |
| C1OUT | | O | — | Comparator 1 output. |
| SEG20 | | O | Analog | SEG20 output for LCD. |
| RF3/AN8/SEG21/C2INB | 17 | | | |
| RF3 | | I/O | ST | Digital I/O. |
| AN8 | | I | Analog | Analog Input 8. |
| SEG21 | | O | Analog | SEG21 output for LCD. |
| C2INB | | I | Analog | Comparator 2 input B. |
| RF4/AN9/SEG22/C2INA | 16 | | | |
| RF4 | | I/O | ST | Digital I/O. |
| AN9 | | I | Analog | Analog Input 9. |
| SEG22 | | O | Analog | SEG22 output for LCD. |
| C2INA | | I | Analog | Comparator 2 input A. |
| RF5/AN10/CV$_{REF}$/ SEG23/C1INB | 15 | | | |
| RF5 | | I/O | ST | Digital I/O. |
| AN10 | | I | Analog | Analog Input 10. |
| CV$_{REF}$ | | O | Analog | Comparator reference voltage output. |
| SEG23 | | O | Analog | SEG23 output for LCD. |
| C1INB | | I | Analog | Comparator 1 input B. |
| RF6/AN11/SEG24/C1INA | 14 | | | |
| RF6 | | I/O | ST | Digital I/O. |
| AN11 | | I | Analog | Analog Input 11. |
| SEG24 | | O | Analog | SEG24 output for LCD. |
| C1INA | | I | Analog | Comparator 1 input A. |
| RF7/AN5/$\overline{SS}$/SEG25 | 13 | | | |
| RF7 | | I/O | ST | Digital I/O. |
| AN5 | | O | Analog | Analog Input 5. |
| $\overline{SS}$ | | I | TTL | SPI slave select input. |
| SEG25 | | O | Analog | SEG25 output for LCD. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V$_{DD}$)

**Note 1:** Default assignment for CCP2 when the CCP2MX Configuration bit is set.

**2:** Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

**TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTH is a bidirectional I/O port. |
| RH0/SEG47 | 79 | | | |
| RH0 | | I/O | ST | Digital I/O. |
| SEG47 | | O | Analog | SEG47 output for LCD. |
| RH1/SEG46 | 80 | | | |
| RH1 | | I/O | ST | Digital I/O. |
| SEG46 | | O | Analog | SEG46 output for LCD. |
| RH2/SEG45 | 1 | | | |
| RH2 | | I/O | ST | Digital I/O. |
| SEG45 | | O | Analog | SEG45 output for LCD. |
| RH3/SEG44 | 2 | | | |
| RH3 | | I/O | ST | Digital I/O. |
| SEG44 | | O | Analog | SEG44 output for LCD. |
| RH4/SEG40 | 22 | | | |
| RH4 | | I/O | ST | Digital I/O. |
| SEG40 | | O | Analog | SEG40 output for LCD. |
| RH5/SEG41 | 21 | | | |
| RH5 | | I/O | ST | Digital I/O. |
| SEG41 | | O | Analog | SEG41 output for LCD. |
| RH6/SEG42 | 20 | | | |
| RH6 | | I/O | ST | Digital I/O. |
| SEG42 | | O | Analog | SEG42 output for LCD. |
| RH7/SEG43 | 19 | | | |
| RH7 | | I/O | ST | Digital I/O. |
| SEG43 | | O | Analog | SEG43 output for LCD. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$)

**Note 1:** Default assignment for CCP2 when the CCP2MX Configuration bit is set.

**2:** Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

**REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRIGSEL | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **TRIGSEL:** Special Trigger Select bit
1 = Selects the special trigger from the CTMU
0 = Selects the special trigger from the CCP2

bit 6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit ($V_{REF-}$ source)
1 = $V_{REF-}$ (AN2)
0 = $AV_{SS}$

bit 4 **VCFG0:** Voltage Reference Configuration bit ($V_{REF+}$ source)
1 = $V_{REF+}$ (AN3)
0 = $AV_{DD}$

bit 3-0 **PCFG<3:0>:** A/D Port Configuration Control bits:

| PCFG<3:0> | AN11 | AN10 | AN9 | AN8 | AN7 | AN6 | AN5 | AN4 | AN3 | AN2 | AN1 | AN0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000 | A | A | A | A | A | A | A | A | A | A | A | A |
| 0001 | A | A | A | A | A | A | A | A | A | A | A | A |
| 0010 | A | A | A | A | A | A | A | A | A | A | A | A |
| 0011 | A | A | A | A | A | A | A | A | A | A | A | A |
| 0100 | D | A | A | A | A | A | A | A | A | A | A | A |
| 0101 | D | D | A | A | A | A | A | A | A | A | A | A |
| 0110 | D | D | D | A | A | A | A | A | A | A | A | A |
| 0111 | D | D | D | D | A | A | A | A | A | A | A | A |
| 1000 | D | D | D | D | D | A | A | A | A | A | A | A |
| 1001 | D | D | D | D | D | D | A | A | A | A | A | A |
| 1010 | D | D | D | D | D | D | D | A | A | A | A | A |
| 1011 | D | D | D | D | D | D | D | D | A | A | A | A |
| 1100 | D | D | D | D | D | D | D | D | D | A | A | A |
| 1101 | D | D | D | D | D | D | D | D | D | D | A | A |
| 1110 | D | D | D | D | D | D | D | D | D | D | D | A |
| 1111 | D | D | D | D | D | D | D | D | D | D | D | D |

A = Analog input D = Digital I/O

 © 2009 Microchip Technology Inc.

**REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADFM | — | ACQT2 | ACQT1 | ACQT0 | ADCS2 | ADCS1 | ADCS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

## 2.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-2. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ**. After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

| **Note:** | When the conversion is started, the holding capacitor is disconnected from the input pin. |
|---|---|

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (1,024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Equation 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

| | | |
|---|---|---|
| CHOLD | = | 25 pF |
| Rs | = | 2.5 kΩ |
| Conversion Error | ≤ | 1/2 LSb |
| VDD | = | 3V → Rss = 2 kΩ |
| Temperature | = | 85°C (system max.) |

**EQUATION 2-1: ACQUISITION TIME**

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$

**EQUATION 2-2: A/D MINIMUM CHARGING TIME**

$$V_{HOLD} = (V_{REF} - (V_{REF}/2048)) \cdot (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$

or

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/2048)$$

**EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME**

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$

$$T_{AMP} = 0.2\ \mu s$$

$$T_{COFF} = (Temp - 25°C)(0.02\ \mu s/°C)$$
$$(85°C - 25°C)(0.02\ \mu s/°C)$$
$$1.2\ \mu s$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, $T_{COFF}$ = 0 ms.

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/2048)\ \mu s$$
$$-(25\ pF)\ (1\ k\Omega + 2\ k\Omega + 2.5\ k\Omega) \ln(0.0004883)\ \mu s$$
$$1.05\ \mu s$$

$$T_{ACQ} = 0.2\ \mu s + 1\ \mu s + 1.2\ \mu s$$
$$2.4\ \mu s$$

 © 2009 Microchip Technology Inc.

## 2.2 Selecting and Configuring Automatic Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set.

When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This occurs when the ACQT<2:0> bits (ADCON2<5:3>) remain in their Reset state ('000') and is compatible with devices that do not offer programmable acquisition times.

If desired, the ACQT bits can be set to select a programmable acquisition time for the A/D module. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 11 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible but greater than the minimum TAD.

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-1: TAD VS. DEVICE OPERATING FREQUENCIES**

| AD Clock Source (TAD) | | Maximum Device Frequency |
|---|---|---|
| Operation | ADCS<2:0> | |
| 2 TOSC | 000 | 2.86 MHz |
| 4 TOSC | 100 | 5.71 MHz |
| 8 TOSC | 001 | 11.43 MHz |
| 16 TOSC | 101 | 22.86 MHz |
| 32 TOSC | 010 | 40.0 MHz |
| 64 TOSC | 110 | 40.0 MHz |
| RC(2) | x11 | 1.00 MHz(1) |

**Note 1:** The RC source has a typical TAD time of 4 μs.

**2:** For device frequencies above 1 MHz, the device must be in Sleep mode for the entire conversion or the A/D accuracy may be out of specification.

## 2.4 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

**Note 1:** When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will be accurately converted.

**2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

## 3.0 SPECIAL FEATURES OF THE CPU

**Note 1:** This section documents only the CPU features that are different from, or in addition to, the features of the PIC18F87J90 family devices.

**2:** For additional details on the Configuration bits, refer to **Section 24.1 "Configuration Bits"** in the *"PIC18F87J90 Family Data Sheet"* (DS39933).

### 3.1 Device ID Registers

The Device ID registers are "read-only" registers. They identify the device type and revision for device programmers and can be read by firmware using table reads.

**TABLE 3-1: DEVICE ID REGISTERS**

| File Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default/ Unprogrammed Value(1) |
|---|---|---|---|---|---|---|---|---|---|---|
| 3FFFFEh | DEVID1 | DEV2 | DEV1 | DEV0 | REV4 | REV3 | REV2 | REV1 | REV0 | xxxx xxxx(2) |
| 3FFFFFh | DEVID2 | DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | DEV3 | 0000 10x1(2) |

**Legend:** x = unknown, – = unimplemented. Shaded cells are unimplemented, read as '0'.

**Note 1:** Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.

**2:** See Register 3-1 and Register 3-2 for DEVID values. These registers are read-only and cannot be programmed by the user.

## 5.0 PACKAGING INFORMATION

For packaging information, see the *"PIC18F87J93 Family Data Sheet"* (DS39933).

 © 2009 Microchip Technology Inc.

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain purchasing information such as pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Pattern |

| | |
|---|---|
| Device[1,2] | PIC18F66J93, PIC18F66J93T<br>PIC18F67J93, PIC18F67J93T<br>PIC18F86J93, PIC18F86J93T<br>PIC18F87J93, PIC18F87J93T |
| Temperature Range | I = -40°C to +85°C (Industrial) |
| Package | PT = TQFP (Thin Quad Flatpack) |
| Pattern | QTP, SQTP, Code or Special Requirements (blank otherwise) |

**Examples:**

a) PIC18F87J93-I/PT 301 = Industrial temperature, TQFP package, QTP pattern #301.

b) PIC18F87J93T-I/PT = Tape and reel, Industrial temperature, TQFP package.

**Note 1:** F = Standard Voltage Range
**2:** T = In Tape and Reel

# WORLDWIDE SALES AND SERVICE

## AMERICAS

**Corporate Office**
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

**Atlanta**
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

**Boston**
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

**Chicago**
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

**Cleveland**
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

**Dallas**
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

**Detroit**
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

**Kokomo**
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

**Los Angeles**
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

**Santa Clara**
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

**Toronto**
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

## ASIA/PACIFIC

**Asia Pacific Office**
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

**Australia - Sydney**
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

**China - Beijing**
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

**China - Chengdu**
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

**China - Hong Kong SAR**
Tel: 852-2401-1200
Fax: 852-2401-3431

**China - Nanjing**
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

**China - Qingdao**
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

**China - Shanghai**
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

**China - Shenyang**
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

**China - Shenzhen**
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

**China - Wuhan**
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

**China - Xiamen**
Tel: 86-592-2388138
Fax: 86-592-2388130

**China - Xian**
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

**China - Zhuhai**
Tel: 86-756-3210040
Fax: 86-756-3210049

## ASIA/PACIFIC

**India - Bangalore**
Tel: 91-80-3090-4444
Fax: 91-80-3090-4080

**India - New Delhi**
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

**India - Pune**
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

**Japan - Yokohama**
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

**Korea - Daegu**
Tel: 82-53-744-4301
Fax: 82-53-744-4302

**Korea - Seoul**
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

**Malaysia - Kuala Lumpur**
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

**Malaysia - Penang**
Tel: 60-4-227-8870
Fax: 60-4-227-4068

**Philippines - Manila**
Tel: 63-2-634-9065
Fax: 63-2-634-9069

**Singapore**
Tel: 65-6334-8870
Fax: 65-6334-8850

**Taiwan - Hsin Chu**
Tel: 886-3-6578-300
Fax: 886-3-6578-370

**Taiwan - Kaohsiung**
Tel: 886-7-536-4818
Fax: 886-7-536-4803

**Taiwan - Taipei**
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

**Thailand - Bangkok**
Tel: 66-2-694-1351
Fax: 66-2-694-1350

## EUROPE

**Austria - Wels**
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

**Denmark - Copenhagen**
Tel: 45-4450-2828
Fax: 45-4485-2829

**France - Paris**
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

**Germany - Munich**
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

**Italy - Milan**
Tel: 39-0331-742611
Fax: 39-0331-466781

**Netherlands - Drunen**
Tel: 31-416-690399
Fax: 31-416-690340

**Spain - Madrid**
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

**UK - Wokingham**
Tel: 44-118-921-5869
Fax: 44-118-921-5820

03/26/09


© 2009 Microchip Technology Inc.