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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3923 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f86j93-i-pt

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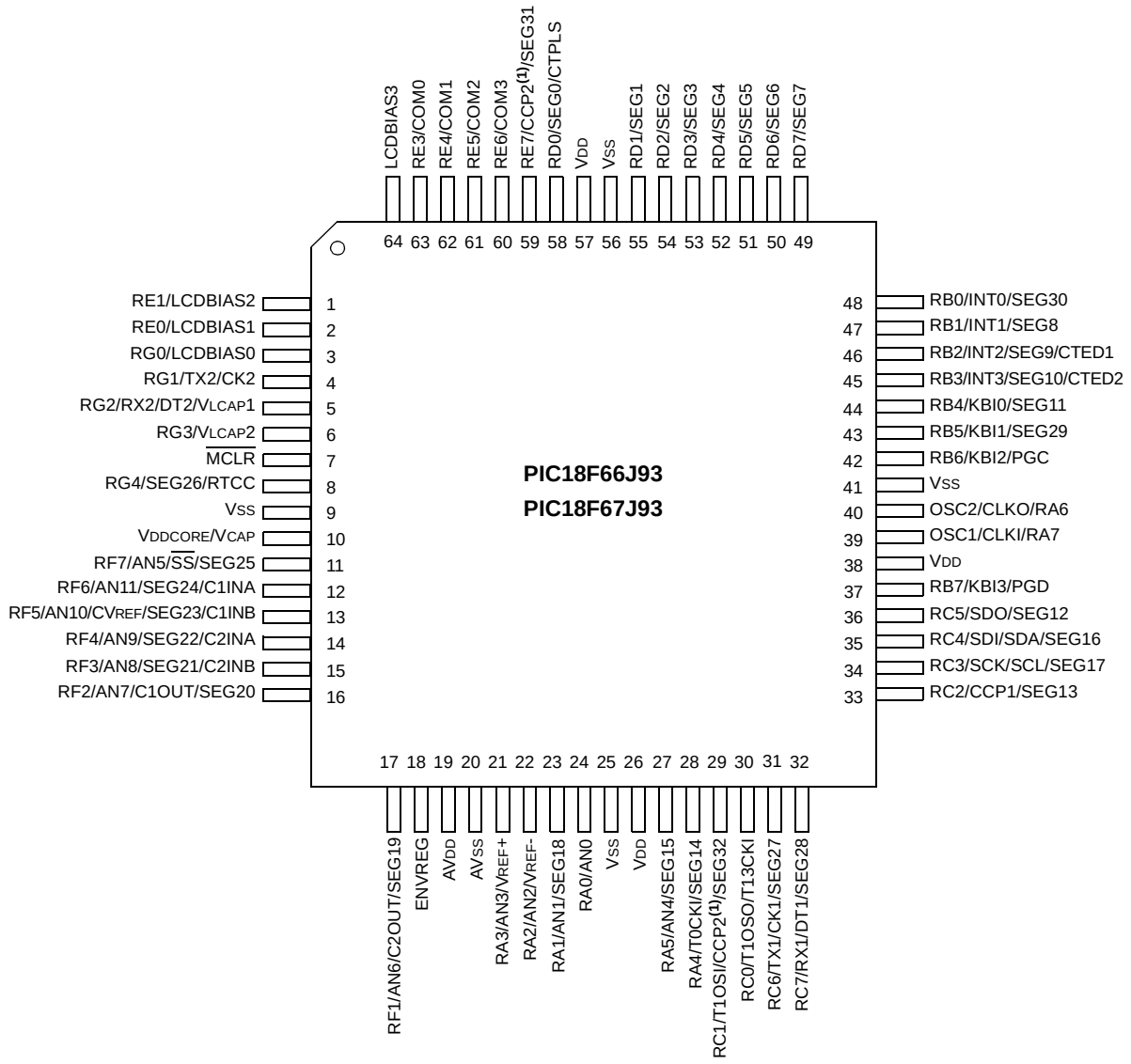
Special Microcontroller Features:

- 10,000 Erase/Write Cycle Flash Program Memory, Typical
- Flash Retention 20 Years, Minimum
- Self-Programmable under Software Control
- Flash Program Memory has Word Write Capability for Data EEPROM Emulators
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug via Two Pins
- Operating Voltage Range: 2.0V to 3.6V
- 5.5V Tolerant Input (digital pins only)
- Selectable Open-Drain Configuration for Serial Communication and CCP Pins for Driving Outputs up to 5V
- On-Chip 2.5V Regulator

Pin Diagrams – PIC18F6XJ93

64-Pin TQFP



Note 1: The CCP2 pin placement depends on the CCP2MX Configuration bit setting.

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F66J93
- PIC18F67J93
- PIC18F86J93
- PIC18F87J93

Note: This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F87J90 family devices. For information on the features and specifications shared by the PIC18F87J93 family and PIC18F87J90 family devices, see the *"PIC18F87J90 Family Data Sheet"* (DS39933).

The PIC18F87J93 family of devices offers the advantages of all PIC18 microcontrollers – high computational performance, a rich feature set and economical price – with the addition of a versatile, on-chip LCD driver. These features make the PIC18F87J93 family a logical choice for many high-performance applications where price is a primary consideration.

1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F87J93 family implements a 12-bit A/D converter. A/D converters in both families incorporate programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.
- **Data RAM:** The PIC18F87J93 family devices have 3,923 bytes of RAM.

1.2 Details on Individual Family Members

Devices in the PIC18F87J93 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

- Flash Program Memory (64 Kbytes for PIC18FX6J93 devices and 128 Kbytes for PIC18FX7J93).
- LCD Pixels:
  - 64-pin devices – 132 pixels (33 SEGs x 4 COMs)
  - 80-pin devices – 192 pixels (48 SEGs x 4 COMs)
- I/O Ports (seven bidirectional ports on PIC18F6XJ93 devices and nine bidirectional ports on PIC18F8XJ93 devices).

All other features for devices in this family are identical and are summarized in Table 1-1 and Table 1-2.

The devices' block diagrams are given in Figure 1-1 and Figure 1-2.

The pinouts for all devices are listed in Table 1-3 and Table 1-4.

TABLE 1-1: DEVICE FEATURES FOR THE PIC18F6XJ93 (64-PIN DEVICES)

Features	PIC18F66J93	PIC18F67J93
Operating Frequency	DC – 48 MHz	
Program Memory (Bytes)	64K	128K
Program Memory (Instructions)	32,768	65,536
Data Memory (Bytes)	3,923	3,923
Interrupt Sources	29	
I/O Ports	Ports A, B, C, D, E, F, G	
LCD Driver (available pixels to drive)	132 (33 SEGs x 4 COMs)	
Timers	4	
Comparators	2	
CTMU	Yes	
RTCC	Yes	
Capture/Compare/PWM Modules	2	
Serial Communications	MSSP, Addressable USART, Enhanced USART	
12-Bit Analog-to-Digital Module	12 Input Channels	
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)	
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled	
Packages	64-Pin TQFP	

TABLE 1-2: DEVICE FEATURES FOR THE PIC18F8XJ93 (80-PIN DEVICES)

Features	PIC18F86J93	PIC18F87J93
Operating Frequency	DC – 48 MHz	
Program Memory (Bytes)	64K	128K
Program Memory (Instructions)	32,768	65,536
Data Memory (Bytes)	3,923	3,923
Interrupt Sources	29	
I/O Ports	Ports A, B, C, D, E, F, G, H, J	
LCD Driver (available pixels to drive)	192 (48 SEGs x 4 COMs)	
Timers	4	
Comparators	2	
CTMU	Yes	
RTCC	Yes	
Capture/Compare/PWM Modules	2	
Serial Communications	MSSP, Addressable USART, Enhanced USART	
12-Bit Analog-to-Digital Module	12 Input Channels	
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)	
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled	
Packages	80-Pin TQFP	

TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTG is a bidirectional I/O port.
RG0/LCDBIAS0	5			
RG0		I/O	ST	Digital I/O.
LCDBIAS0		I	Analog	BIAS0 input for LCD.
RG1/TX2/CK2	6			
RG1		I/O	ST	Digital I/O.
TX2		O	—	AUSART asynchronous transmit.
CK2		I/O	ST	AUSART synchronous clock (see related RX2/DT2).
RG2/RX2/DT2/VLCAP1	7			
RG2		I/O	ST	Digital I/O.
RX2		I	ST	AUSART asynchronous receive.
DT2		I/O	ST	AUSART synchronous data (see related TX2/CK2).
VLCAP1		I	Analog	LCD charge pump capacitor input.
RG3/VLCAP2	8			
RG3		I/O	ST	Digital I/O.
VLCAP2		I	Analog	LCD charge pump capacitor input.
RG4/SEG26/RTCC	10			
RG4		I/O	ST	Digital I/O.
SEG26		O	Analog	SEG26 output for LCD.
RTCC		O	—	RTCC output.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTH is a bidirectional I/O port.
RH0/SEG47	79			
RH0		I/O	ST	Digital I/O.
SEG47		O	Analog	SEG47 output for LCD.
RH1/SEG46	80			
RH1		I/O	ST	Digital I/O.
SEG46		O	Analog	SEG46 output for LCD.
RH2/SEG45	1			
RH2		I/O	ST	Digital I/O.
SEG45		O	Analog	SEG45 output for LCD.
RH3/SEG44	2			
RH3		I/O	ST	Digital I/O.
SEG44		O	Analog	SEG44 output for LCD.
RH4/SEG40	22			
RH4		I/O	ST	Digital I/O.
SEG40		O	Analog	SEG40 output for LCD.
RH5/SEG41	21			
RH5		I/O	ST	Digital I/O.
SEG41		O	Analog	SEG41 output for LCD.
RH6/SEG42	20			
RH6		I/O	ST	Digital I/O.
SEG42		O	Analog	SEG42 output for LCD.
RH7/SEG43	19			
RH7		I/O	ST	Digital I/O.
SEG43		O	Analog	SEG43 output for LCD.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) converter module has 12 inputs for all PIC18F87J93 family devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has these registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCAL	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ADCAL:** A/D Calibration bit
1 = Calibration is performed on next A/D conversion
0 = Normal A/D converter operation (no calibration is performed)

bit 6 **Unimplemented:** Read as ‘0’

bit 5-2 **CHS<3:0>:** Analog Channel Select bits
0000 = Channel 00 (AN0)
0001 = Channel 01 (AN1)
0010 = Channel 02 (AN2)
0011 = Channel 03 (AN3)
0100 = Channel 04 (AN4)
0101 = Channel 05 (AN5)
0110 = Channel 06 (AN6)
0111 = Channel 07 (AN7)
1000 = Channel 08 (AN8)
1001 = Channel 09 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
11xx = Unused

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit
1 = A/D converter module is enabled
0 = A/D converter module is disabled

REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIGSEL	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TRIGSEL:** Special Trigger Select bit
1 = Selects the special trigger from the CTMU
0 = Selects the special trigger from the CCP2

bit 6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = AV_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = AV_{DD}

bit 3-0 **PCFG<3:0>:** A/D Port Configuration Control bits:

PCFG<3:0>	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A
0011	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (AV_{DD} and AV_{SS}) or the voltage level on the RA3/AN3/V_{REF+} and RA2/AN2/V_{REF-} pins.

The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

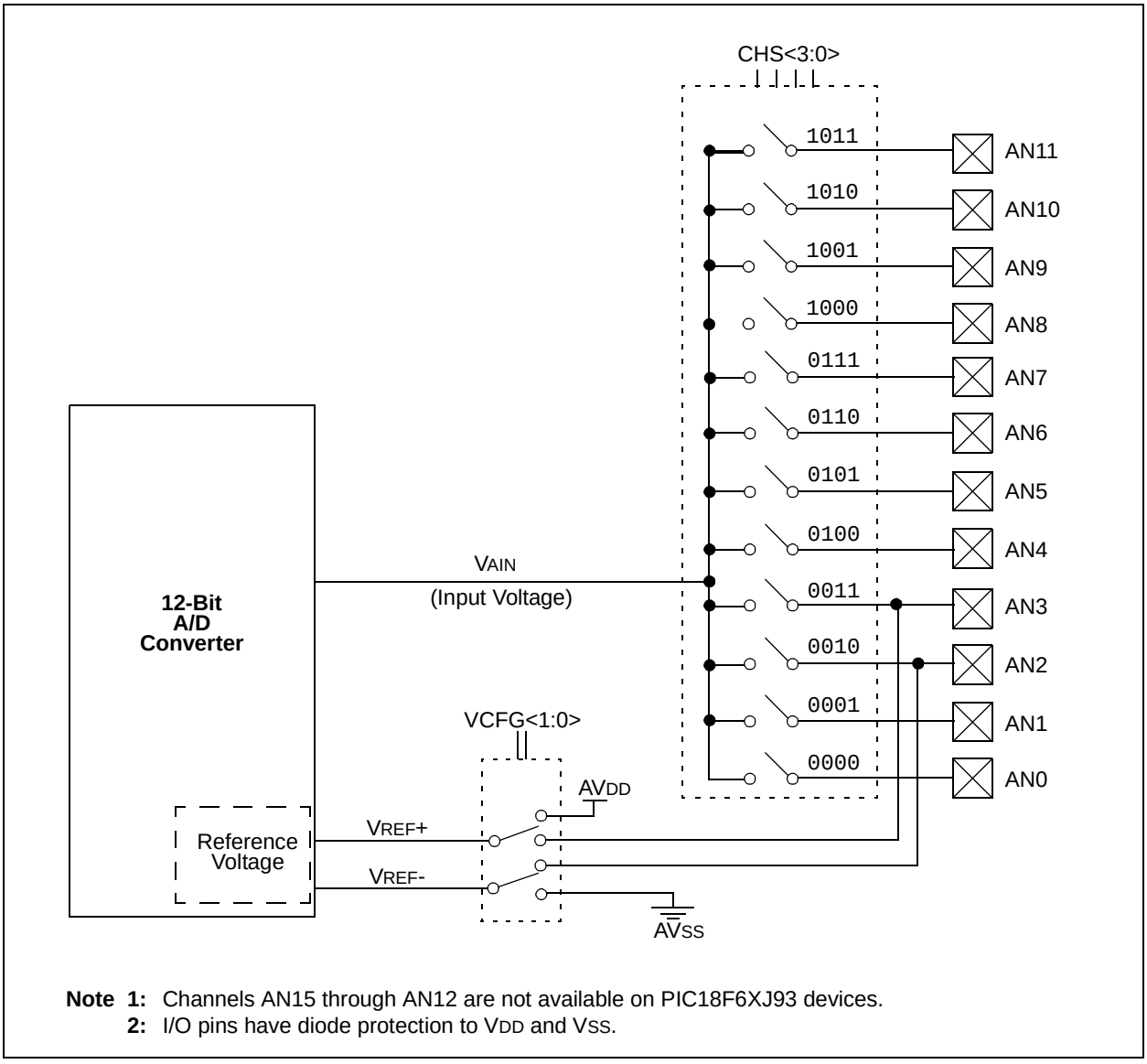
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

Each port pin associated with the A/D converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted. The value in the ADRESH:ADRESL register pair is not modified for a Power-on Reset. These registers will contain unknown data after a Power-on Reset.

The block diagram of the A/D module is shown in Figure 2-1.

FIGURE 2-1: A/D BLOCK DIAGRAM(1,2)



Note 1: Channels AN15 through AN12 are not available on PIC18F6XJ93 devices.
2: I/O pins have diode protection to V_{DD} and V_{SS}.

2.2 Selecting and Configuring Automatic Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set.

When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This occurs when the ACQT<2:0> bits (ADCON2<5:3>) remain in their Reset state ('000') and is compatible with devices that do not offer programmable acquisition times.

If desired, the ACQT bits can be set to select a programmable acquisition time for the A/D module. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 11 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible but greater than the minimum TAD.

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-1: TAD VS. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Maximum Device Frequency
Operation	ADCS<2:0>	
2 TOSC	000	2.86 MHz
4 TOSC	100	5.71 MHz
8 TOSC	001	11.43 MHz
16 TOSC	101	22.86 MHz
32 TOSC	010	40.0 MHz
64 TOSC	110	40.0 MHz
RC(2)	x11	1.00 MHz(1)

Note 1: The RC source has a typical TAD time of 4 μs.

2: For device frequencies above 1 MHz, the device must be in Sleep mode for the entire conversion or the A/D accuracy may be out of specification.

2.4 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

Note 1: When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will be accurately converted.

2: Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

2.5 A/D Conversions

Figure 2-3 shows the operation of the A/D converter after the GO/$\overline{\text{DONE}}$ bit has been set and the ACQT<2:0> bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-4 shows the operation of the A/D converter after the GO/$\overline{\text{DONE}}$ bit has been set; the ACQT<2:0> bits are set to '010' and a 4 TAD acquisition time is selected before the conversion starts.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D.

2.6 Use of the CCP2 Trigger

An A/D conversion can be started by the "Special Event Trigger" of the CCP2 module. This requires that the CCP2M<3:0> bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time is selected before the Special Event Trigger sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module but will still reset the Timer1 (or Timer3) counter.

FIGURE 2-3: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)

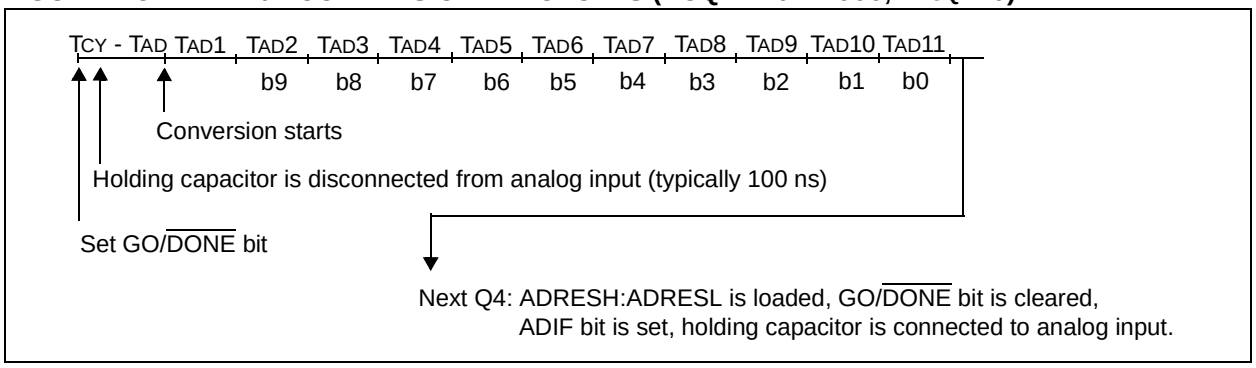
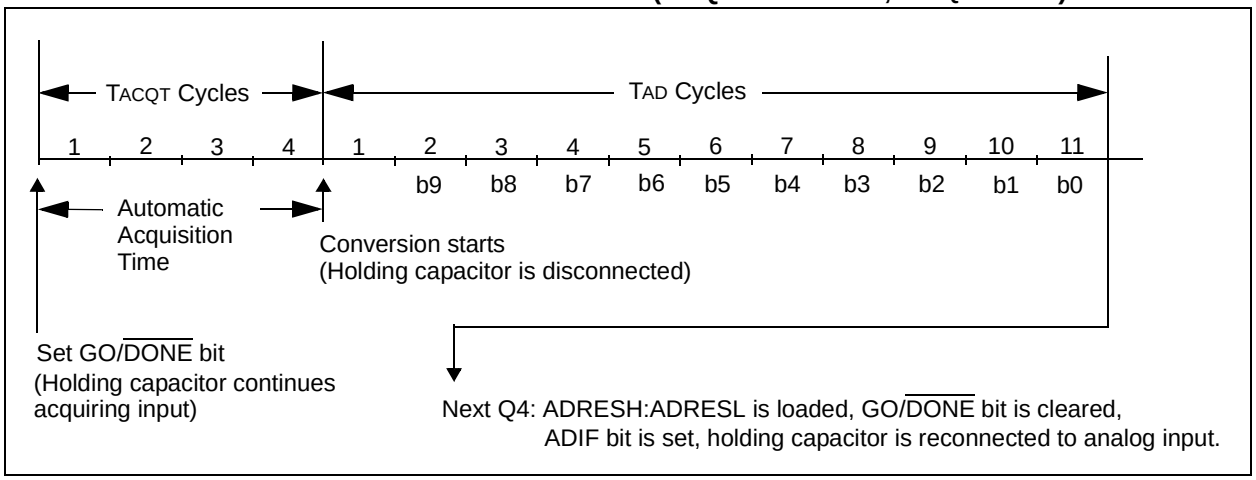


FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



3.0 SPECIAL FEATURES OF THE CPU

Note 1: This section documents only the CPU features that are different from, or in addition to, the features of the PIC18F87J90 family devices.

2: For additional details on the Configuration bits, refer to **Section 24.1 "Configuration Bits"** in the *"PIC18F87J90 Family Data Sheet"* (DS39933).

3.1 Device ID Registers

The Device ID registers are "read-only" registers. They identify the device type and revision for device programmers and can be read by firmware using table reads.

TABLE 3-1: DEVICE ID REGISTERS

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value(1)
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx(2)
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0000 10x1(2)

Legend: x = unknown, – = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.

2: See Register 3-1 and Register 3-2 for DEVID values. These registers are read-only and cannot be programmed by the user.

REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F87J93 FAMILY DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:
R = Read-only bit

bit 7-5 **DEV<2:0>:** Device ID bits

111 = PIC18F87J93
110 = PIC18F86J93
011 = PIC18F67J93
010 = PIC18F66J93

bit 4-0 **REV<4:0>:** Revision ID bits

These bits are used to indicate the device revision.

REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F87J93 FAMILY DEVICES

R	R	R	R	R	R	R	R
DEV10(1)	DEV9(1)	DEV8(1)	DEV7(1)	DEV6(1)	DEV5(1)	DEV4(1)	DEV3(1)
bit 7							bit 0

Legend:
R = Read-only bit

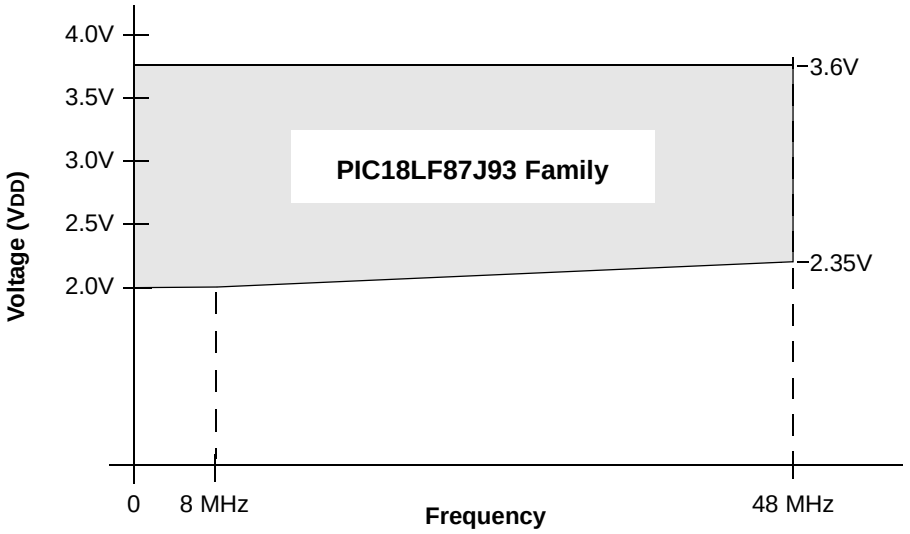
bit 7-0 **DEV<10:3>:** Device ID bits(1)

These bits are used with the DEV<2:0> bits in the Device ID Register 1 to identify the part number.

0101 0000 = PIC18F87J93 family devices

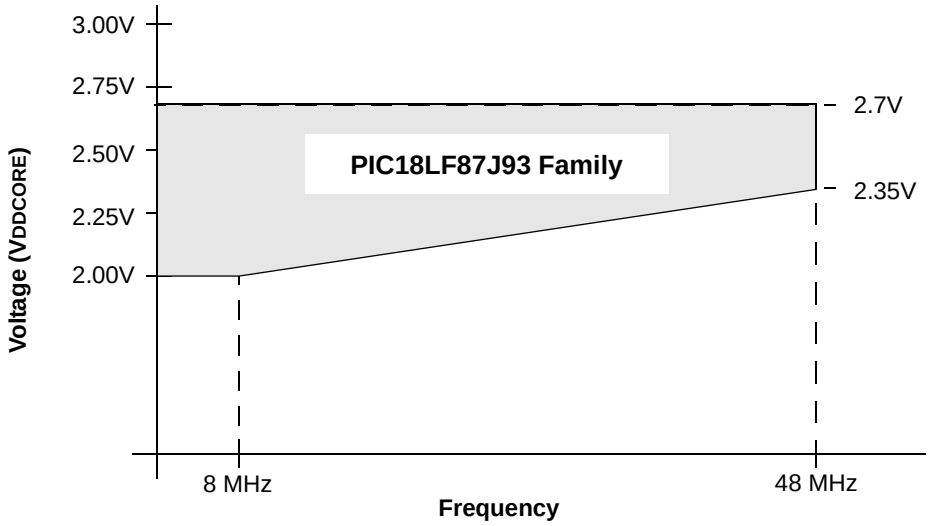
Note 1: The values for DEV<10:3> may be shared with other device families. The specific device is always identified by using the entire DEV<10:0> bit sequence.

FIGURE 4-1: VOLTAGE-FREQUENCY GRAPH, REGULATOR ENABLED (INDUSTRIAL)(1)



Note 1: When the on-chip regulator is enabled, its BOR circuit will automatically trigger a device Reset before VDD reaches a level at which full-speed operation is not possible.

FIGURE 4-2: VOLTAGE-FREQUENCY GRAPH, REGULATOR DISABLED (INDUSTRIAL)(1)



Note 1: When the on-chip voltage regulator is disabled, VDD and VDDCORE must be maintained so that VDDCORE ≤ VDD ≤ 3.6V.

TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F87J93 FAMILY (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
A01	NR	Resolution	—	—	12	bit	ΔVREF ≥ 3.0V
A03	EIL	Integral Linearity Error	—	<±1	±2.0	LSB	ΔVREF ≥ 3.0V
A04	EDL	Differential Linearity Error	—	<±1	±1.5	LSB	ΔVREF ≥ 3.0V
A06	EOFF	Offset Error	—	<±1	±5	LSB	ΔVREF ≥ 3.0V
A07	EGN	Gain Error	—	<±1	±3	LSB	ΔVREF ≥ 3.0V
A10	—	Monotonicity	Guaranteed(1)			—	VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	VDD – VSS	V	For 12-bit resolution
A21	VREFH	Reference Voltage High	VSS + 3.0V	—	VDD + 0.3V	V	For 12-bit resolution
A22	VREFL	Reference Voltage Low	VSS – 0.3V	—	VDD – 3.0V	V	For 12-bit resolution
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V	**Note 2**
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ	
A50	IREF	VREF Input Current(2)	— —	— —	5 150	μA μA	During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

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