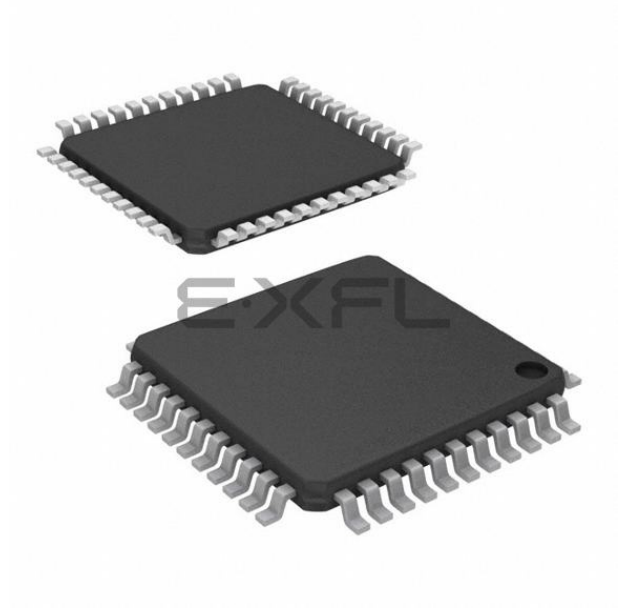


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08ac128cfge

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Table of Contents

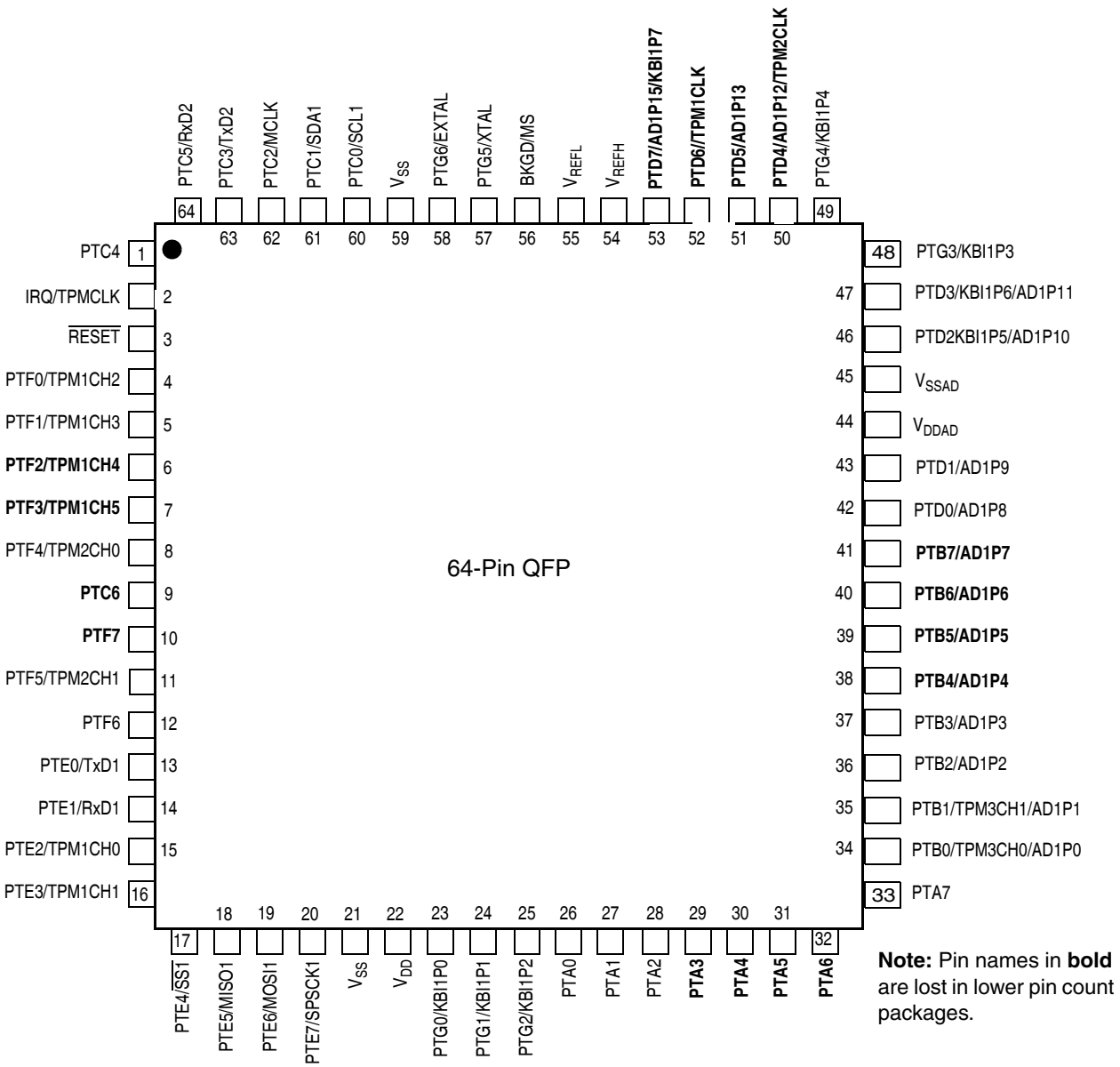
Chapter 1
Device Overview 3
1.1 MCU Block Diagram 3
Chapter 2
Pins and Connections 5
2.1 Device Pin Assignment 5
Chapter 3
Electrical Characteristics and Timing Specifications 11
3.1 Introduction 11
3.2 Parameter Classification 11
3.3 Absolute Maximum Ratings 11
3.4 Thermal Characteristics 13
3.5 ESD Protection and Latch-Up Immunity 14
3.6 DC Characteristics 14
3.7 Supply Current Characteristics 18
3.8 ADC Characteristics 21
3.9 Internal Clock Generation Module Characteristics . . . 24
3.9.1 ICG Frequency Specifications 25
3.10 AC Characteristics 27
3.10.1 Control Timing 27
3.10.2 Timer/PWM (TPM) Module Timing 28
3.11 SPI Characteristics 30
3.12 FLASH Specifications 33
3.13 EMC Performance 34
3.13.1 Radiated Emissions 34
Chapter 4
Ordering Information and Mechanical Drawings 35
4.1 Ordering Information 35
4.2 Orderable Part Numbering System 35
4.3 Mechanical Drawings 35
Chapter 5
Revision History 37

Related Documentation

MC9S08AC128 Series Reference Manual (MC9S08AC128RM)
contains extensive product information including modes of operartion, memory, resets and interrupts, register definitions, port pins, CPU, and all peripheral module information.

For the latest version of the documentation, check our website at:
http://www.freescale.com

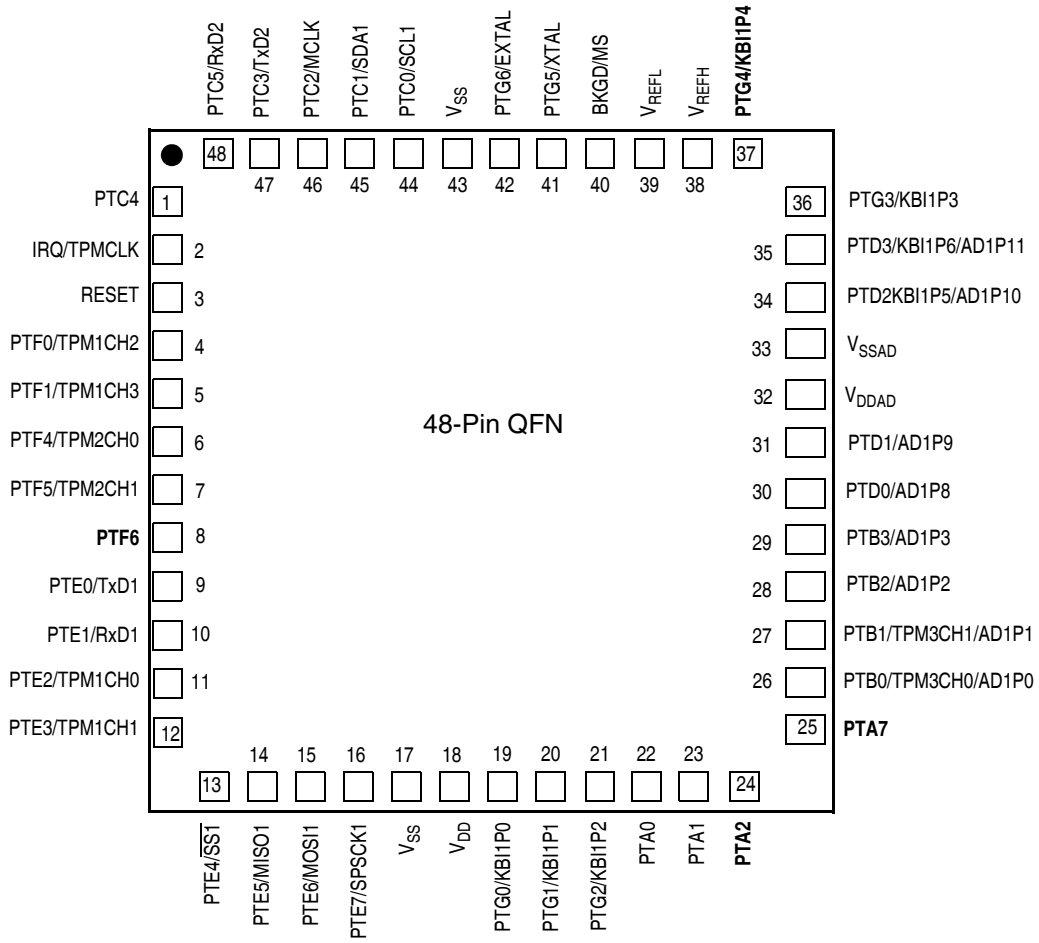
Figure 2-2 shows the 64-pin package assignments for the MC9S08AC128 Series devices.



Note: Pin names in **bold** are lost in lower pin count packages.

Figure 2-2. MC9S08AC128 Series in 64-Pin QFP Package

Figure 2-1 shows the 48-pin package assignments for the MC9S08AC128 Series devices.



Note: Pin names in **bold** are lost in lower pin count packages.

Figure 2-1. MC9S08AC128 Series in 48-Pin QFN Package

Figure 2-3 shows the 44-pin LQFP pin assignments for the MC9S08AC128 Series device.

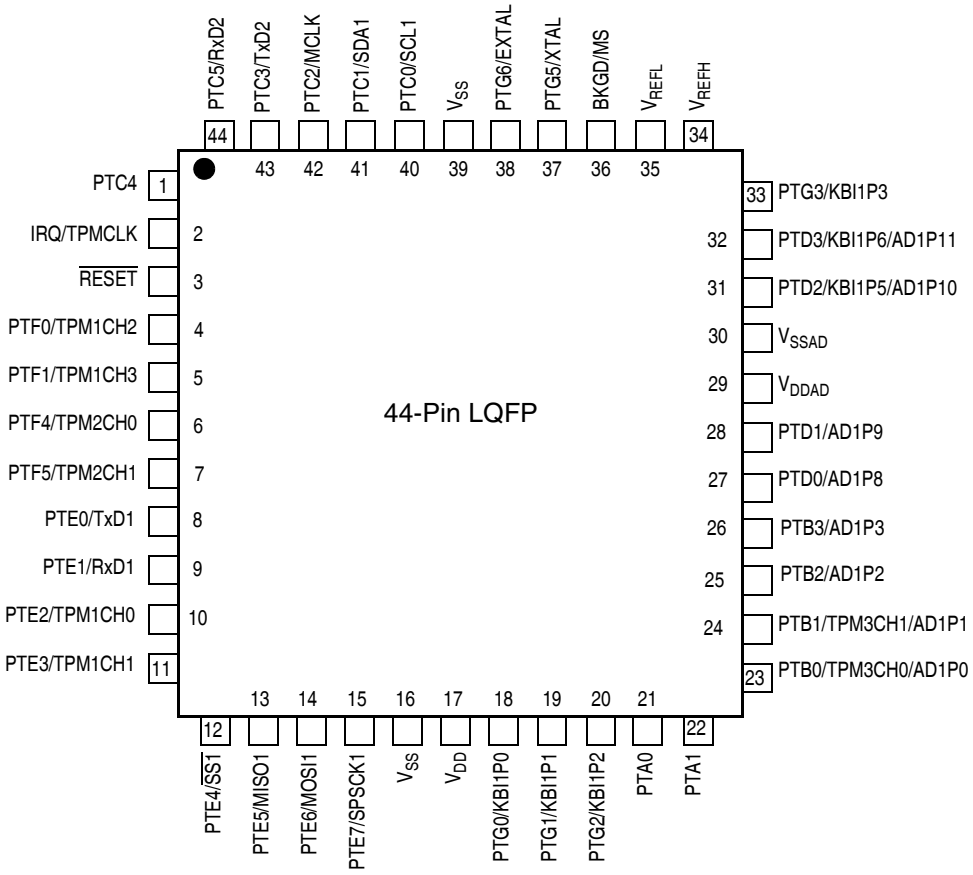


Figure 2-3. MC9S08AC128 Series in 44-Pin LQFP Package

Table 2-4. Pin Availability by Package Pin-Count

Pin Number				Lowest <-- Priority --> Highest		
80	64	48	44	Port Pin	Alt 1	Alt 2
1	1	1	1	PTC4		
2	2	2	2	IRQ	TPMCLK[1]	
3	3	3	3	$\overline{\text{RESET}}$		
4	4	4	4	PTF0	TPM1CH2	
5	5	5	5	PTF1	TPM1CH3	
6	6	—	—	PTF2	TPM1CH4	
7	7	—	—	PTF3	TPM1CH5	
8	8	6	6	PTF4	TPM2CH0	
9	9	—	—	PTC6		
10	10	—	—	PTF7		
11	11	7	7	PTF5	TPM2CH1	
12	12	8	—	PTF6		

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <-- Priority --> Highest		
80	**64**	**48**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
54	42	30	27	PTD0	AD1P8	
55	43	31	28	PTD1	AD1P9	
56	44	32	29	V_{DDAD}		
57	45	33	30	V_{SSAD}		
58	46	34	31	PTD2	KBI1P5	AD1P10
59	47	35	32	PTD3	KBI1P6	AD1P11
60	48	36	33	PTG3	KBI1P3	
61	49	37	—	PTG4	KBI1P4	
62	50	—	—	PTD4	TPM2CLK	AD1P12
63	51	—	—	PTD5	AD1P13	
64	52	—	—	PTD6	TPM1CLK	AD1P14
65	53	—	—	PTD7	KBI1P7	AD1P15
66	54	38	34	V_{REFH}		
67	55	39	35	V_{REFL}		
68	56	40	36	BKGD	MS	
69	57	41	37	PTG5	XTAL	
70	58	42	38	PTG6	EXTAL	
71	59	43	39	V_{SS}		
72	—	—	—	V_{DD}(NC)		
73	60	44	40	PTC0	SCL1	
74	61	45	41	PTC1	SDA1	
75	—	—	—	PTH4	SPSCK2	
76	—	—	—	PTH5	MOSI2	
77	—	—	—	PTH6	MISO2	
78	62	46	42	PTC2	MCLK	
79	63	47	43	PTC3	TxD2	
80	64	48	44	PTC5	RxD2	

[1] TPMCLK, TPM1CLK, and TPM2CLK options are configured via software; out of reset, TPM1CLK, TPM2CLK, and TPMCLK are available to TPM1, TPM2, and TPM3 respectively.

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3-3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits and JEDEC Standard for Non-Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3-4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		– 2.5	V
	Maximum input voltage limit		7.5	V

Table 3-5. ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	± 2000	–	V
2	C	Machine Model (MM)	V_{MM}	± 200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	± 500	–	V
4	C	Latch-up Current at T_A = 125°C	I_{LAT}	± 100	–	mA

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

3.8 ADC Characteristics

Table 3-8. 5 Volt 10-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V
	Delta to V_{DD} (V_{DD}–V_{DDAD})[2]	ΔV_{DDAD}	–100	0	+100	mV
Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSAD})[2]	ΔV_{SSAD}	–100	0	+100	mV
Ref voltage high		V_{REFH}	2.7	V_{DDAD}	V_{DDAD}	V
Ref voltage low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V
Supply current	Stop, reset, module off	I_{DDAD}	—	0.011	1	μA
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input capacitance		C_{ADIN}	—	4.5	5.5	pF
Input resistance		R_{ADIN}	—	3	5	kΩ
Analog source resistance External to MCU	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ
	8-bit mode (all valid f_{ADCK})		—	—	10	
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz
	Low power (ADLPC = 1)		0.4	—	4.0	
Temp Sensor Slope	–40°C to 25°C	m	—	3.266	—	mV/°C
	25°C to 125°C			3.638	—	
Temp Sensor Voltage	25°C	V_{TEMP25}	—	1.396	—	V

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 dc potential difference.

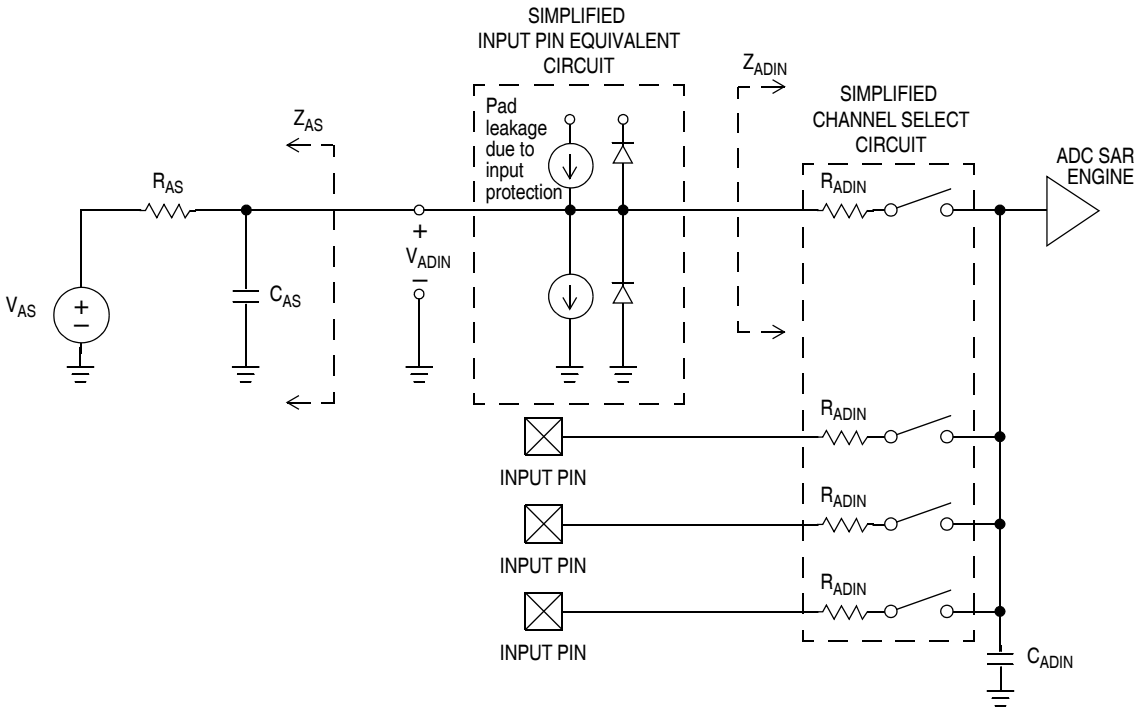


Figure 3-8. ADC Input Impedance Equivalency Diagram

Table 3-9. 5 Volt 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDAD}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDAD}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	—	μA
	$V_{DDAD} \leq 5.5$ V	P		—	—	1	mA
ADC asynchronous clock source $t_{ADACK} = 1/f_{ADACK}$	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (Including sample time)	Short sample (ADLSMP = 0)	P	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	P	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted error Includes quantization	10-bit mode	P	E_{TUE}	—	±1	±2.5	LSB[2]
	8-bit mode			—	±0.5	±1.0	
Differential non-linearity	10-bit mode	P	DNL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
	Monotonicity and no-missing-codes guaranteed						
Integral non-linearity	10-bit mode	C	INL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
Zero-scale error $V_{ADIN} = V_{SSA}$	10-bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Full-scale error $V_{ADIN} = V_{DDA}$	10-bit mode	P	E_{FS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Quantization error	10-bit mode	D	E_Q	—	—	±0.5	LSB[2]
	8-bit mode			—	—	±0.5	

Table 3-9. 5 Volt 10-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Input leakage error Pad leakage[3] * R_{AS}	10-bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[2]
	8-bit mode			—	±0.1	±1	

1 Typical values assume V_{DDAD} = 5.0V, Temp = 25C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electricals.

3.9 Internal Clock Generation Module Characteristics

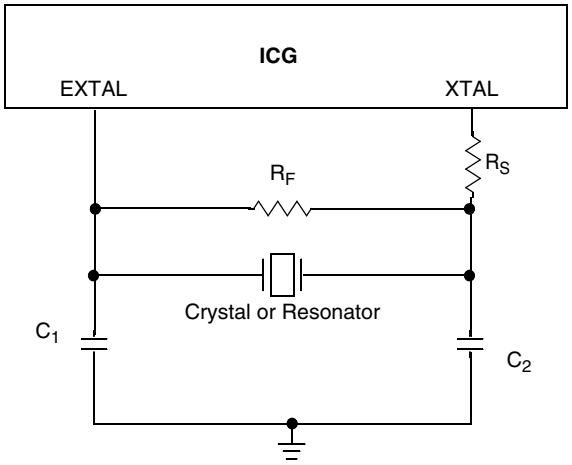


Table 3-10. ICG DC Electrical Specifications (Temperature Range = –40 to 125°C Ambient)

Characteristic	Symbol	Min	Typ[1]	Max	Unit
Load capacitors	C_1 C_2	See Note [2]			
Feedback resistor Low range (32k to 100 kHz) High range (1M – 16 MHz)	R_F		10 1		MΩ MΩ
Series resistor Low range Low Gain (HGO = 0) High Gain (HGO = 1) High range Low Gain (HGO = 0) High Gain (HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 10 20	 — — — — — —	 kΩ

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C or is typical recommended value.

2 See crystal or resonator manufacturer's recommendation.

3.9.1 ICG Frequency Specifications

Table 3-11. ICG Frequency Specifications

(V_{DDA} = V_{DDA} (min) to V_{DDA} (max), Temperature Range = –40 to 125°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1		Oscillator crystal or resonator (REFS = 1) (Fundamental mode crystal or ceramic resonator) Low range High range High Gain, FBE (HGO = 1,CLKS = 10) High Gain, FEE (HGO = 1,CLKS = 11) Low Power, FBE (HGO = 0, CLKS = 10) Low Power, FEE (HGO = 0, CLKS = 11)	 flo fhi_byp fhi_eng flp_byp flp_eng	 32 1 2 1 2	 — — — 	 100 16 10 8 8	 kHz MHz MHz MHz MHz
2		Input clock frequency (CLKS = 11, REFS = 0) Low range High range	 f_{lo} f_{hi_eng}	 32 2	 — —	 100 10	 kHz MHz
3		Input clock frequency (CLKS = 10, REFS = 0)	f_{Extal}	0	—	40	MHz
4		Internal reference frequency (untrimmed)	$f_{ICGIRCLK}$	182.25	243	303.75	kHz
5		Duty cycle of input clock (REFS = 0)	t_{dc}	40	—	60	%
6		Output clock ICGOUT frequency CLKS = 10, REFS = 0 All other cases	f_{ICGOUT}	f_{Extal} (min) f_{lo} (min)	— —	f_{Extal} (max) $f_{ICGDCLKmax}$(max)	MHz
7		Minimum DCO clock (ICGDCLK) frequency	$f_{ICGDCLKmin}$	3	—		MHz
8		Maximum DCO clock (ICGDCLK) frequency	$f_{ICGDCLKmax}$		—	40	MHz
9		Self-clock mode (ICGOUT) frequency [2]	f_{Self}	$f_{ICGDCLKmin}$		$f_{ICGDCLKmax}$	MHz
10		Self-clock mode reset (ICGOUT) frequency	f_{Self_reset}	5.5	8	10.5	MHz
11		Loss of reference frequency [3] Low range High range	f_{LOR}	5 50		25 500	kHz
12		Loss of DCO frequency [4]	f_{LOD}	0.5		1.5	MHz
13		Crystal start-up time [5, 6] Low range High range	t_{CSTL} t_{CSTH}	— —	430 4	— —	ms
14		FLL lock time [, 7] Low range High range	t_{Lockl} t_{Lockh}	— —		2 2	ms
15		FLL frequency unlock range	n_{Unlock}	–4*N		4*N	counts
16		FLL frequency lock range	n_{Lock}	–2*N		2*N	counts
17		ICGOUT period jitter, [8] measured at f_{ICGOUT} Max Long term jitter (averaged over 2 ms interval)	C_{Jitter}	—		0.2	% f_{ICG}
18		Internal oscillator deviation from trimmed frequency[9] V_{DD} = 2.7 – 5.5 V, (constant temperature) V_{DD} = 5.0 V ±10%, –40° C to 125°C	ACC_{int}	— —	±0.5 ±0.5	±2 ±2	%

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 Self-clocked mode frequency is the frequency that the DCO generates when the FLL is open-loop.

3 Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.

4 Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

7 This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{ICGOUT}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDA} and V_{SSA} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

9 See Figure 3-9

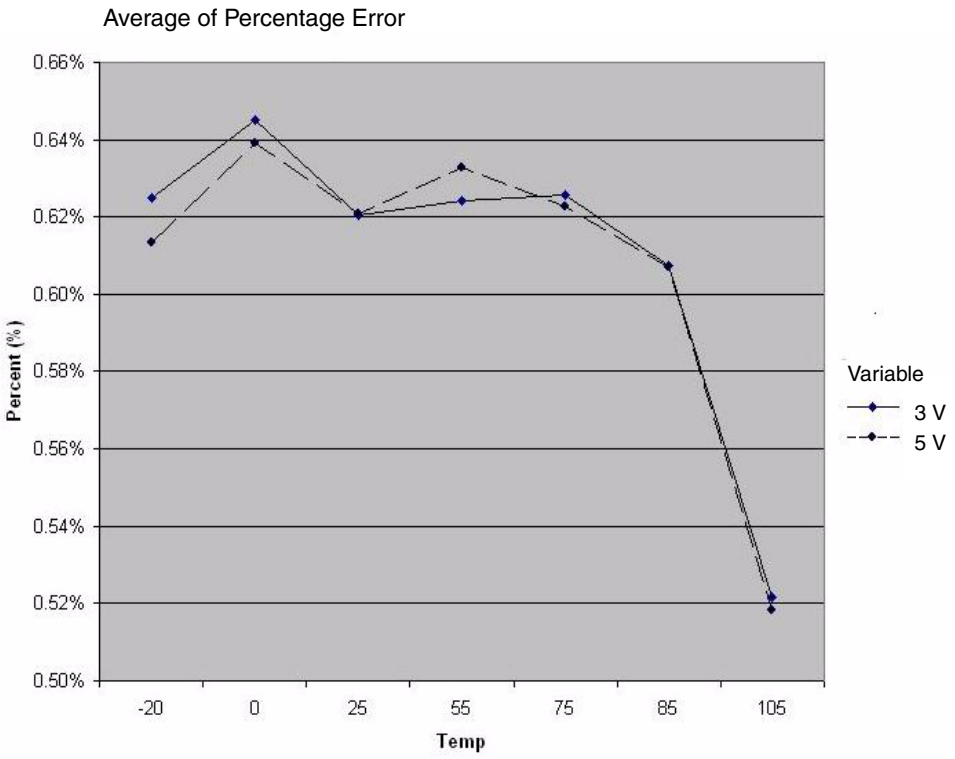


Figure 3-9. Internal Oscillator Deviation from Trimmed Frequency

3.10 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 3-12. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2		Real-time interrupt internal oscillator period	t_{RTI}	600		1500	µs
3		External reset pulse width[2] (t_{cyc} = 1/f_{Self_reset})	t_{extrst}	1.5 x t_{Self_reset}		—	ns
4		Reset low drive[3]	t_{rstdrv}	34 x t_{cyc}		—	ns
5		Active background debug mode latch setup time	t_{MSSU}	25		—	ns
6		Active background debug mode latch hold time	t_{MSH}	25		—	ns
7		IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8		KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9		Port rise and fall time (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 3 30	 	ns

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 When any reset is initiated, internal circuitry drives the reset pin low for about 34 bus cycles and then samples the level on the reset pin about 38 bus cycles later to distinguish external reset requests from internal requests.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 125°C.

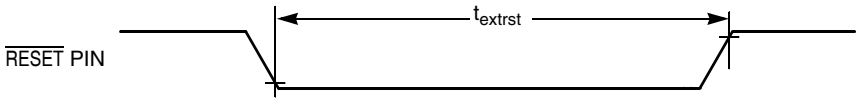


Figure 3-10. Reset Timing

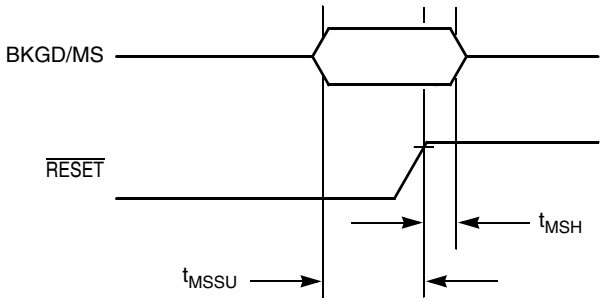


Figure 3-11. Active Background Debug Mode Latch Timing

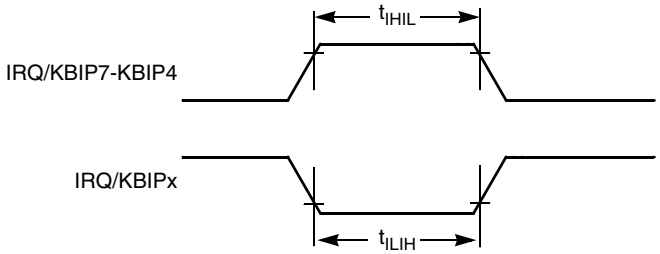


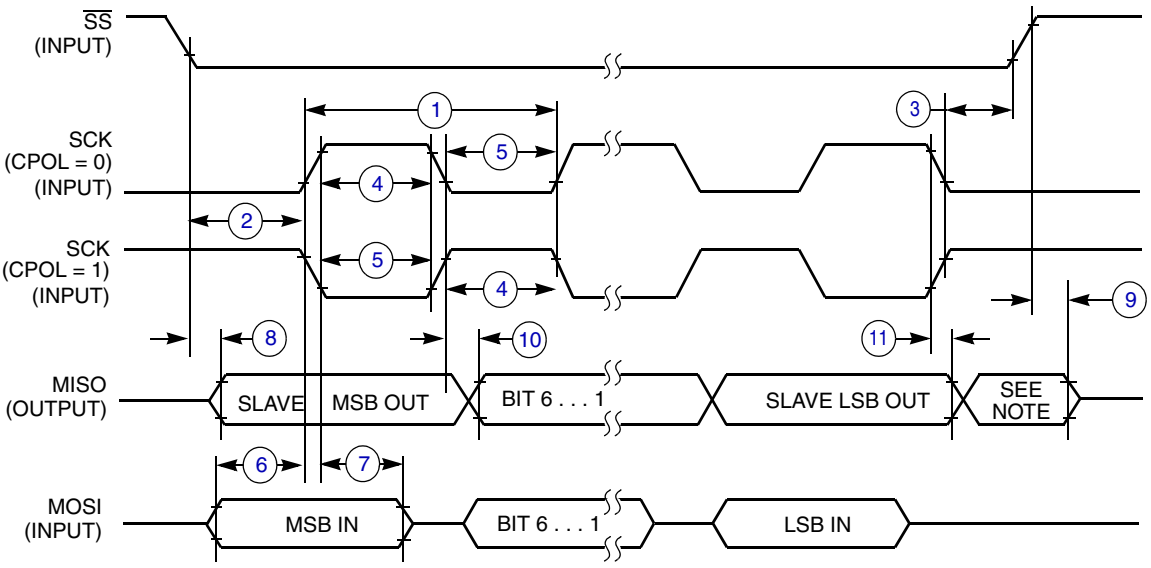
Figure 3-12. IRQ/KBIPx Timing

3.10.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

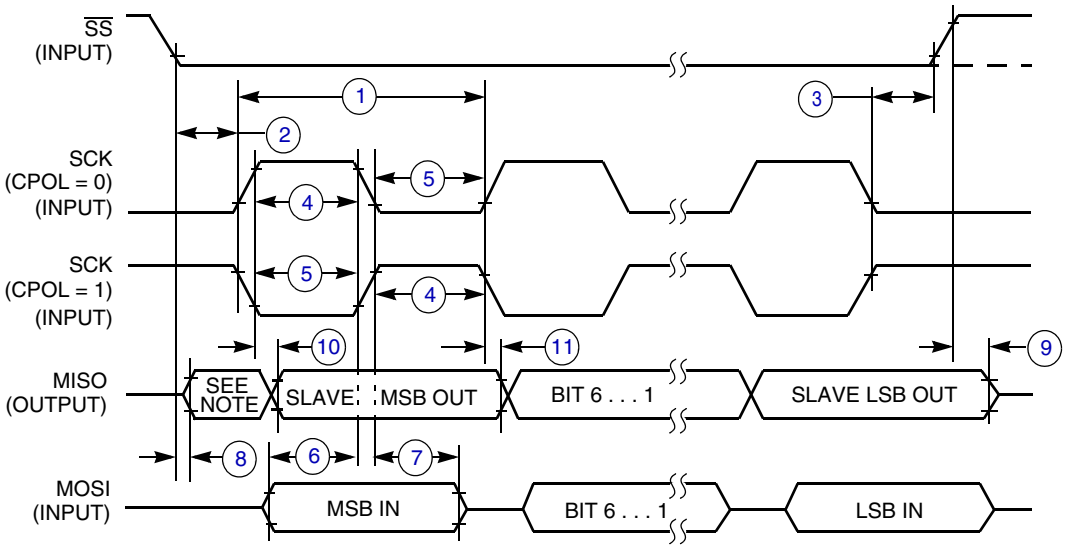
Table 3-13. TPM Input Timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
External clock period	t_{TPMext}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}



NOTE:
1. Not defined but normally MSB of character just received

Figure 3-17. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 3-18. SPI Slave Timing (CPHA = 1)

3.13 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 3-16. Radiated Emissions

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field and magnetic field	V_{RE_TEM}	V_{DD} = 5.0 V T_A = +25°C package type 80 LQFP	0.15 – 50 MHz	32kHz crystal 20MHz Bus	30	dBμV
			50 – 150 MHz		32	
			150 – 500 MHz		19	
			500 – 1000 MHz		7	
			IEC Level		I^2	—
			SAE Level		I^2	—

1 Data based on laboratory test results.

2 IEC and SAE Level Maximums: I=36 dBuV.

Chapter 5
Revision History

To provide the most up-to-date information, the version of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	9/2008	Initial release of a separate data sheet and reference manual. Removed PTH7, clarified SPI as one full and one master-only, added missing RoHS logo, updated back cover addresses, and incorporated general release edits and updates. Added some finalized electrical characteristics.
2	6/2009	Added the parameter “Bandgap Voltage Reference” in Table 3-6 Updated Section 3.13, “EMC Performance” and corrected Table 3-16. Updated disclaimer page.
3	9/2010	Added 48-pin QFN package information.
4	8/2011	Updated the t_{RTI} in the Table 3-12. Updated the RI_{DD} in the Table 3-7.