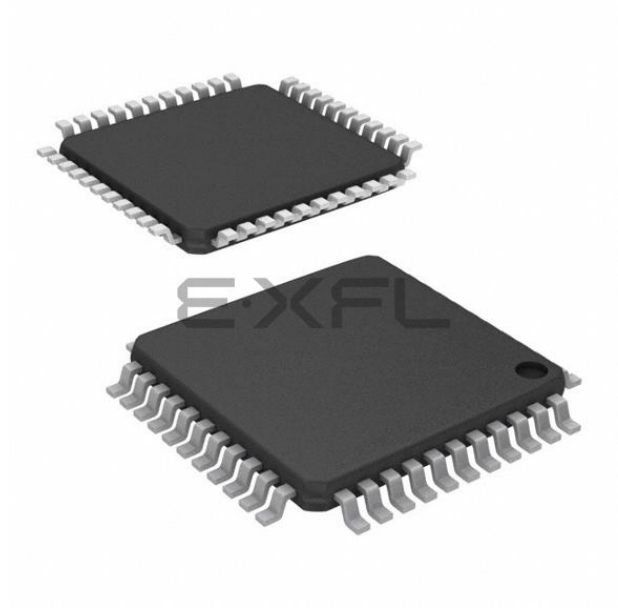

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08ac128mfge

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Chapter 1
Device Overview

The MC9S08AC128 is a member of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). The MC9S08AC128 uses the enhanced HCS08 core.

1.1 MCU Block Diagram

The block diagram in Figure 1-1 shows the structure of the MC9S08AC128 Series MCU.

Chapter 2
Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

2.1 Device Pin Assignment

Figure 2-1 shows the 80-pin LQFP package pin assignments for the MC9S08AC128 Series device.

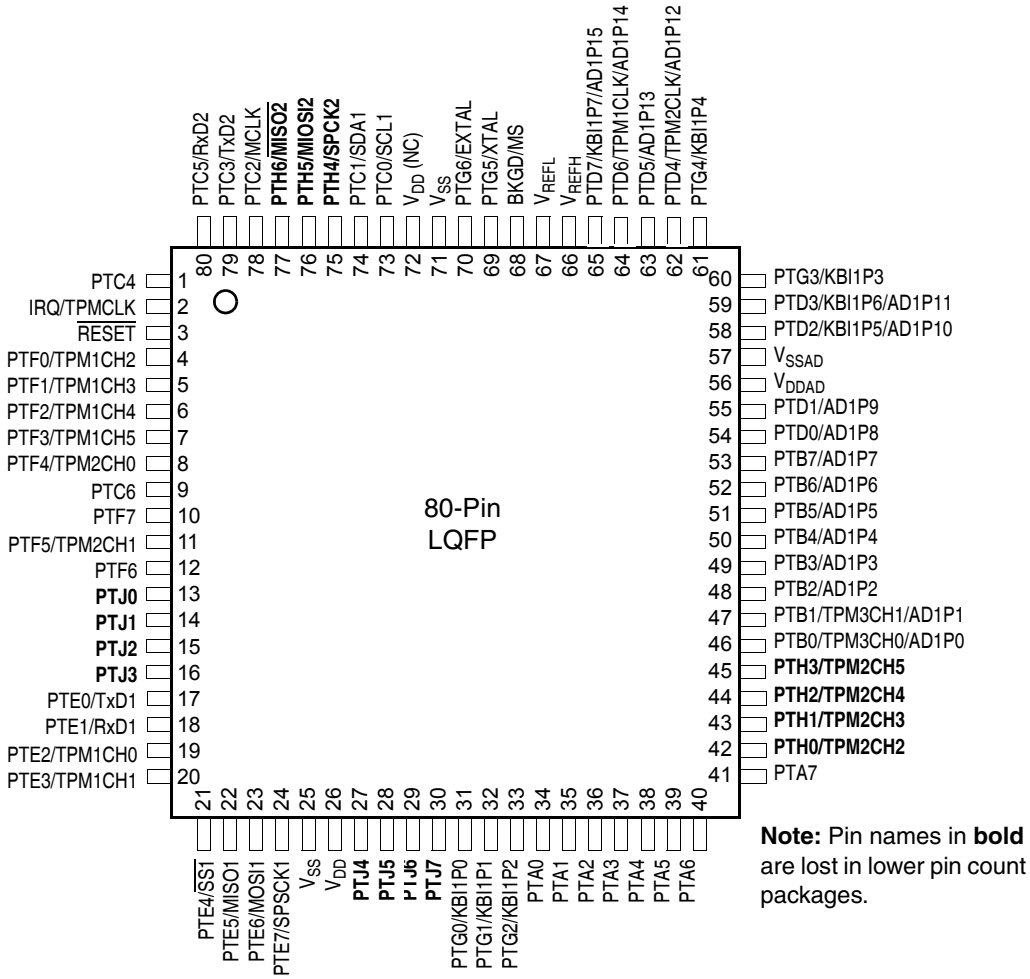
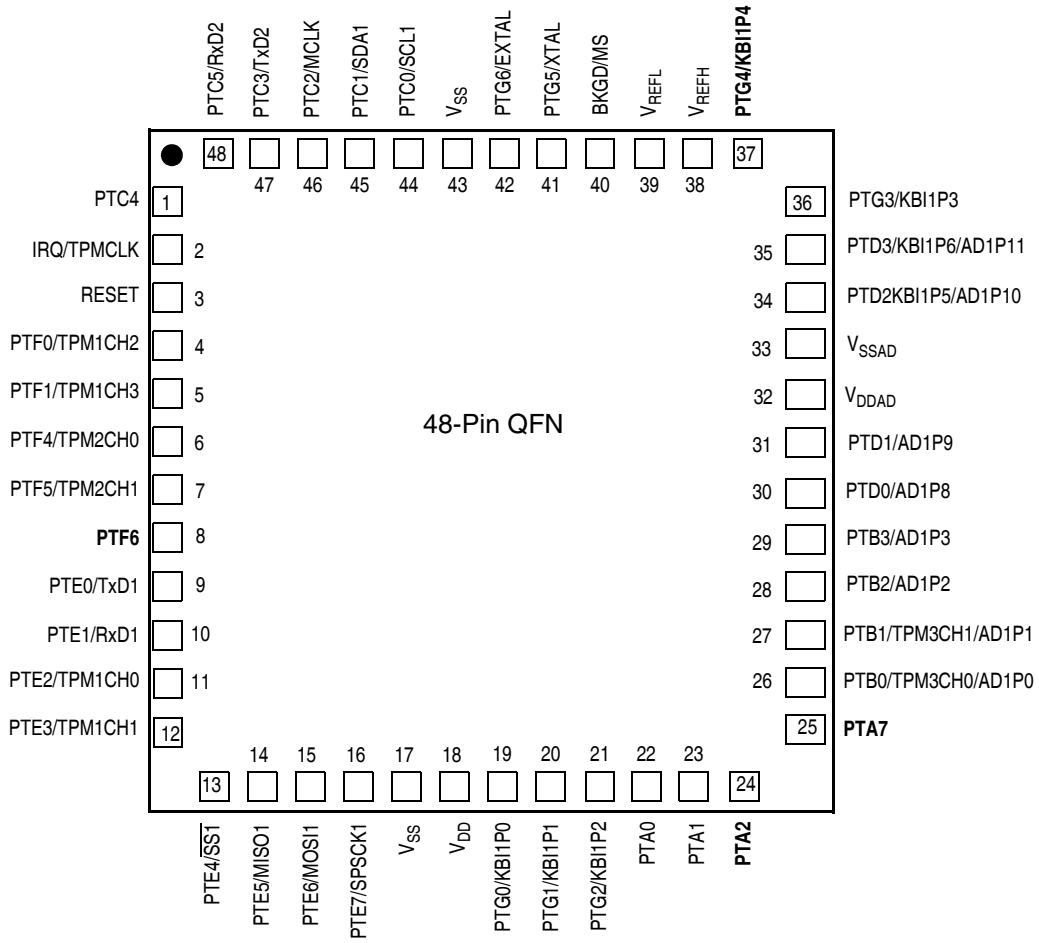


Figure 2-1. MC9S08AC128 Series in 80-Pin LQFP Package

Figure 2-1 shows the 48-pin package assignments for the MC9S08AC128 Series devices.



Note: Pin names in **bold** are lost in lower pin count packages.

Figure 2-1. MC9S08AC128 Series in 48-Pin QFN Package

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <-- Priority --> Highest		
80	**64**	**48**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
13	—	—	—	PTJ0		
14	—	—	—	PTJ1		
15	—	—	—	PTJ2		
16	—	—	—	PTJ3		
17	13	9	8	PTE0	TxD1	
18	14	10	9	PTE1	RxD1	
19	15	11	10	PTE2	TPM1CH0	
20	16	12	11	PTE3	TPM1CH1	
21	17	13	12	PTE4	$\overline{SS1}$	
22	18	14	13	PTE5	MISO1	
23	19	15	14	PTE6	MOSI1	
24	20	16	15	PTE7	SPSCK1	
25	21	17	16	V_{SS}		
26	22	18	17	V_{DD}		
27	—	—	—	PTJ4		
28	—	—	—	PTJ5		
29	—	—	—	PTJ6		
30	—	—	—	PTJ7		
31	23	19	18	PTG0	KBI1P0	
32	24	20	19	PTG1	KBI1P1	
33	25	21	20	PTG2	KBI1P2	
34	26	22	21	PTA0		
35	27	23	22	PTA1		
36	28	24	—	PTA2		
37	29	—	—	PTA3		
38	30	—	—	PTA4		
39	31	—	—	PTA5		
40	32	—	—	PTA6		
41	33	25	—	PTA7		
42	—	—	—	PTH0	TPM2CH2	
43	—	—	—	PTH1	TPM2CH3	
44	—	—	—	PTH2	TPM2CH4	
45	—	—	—	PTH3	TPM2CH5	
46	34	26	23	PTB0	TPM3CH0	AD1P0
47	35	27	24	PTB1	TPM3CH1	AD1P1
48	36	28	25	PTB2	AD1P2	
49	37	29	26	PTB3	AD1P3	
50	38	—	—	PTB4	AD1P4	
51	39	—	—	PTB5	AD1P5	
52	40	—	—	PTB6	AD1P6	
53	41	—	—	PTB7	AD1P7	

Table 3-2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to + 5.8	V
Input voltage	V_{In}	− 0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1], [2], [3]	I_D	± 25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	−55 to +150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

Table 3-6. DC Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	—	Operating Voltage	V_{DD}	2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA 5 V, I_{Load} = –0.4 mA 3 V, I_{Load} = –0.24 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
	P	Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA 5 V, I_{Load} = 0.4 mA 3 V, I_{Load} = 0.24 mA	V_{OL}	 — — — —	 — — — —	 1.5 1.5 0.8 0.8	V
	P	Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.4 mA		 — — — —	 — — — —	 1.5 1.5 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5V 3V	I_{OLT}	 — —	 — —	 100 60	mA
6	P	Input high voltage; all digital inputs 2.7v ≤ V_{DD} 4.5v	V_{IH}	0.70xV_{DD}	—	—	V
		4.5v ≤ V_{DD} ≤ 5.5v	V_{IH}	0.65xV_{DD}	—	—	
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 x V_{DD}	
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}			mV
9	P	Input leakage current; input only pins[2]	$\|I_{In}\|$	—	0.1	1	µA
10	P	High Impedance (off-state) leakage current[2]	$\|I_{OZ}\|$	—	0.1	1	µA
11	P	Internal pullup resistors[3]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V
15	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
16	D	POR rearm time	t_{POR}	10	—	—	µs
17	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVDH}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
18	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVDL}	 2.48 2.54	 2.56 2.62	 2.64 2.7	V

Table 3-6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
19	P	Low-voltage warning threshold — high range V_{DD} falling V_{DD} rising	V_{LVWH}	4.2 4.3	4.3 4.4	4.4 4.5	V
20	P	Low-voltage warning threshold — low range V_{DD} falling V_{DD} rising	V_{LVWL}	2.48 2.54	2.56 2.62	2.64 2.7	V
21	P	Low-voltage inhibit reset/recover hysteresis 5V 3V	V_{hys}	— —	100 60	— —	mV
22	P	Bandgap Voltage Reference[5]	V_{BG}	1.170	1.200	1.230	V

1 Typical values are based on characterization data at 25°C unless otherwise stated.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 Factory trimmed at V_{DD} = 3.0 V, Temperature = 25 °C.

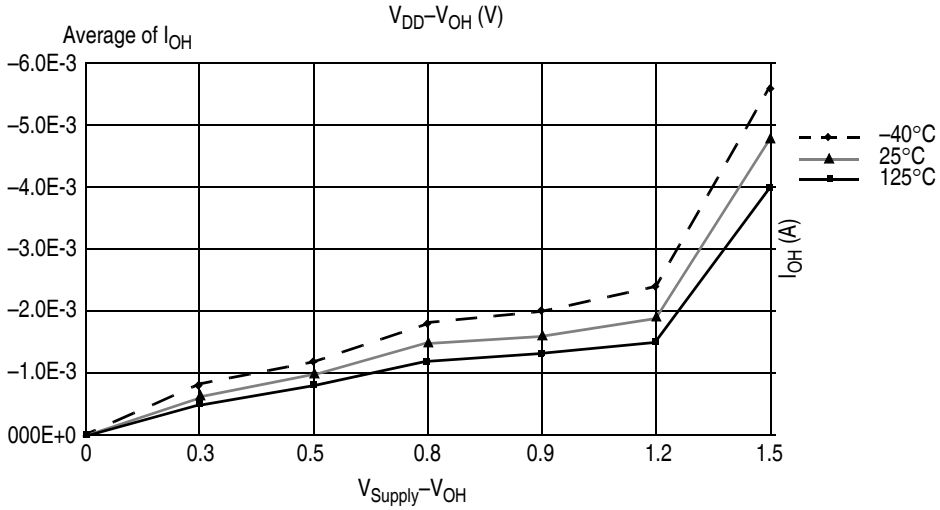


Figure 3-1. Typical I_{OH} (Low Drive) vs V_{DD}–V_{OH} at V_{DD} = 3 V

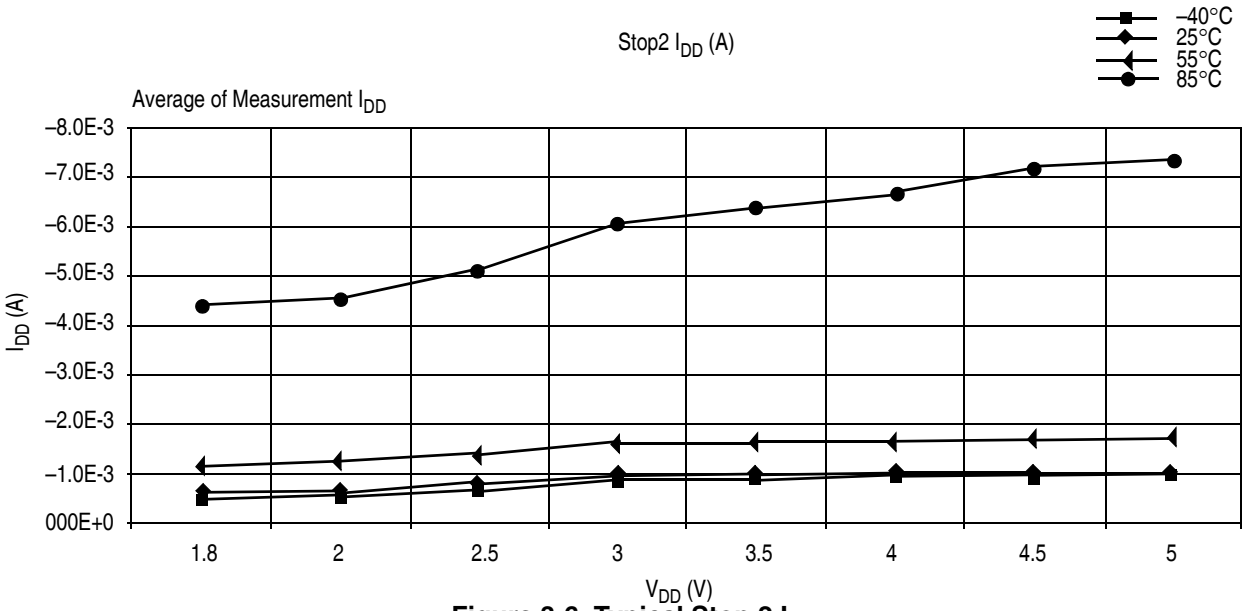


Figure 3-6. Typical Stop 2 I_{DD}

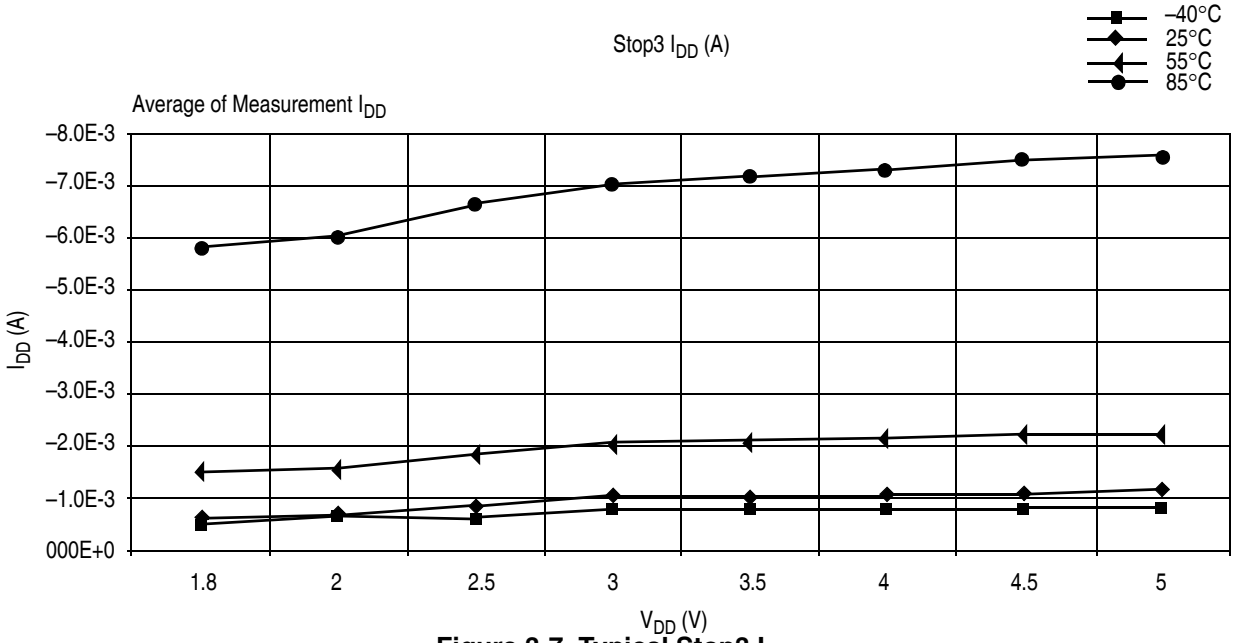


Figure 3-7. Typical Stop3 I_{DD}

3.9.1 ICG Frequency Specifications

Table 3-11. ICG Frequency Specifications

(V_{DDA} = V_{DDA} (min) to V_{DDA} (max), Temperature Range = –40 to 125°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1		Oscillator crystal or resonator (REFS = 1) (Fundamental mode crystal or ceramic resonator) Low range High range High Gain, FBE (HGO = 1,CLKS = 10) High Gain, FEE (HGO = 1,CLKS = 11) Low Power, FBE (HGO = 0, CLKS = 10) Low Power, FEE (HGO = 0, CLKS = 11)	 flo fhi_byp fhi_eng flp_byp flp_eng	 32 1 2 1 2	 — — — 	 100 16 10 8 8	 kHz MHz MHz MHz MHz
2		Input clock frequency (CLKS = 11, REFS = 0) Low range High range	 f_{lo} f_{hi_eng}	 32 2	 — —	 100 10	 kHz MHz
3		Input clock frequency (CLKS = 10, REFS = 0)	f_{Extal}	0	—	40	MHz
4		Internal reference frequency (untrimmed)	$f_{ICGIRCLK}$	182.25	243	303.75	kHz
5		Duty cycle of input clock (REFS = 0)	t_{dc}	40	—	60	%
6		Output clock ICGOUT frequency CLKS = 10, REFS = 0 All other cases	f_{ICGOUT}	f_{Extal} (min) f_{lo} (min)	— —	f_{Extal} (max) $f_{ICGDCLKmax}$(max)	MHz
7		Minimum DCO clock (ICGDCLK) frequency	$f_{ICGDCLKmin}$	3	—		MHz
8		Maximum DCO clock (ICGDCLK) frequency	$f_{ICGDCLKmax}$		—	40	MHz
9		Self-clock mode (ICGOUT) frequency [2]	f_{Self}	$f_{ICGDCLKmin}$		$f_{ICGDCLKmax}$	MHz
10		Self-clock mode reset (ICGOUT) frequency	f_{Self_reset}	5.5	8	10.5	MHz
11		Loss of reference frequency [3] Low range High range	f_{LOR}	5 50		25 500	kHz
12		Loss of DCO frequency [4]	f_{LOD}	0.5		1.5	MHz
13		Crystal start-up time [5, 6] Low range High range	t_{CSTL} t_{CSTH}	— —	430 4	— —	ms
14		FLL lock time [, 7] Low range High range	t_{Lockl} t_{Lockh}	— —		2 2	ms
15		FLL frequency unlock range	n_{Unlock}	–4*N		4*N	counts
16		FLL frequency lock range	n_{Lock}	–2*N		2*N	counts
17		ICGOUT period jitter, [8] measured at f_{ICGOUT} Max Long term jitter (averaged over 2 ms interval)	C_{Jitter}	—		0.2	% f_{ICG}
18		Internal oscillator deviation from trimmed frequency[9] V_{DD} = 2.7 – 5.5 V, (constant temperature) V_{DD} = 5.0 V ±10%, –40° C to 125°C	ACC_{int}	— —	±0.5 ±0.5	±2 ±2	%

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 Self-clocked mode frequency is the frequency that the DCO generates when the FLL is open-loop.

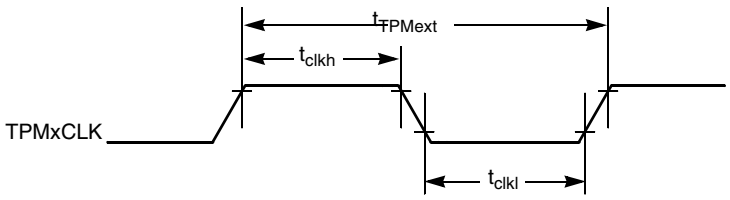


Figure 3-13. Timer External Clock

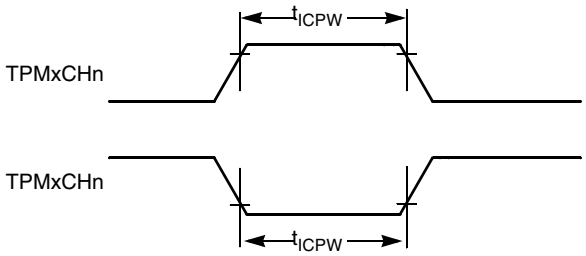


Figure 3-14. Timer Input Capture Pulse

3.11 SPI Characteristics

Table 3-14 and Figure 3-15 through Figure 3-18 describe the timing requirements for the SPI system.

Table 3-14. SPI Electrical Characteristic

Num[1]	C	Characteristic[2]	Symbol	Min	Max	Unit
		Operating frequency[3] Master Slave	 f_{op} f_{op}	 $f_{Bus}/2048$ dc	 $f_{Bus}/2$ $f_{Bus}/4$	Hz
1		Cycle time Master Slave	 t_{SCK} t_{SCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
2		Enable lead time Master Slave	 t_{Lead} t_{Lead}	 — 1/2	 1/2 —	 t_{SCK} t_{SCK}
3		Enable lag time Master Slave	 t_{Lag} t_{Lag}	 — 1/2	 1/2 —	 t_{SCK} t_{SCK}
4		Clock (SPSCK) high time Master and Slave	t_{SCKH}	1/2 t_{SCK} – 25	—	ns
5		Clock (SPSCK) low time Master and Slave	t_{SCKL}	1/2 t_{SCK} – 25	—	ns
6		Data setup time (inputs) Master Slave	 $t_{SI(M)}$ $t_{SI(S)}$	 30 30	 — —	 ns ns
7		Data hold time (inputs) Master Slave	 $t_{HI(M)}$ $t_{HI(S)}$	 30 30	 — —	 ns ns
8		Access time, slave[4]	t_A	0	40	ns
9		Disable time, slave[5]	t_{dis}	—	40	ns
10		Data setup time (outputs) Master Slave	 t_{SO} t_{SO}	 25 25	 — —	 ns ns
11		Data hold time (outputs) Master Slave	 t_{HO} t_{HO}	 –10 –10	 — —	 ns ns

1 Refer to Figure 3-15 through Figure 3-18.

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Maximum baud rate must be limited to 5 MHz due to pad input characteristics.

4 Time to data active from high-impedance state.

5 Hold time to high-impedance state.

3.12 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 3-15. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	P	Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2	P	Supply voltage for read operation	V_{Read}	2.7		5.5	V
3	P	Internal FCLK frequency[2]	f_{FCLK}	150		200	kHz
4	P	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
5	P	Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
6	C	Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to + 125°C T = 25°C		10,000 —	— 100,000	— —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25°C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 **Typical endurance for Flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

3.13 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 3-16. Radiated Emissions

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field and magnetic field	V_{RE_TEM}	V_{DD} = 5.0 V T_A = +25°C package type 80 LQFP	0.15 – 50 MHz	32kHz crystal 20MHz Bus	30	dBμV
			50 – 150 MHz		32	
			150 – 500 MHz		19	
			500 – 1000 MHz		7	
			IEC Level		I^2	—
			SAE Level		I^2	—

1 Data based on laboratory test results.

2 IEC and SAE Level Maximums: I=36 dBuV.

Chapter 4
Ordering Information and Mechanical Drawings

4.1 Ordering Information

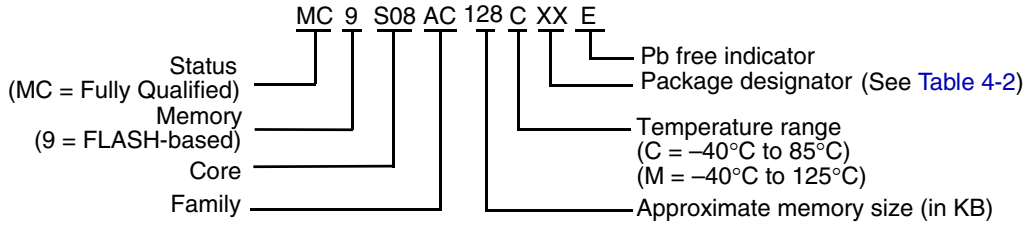
This section contains ordering numbers for MC9S08AC128 Series devices. See below for an example of the device numbering system.

Table 4-1. Device Numbering System

Device Number	Memory		Available Packages[1]
	FLASH	RAM	Type
MC9S08AC128	128K	8K	80 LQFP, 64 QFP, 48-QFN, 44-LQFP
MC9S08AC96	96K	6K	80 LQFP, 64 QFP, 48-QFN, 44-LQFP

1 See Table 4-2 for package information.

4.2 Orderable Part Numbering System



4.3 Mechanical Drawings

Table 4-2 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08AC128 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 4-2, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 4-2) in the "Enter Keyword" search box at the top of the page.

Table 4-2. Package Information

Pin Count	Type	Designator	Document No.
80	LQFP	LK	98ASS23237W
64	QFP	FU	98ASB42844B
48	QFN	FT	98ARH99048A
44	LQFP	FG	98ASS23225W

Chapter 5
Revision History

To provide the most up-to-date information, the version of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	9/2008	Initial release of a separate data sheet and reference manual. Removed PTH7, clarified SPI as one full and one master-only, added missing RoHS logo, updated back cover addresses, and incorporated general release edits and updates. Added some finalized electrical characteristics.
2	6/2009	Added the parameter “Bandgap Voltage Reference” in Table 3-6 Updated Section 3.13, “EMC Performance” and corrected Table 3-16. Updated disclaimer page.
3	9/2010	Added 48-pin QFN package information.
4	8/2011	Updated the t_{RTI} in the Table 3-12. Updated the RI_{DD} in the Table 3-7.

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