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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08ac128mfue">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08ac128mfue</a>

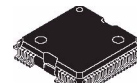
# MC9S08AC128 8-Bit Microcontroller Data Sheet

## MC9S08AC128

917A-03

840B-01

824D-02



### 8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 20-MHz internal bus frequency
- HC08 instruction set with added BGND, CALL and RTC instructions
- Memory Management Unit to support paged memory.
- Linear Address Pointer to allow direct page data accesses of the entire memory map

### Development Support

- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip in-circuit emulator (ICE) Debug module containing three comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Supports both tag and force breakpoints.

### Memory Options

- Up to 128K FLASH — read/program/erase over full operating voltage and temperature
- Up to 8K Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and FLASH contents

### Clock Source Options

- Clock source options include crystal, resonator, external clock, or internally generated clock with precision NVM trimming using ICG module

### System Protection

- Optional computer operating properly (COP) reset with option to run from independent internal clock source or bus clock
- CRC module to support fast cyclic redundancy checks on system memory
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Master reset pin and power-on reset (POR)

### Power-Saving Modes

- Wait plus two stops

### Peripherals

- **ADC** — 16-channel, 10-bit resolution, 2.5  $\mu$ s conversion time, automatic compare function, temperature sensor, internal bandgap reference channel
- **SC1x** — Two serial communications interface modules supporting LIN 2.0 Protocol and SAE J2602 protocols; Full duplex non-return to zero (NRZ); Master extended break generation; Slave extended break detection; Wakeup on active edge
- **SPIx** — One full and one master-only serial peripheral interface modules; Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Inter-integrated circuit bus module; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- **TPMx** — One 2-channel and two 6-channel 16-bit timer/pulse-width modulator (TPM) modules: Selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels
- **KBI** — 8-pin keyboard interrupt module

### Input/Output

- Up to 70 general-purpose input/output pins
- Software selectable pullups on input port pins
- Software selectable drive strength and slew rate control on ports when used as outputs

### Package Options

- 80-pin low-profile quad flat package (LQFP)
- 64-pin quad flat package (QFP)
- 48-pin quad flat no-lead package (QFN)
- 44-pin low-profile quad flat package (LQFP)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

# Chapter 2

## Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

### 2.1 Device Pin Assignment

Figure 2-1 shows the 80-pin LQFP package pin assignments for the MC9S08AC128 Series device.

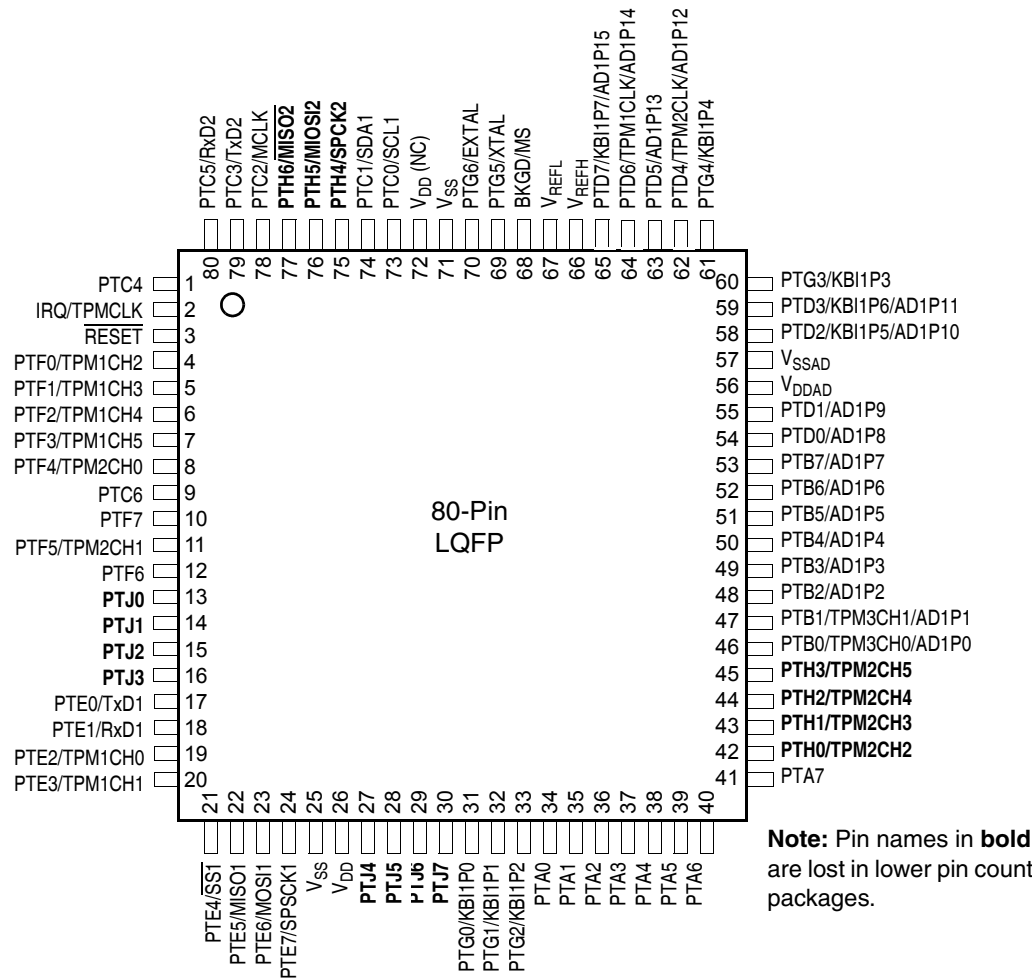
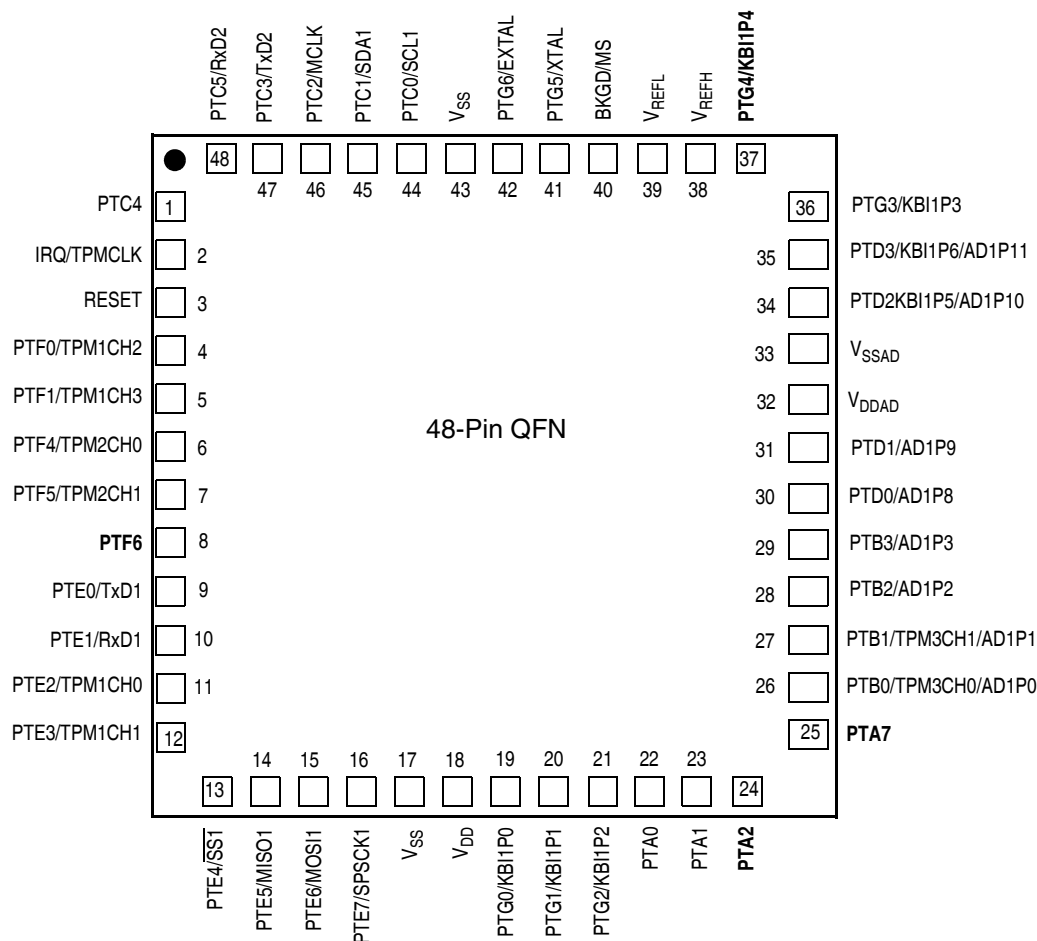


Figure 2-1. MC9S08AC128 Series in 80-Pin LQFP Package

Figure 2-1 shows the 48-pin package assignments for the MC9S08AC128 Series devices.



**Note:** Pin names in **bold** are lost in lower pin count packages.

Figure 2-1. MC9S08AC128 Series in 48-Pin QFN Package

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <--	Priority	--> Highest
80	64	48	44	Port Pin	Alt 1	Alt 2
13	—	—	—	PTJ0		
14	—	—	—	PTJ1		
15	—	—	—	PTJ2		
16	—	—	—	PTJ3		
17	13	9	8	PTE0	TxD1	
18	14	10	9	PTE1	RxD1	
19	15	11	10	PTE2	TPM1CH0	
20	16	12	11	PTE3	TPM1CH1	
21	17	13	12	PTE4	$\overline{SS1}$	
22	18	14	13	PTE5	MISO1	
23	19	15	14	PTE6	MOSI1	
24	20	16	15	PTE7	SPSCK1	
25	21	17	16	V <sub>SS</sub>		
26	22	18	17	V <sub>DD</sub>		
27	—	—	—	PTJ4		
28	—	—	—	PTJ5		
29	—	—	—	PTJ6		
30	—	—	—	PTJ7		
31	23	19	18	PTG0	KBI1P0	
32	24	20	19	PTG1	KBI1P1	
33	25	21	20	PTG2	KBI1P2	
34	26	22	21	PTA0		
35	27	23	22	PTA1		
36	28	24	—	PTA2		
37	29	—	—	PTA3		
38	30	—	—	PTA4		
39	31	—	—	PTA5		
40	32	—	—	PTA6		
41	33	25	—	PTA7		
42	—	—	—	PTH0	TPM2CH2	
43	—	—	—	PTH1	TPM2CH3	
44	—	—	—	PTH2	TPM2CH4	
45	—	—	—	PTH3	TPM2CH5	
46	34	26	23	PTB0	TPM3CH0	AD1P0
47	35	27	24	PTB1	TPM3CH1	AD1P1
48	36	28	25	PTB2	AD1P2	
49	37	29	26	PTB3	AD1P3	
50	38	—	—	PTB4	AD1P4	
51	39	—	—	PTB5	AD1P5	
52	40	—	—	PTB6	AD1P6	
53	41	—	—	PTB7	AD1P7	

**Table 3-2. Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	-0.3 to + 5.8	V
Input voltage	$V_{In}$	- 0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	± 25	mA
Maximum current into $V_{DD}$	$I_{DD}$	120	mA
Storage temperature	$T_{stg}$	-55 to +150	°C

<sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.

<sup>2</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>3</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

Table 3-6. DC Characteristics

Num	C	Parameter	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	—	Operating Voltage	$V_{DD}$	2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = -2$ mA 3 V, $I_{Load} = -0.6$ mA 5 V, $I_{Load} = -0.4$ mA 3 V, $I_{Load} = -0.24$ mA	$V_{OH}$	$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	V
	P	Output high voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = -10$ mA 3 V, $I_{Load} = -3$ mA 5 V, $I_{Load} = -2$ mA 3 V, $I_{Load} = -0.4$ mA		$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 0.6$ mA 5 V, $I_{Load} = 0.4$ mA 3 V, $I_{Load} = 0.24$ mA	$V_{OL}$	— — — —	— — — —	1.5 1.5 0.8 0.8	V
	P	Output low voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = 10$ mA 3 V, $I_{Load} = 3$ mA 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 0.4$ mA		— — — —	— — — —	1.5 1.5 0.8 0.8	
4	P	Output high current — Max total $I_{OH}$ for all ports 5V 3V	$I_{OHT}$	— —	— —	100 60	mA
5	P	Output low current — Max total $I_{OL}$ for all ports 5V 3V	$I_{OLT}$	— —	— —	100 60	mA
6	P	Input high voltage; all digital inputs $2.7v \leq V_{DD} < 4.5v$ $4.5v \leq V_{DD} \leq 5.5v$	$V_{IH}$	$0.70 \times V_{DD}$ $0.65 \times V_{DD}$	— —	— —	V
		Input low voltage; all digital inputs	$V_{IL}$	—	—	$0.35 \times V_{DD}$	
7	P	Input hysteresis; all digital inputs	$V_{hys}$	$0.06 \times V_{DD}$			mV
9	P	Input leakage current; input only pins <sup>2</sup>	$ I_{In} $	—	0.1	1	$\mu A$
10	P	High Impedance (off-state) leakage current <sup>2</sup>	$ I_{OZ} $	—	0.1	1	$\mu A$
11	P	Internal pullup resistors <sup>3</sup>	$R_{PU}$	20	45	65	k $\Omega$
12	P	Internal pulldown resistors <sup>4</sup>	$R_{PD}$	20	45	65	k $\Omega$
13	C	Input Capacitance; all non-supply pins	$C_{In}$	—	—	8	pF
14	D	RAM retention voltage	$V_{RAM}$	—	0.6	1.0	V
15	P	POR rearm voltage	$V_{POR}$	0.9	1.4	2.0	V
16	D	POR rearm time	$t_{POR}$	10	—	—	$\mu s$
17	P	Low-voltage detection threshold — high range $V_{DD}$ falling $V_{DD}$ rising	$V_{LVDH}$	4.2 4.3	4.3 4.4	4.4 4.5	V
		Low-voltage detection threshold — low range $V_{DD}$ falling $V_{DD}$ rising		2.48 2.54	2.56 2.62	2.64 2.7	

Table 3-6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typ <sup>1</sup>	Max	Unit
19	P	Low-voltage warning threshold — high range $V_{DD}$ falling $V_{DD}$ rising	$V_{LVWH}$	4.2 4.3	4.3 4.4	4.4 4.5	V
20	P	Low-voltage warning threshold — low range $V_{DD}$ falling $V_{DD}$ rising	$V_{LVWL}$	2.48 2.54	2.56 2.62	2.64 2.7	V
21	P	Low-voltage inhibit reset/recover hysteresis 5V 3V	$V_{hys}$	— —	100 60	— —	mV
22	P	Bandgap Voltage Reference <sup>5</sup>	$V_{BG}$	1.170	1.200	1.230	V

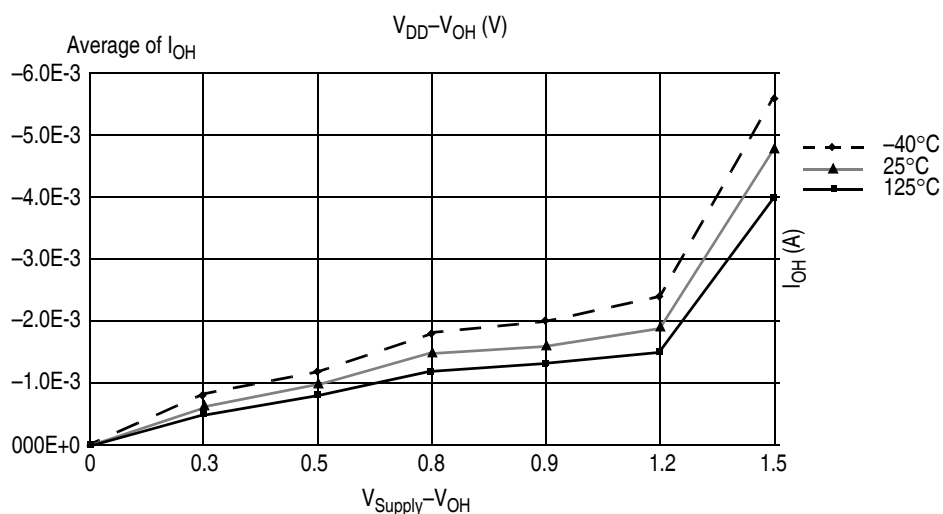
<sup>1</sup> Typical values are based on characterization data at 25°C unless otherwise stated.

<sup>2</sup> Measured with  $V_{In} = V_{DD}$  or  $V_{SS}$ .

<sup>3</sup> Measured with  $V_{In} = V_{SS}$ .

<sup>4</sup> Measured with  $V_{In} = V_{DD}$ .

<sup>5</sup> Factory trimmed at  $V_{DD} = 3.0$  V, Temperature = 25 °C.


Figure 3-1. Typical  $I_{OH}$  (Low Drive) vs  $V_{DD} - V_{OH}$  at  $V_{DD} = 3$  V



## 3.7 Supply Current Characteristics

Table 3-7. Supply Current Characteristics

Num	C	Parameter	Symbol	V <sub>DD</sub> (V)	Typ <sup>1</sup>	Max	Unit	Temp (°C)
1	C	Run supply current <sup>2</sup> measured at (CPU clock = 2 MHz, f <sub>BUS</sub> = 1 MHz)	R <sub>I</sub> DD	5	1.1	1.4 <sup>3</sup>	mA	–40 to 125°C
				3	1.0	1.2		
2	C	Run supply current <sup>4</sup> measured at (CPU clock = 16 MHz, f <sub>BUS</sub> = 8 MHz)	R <sub>I</sub> DD	5	6.7	8.0 <sup>5</sup>	mA	–40 to 125°C
				3	6	7.5		
3	C	Stop2 mode supply current	S2I <sub>DD</sub>	5	1.0	25 160	μA	–40 to 85°C –40 to 125°C
				3	0.8	23 150	μA	–40 to 85°C –40 to 125°C
4	C	Stop3 mode supply current	S3I <sub>DD</sub>	5	1.2	27 180 <sup>3</sup>	μA	–40 to 85°C –40 to 125°C
				3	1.0	25 170	μA	–40 to 85°C –40 to 125°C
5	C	RTI adder to stop2 or stop3 <sup>6</sup>	S23I <sub>DDRTI</sub>	5	300	500 500	nA	–40 to 85°C –40 to 125°C
				3	300	500 500	nA	–40 to 85°C –40 to 125°C
6	C	LVD adder to stop3 (LVDE = LVDSE = 1)	S3I <sub>DDLVD</sub>	5	110	180 180	μA	–40 to 85°C –40 to 125°C
				3	90	160 160	μA	–40 to 85°C –40 to 125°C
7	C	Adder to stop3 for oscillator enabled <sup>7</sup> (OSCSTEN = 1)	S3I <sub>DDOSC</sub>	5,3	5	8 8	μA μA	–40 to 85°C –40 to 125°C

<sup>1</sup> Typical values are based on characterization data at 25°C unless otherwise stated. See Figure 3-5 through Figure 3-7 for typical curves across voltage/temperature.

<sup>2</sup> All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

<sup>3</sup> Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

<sup>4</sup> All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

<sup>5</sup> Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

<sup>6</sup> Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 560 μA at 3 V with f<sub>BUS</sub> = 1 MHz.

<sup>7</sup> Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal, low power mode (HGO = 0), clock monitor disabled (LOCD = 1).

## 3.8 ADC Characteristics

Table 3-8. 5 Volt 10-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit
Supply voltage	Absolute	$V_{DDAD}$	2.7	—	5.5	V
	Delta to $V_{DD}$ ( $V_{DD}-V_{DDAD}$ ) <sup>2</sup>	$\Delta V_{DDAD}$	-100	0	+100	mV
Ground voltage	Delta to $V_{SS}$ ( $V_{SS}-V_{SSAD}$ ) <sup>2</sup>	$\Delta V_{SSAD}$	-100	0	+100	mV
Ref voltage high		$V_{REFH}$	2.7	$V_{DDAD}$	$V_{DDAD}$	V
Ref voltage low		$V_{REFL}$	$V_{SSAD}$	$V_{SSAD}$	$V_{SSAD}$	V
Supply current	Stop, reset, module off	$I_{DDAD}$	—	0.011	1	$\mu$ A
Input voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V
Input capacitance		$C_{ADIN}$	—	4.5	5.5	pF
Input resistance		$R_{ADIN}$	—	3	5	k $\Omega$
Analog source resistance External to MCU	10-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	$R_{AS}$	— —	— —	5 10	k $\Omega$
	8-bit mode (all valid $f_{ADCK}$ )		—	—	10	
ADC conversion clock frequency	High speed (ADLPC = 0)	$f_{ADCK}$	0.4	—	8.0	MHz
	Low power (ADLPC = 1)		0.4	—	4.0	
Temp Sensor Slope	-40°C to 25°C	m	—	3.266	—	mV/°C
	25°C to 125°C			3.638	—	
Temp Sensor Voltage	25°C	$V_{TEMP25}$	—	1.396	—	V

<sup>1</sup> Typical values assume  $V_{DDAD} = 5.0\text{ V}$ , Temp = 25°C,  $f_{ADCK} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> dc potential difference.

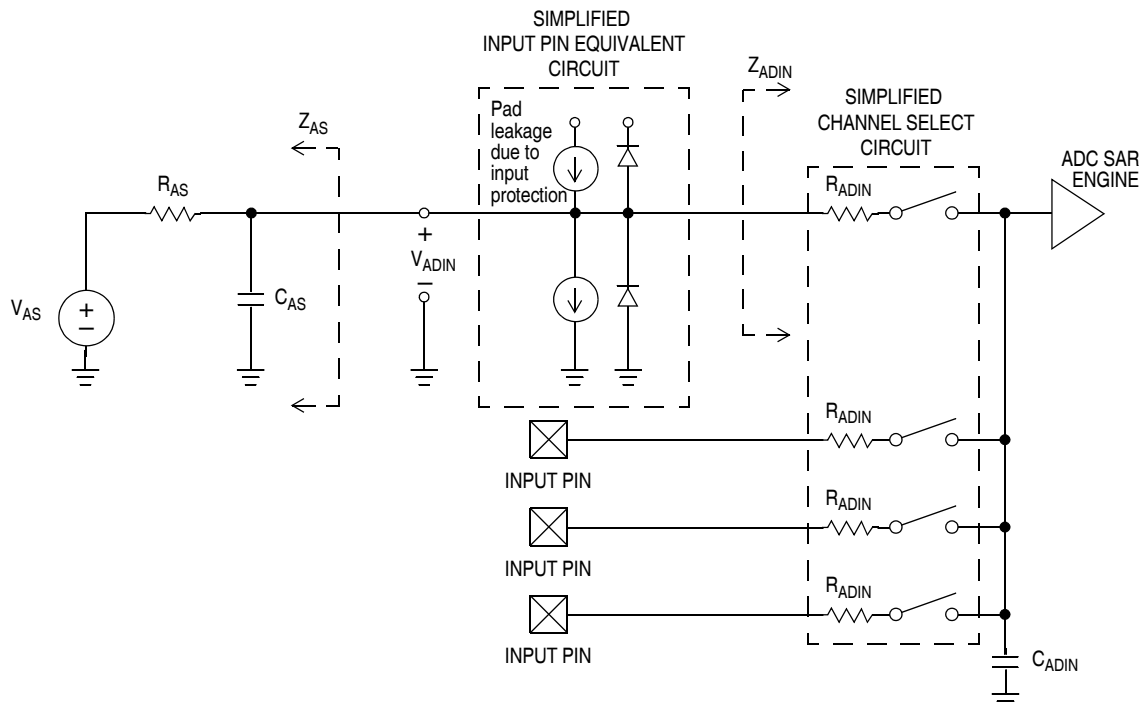


Figure 3-8. ADC Input Impedance Equivalency Diagram

**Table 3-9. 5 Volt 10-bit ADC Characteristics ( $V_{REFH} = V_{DDAD}$ ,  $V_{REFL} = V_{SSAD}$ )**

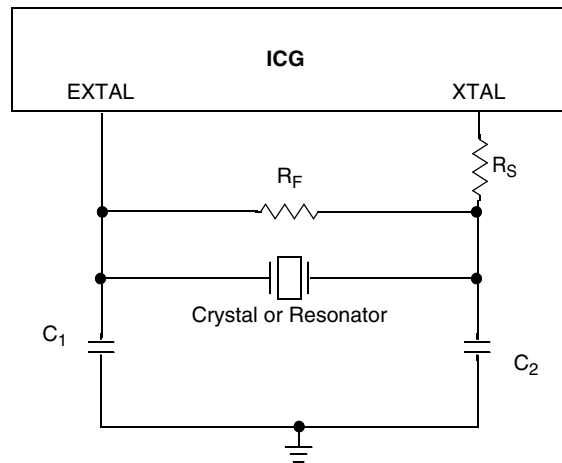
Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit
Input leakage error Pad leakage <sup>3</sup> * $R_{AS}$	10-bit mode	D	$E_{IL}$	—	±0.2	±2.5	LSB <sup>2</sup>
	8-bit mode			—	±0.1	±1	

<sup>1</sup> Typical values assume  $V_{DDAD} = 5.0V$ , Temp = 25°C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$

<sup>3</sup> Based on input pad leakage current. Refer to pad electricals.

### 3.9 Internal Clock Generation Module Characteristics



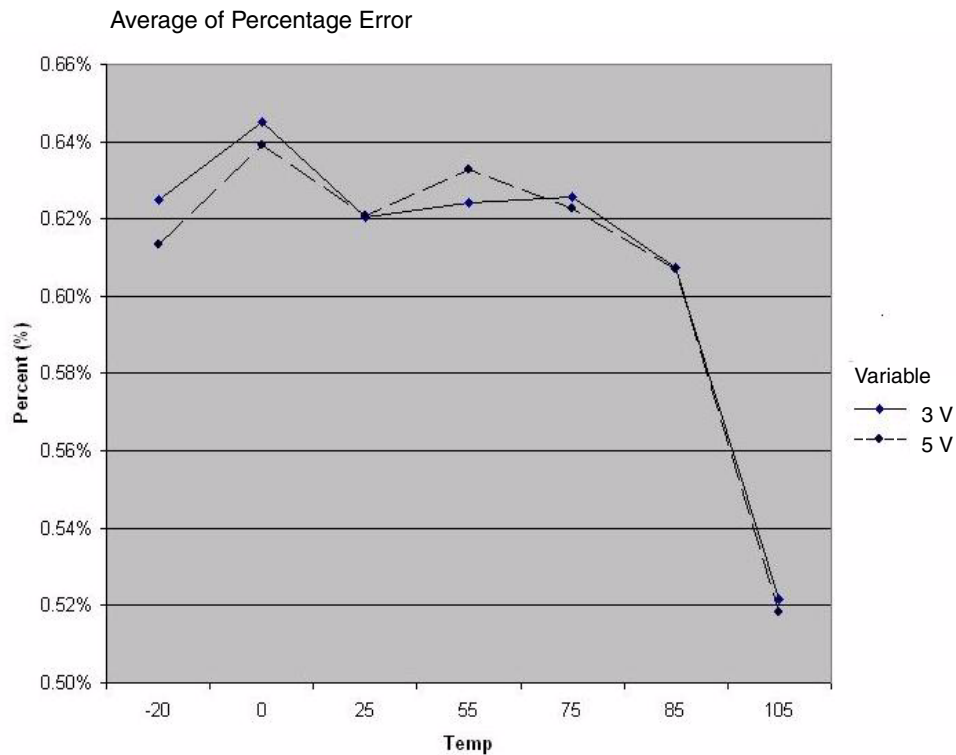
**Table 3-10. ICG DC Electrical Specifications (Temperature Range = -40 to 125°C Ambient)**

Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
Load capacitors	$C_1$ $C_2$	See Note <sup>2</sup>			
Feedback resistor	$R_F$		10 1		MΩ MΩ
Low range (32k to 100 kHz)					
High range (1M – 16 MHz)					
Series resistor	$R_S$		0 100 0 0 10 20		kΩ
Low range					
Low Gain (HGO = 0)					
High Gain (HGO = 1)					
High range					
Low Gain (HGO = 0)					
High Gain (HGO = 1)					
≥ 8 MHz					
4 MHz					
1 MHz					

<sup>1</sup> Typical values are based on characterization data at  $V_{DD} = 5.0V$ , 25°C or is typical recommended value.

<sup>2</sup> See crystal or resonator manufacturer's recommendation.

- <sup>3</sup> Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.
- <sup>4</sup> Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.
- <sup>5</sup> This parameter is characterized before qualification rather than 100% tested.
- <sup>6</sup> Proper PC board layout procedures must be followed to achieve specifications.
- <sup>7</sup> This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- <sup>8</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{ICGOUT}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via  $V_{DDA}$  and  $V_{SSA}$  and variation in crystal oscillator frequency increase the  $C_{Jitter}$  percentage for a given interval.
- <sup>9</sup> See Figure 3-9



**Figure 3-9. Internal Oscillator Deviation from Trimmed Frequency**

## 3.10 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

### 3.10.1 Control Timing

Table 3-12. Control Timing

Num	C	Parameter	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1		Bus frequency ( $t_{cyc} = 1/f_{Bus}$ )	$f_{Bus}$	dc	—	20	MHz
2		Real-time interrupt internal oscillator period	$t_{RTI}$	600		1500	$\mu s$
3		External reset pulse width <sup>2</sup> ( $t_{cyc} = 1/f_{Self\_reset}$ )	$t_{extrst}$	1.5 x $t_{Self\_reset}$		—	ns
4		Reset low drive <sup>3</sup>	$t_{rstdrv}$	34 x $t_{cyc}$		—	ns
5		Active background debug mode latch setup time	$t_{MSSU}$	25		—	ns
6		Active background debug mode latch hold time	$t_{MSH}$	25		—	ns
7		IRQ pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>4</sup>	$t_{LIH}, t_{IHIL}$	100 1.5 x $t_{cyc}$	—	—	ns
8		KBIPx pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>3</sup>	$t_{LIH}, t_{IHIL}$	100 1.5 x $t_{cyc}$	—	—	ns
9		Port rise and fall time (load = 50 pF) <sup>5</sup> Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{Rise}, t_{Fall}$	— —	3 30		ns

<sup>1</sup> Typical values are based on characterization data at  $V_{DD} = 5.0V$ , 25°C unless otherwise stated.

<sup>2</sup> This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

<sup>3</sup> When any reset is initiated, internal circuitry drives the reset pin low for about 34 bus cycles and then samples the level on the reset pin about 38 bus cycles later to distinguish external reset requests from internal requests.

<sup>4</sup> This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

<sup>5</sup> Timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  levels. Temperature range –40°C to 125°C.

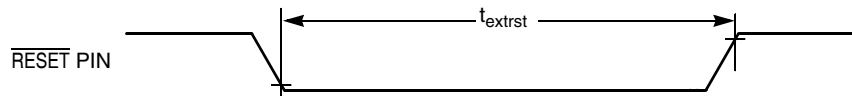


Figure 3-10. Reset Timing

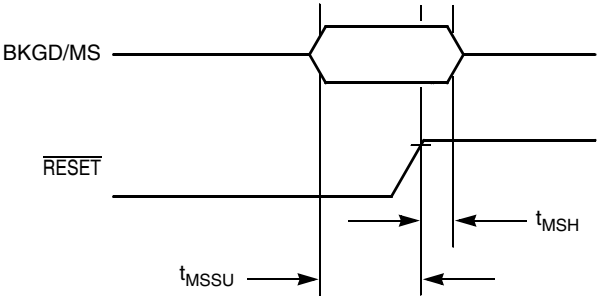


Figure 3-11. Active Background Debug Mode Latch Timing

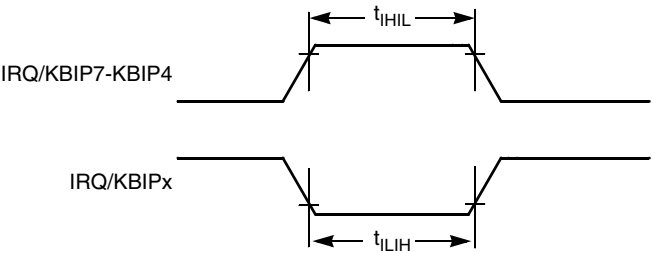


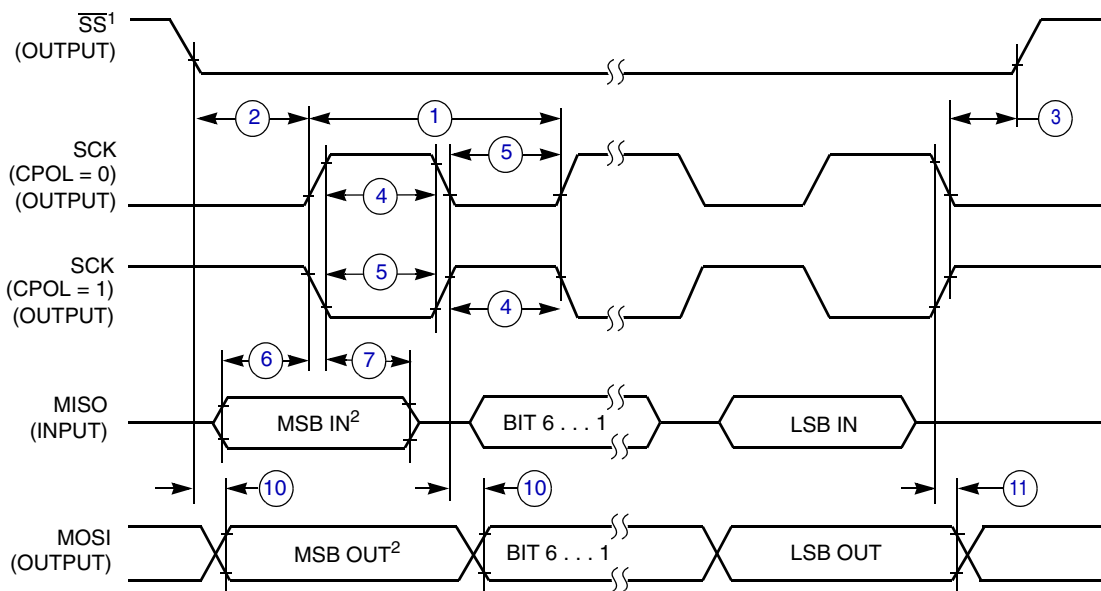
Figure 3-12. IRQ/KBIPx Timing

### 3.10.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 3-13. TPM Input Timing

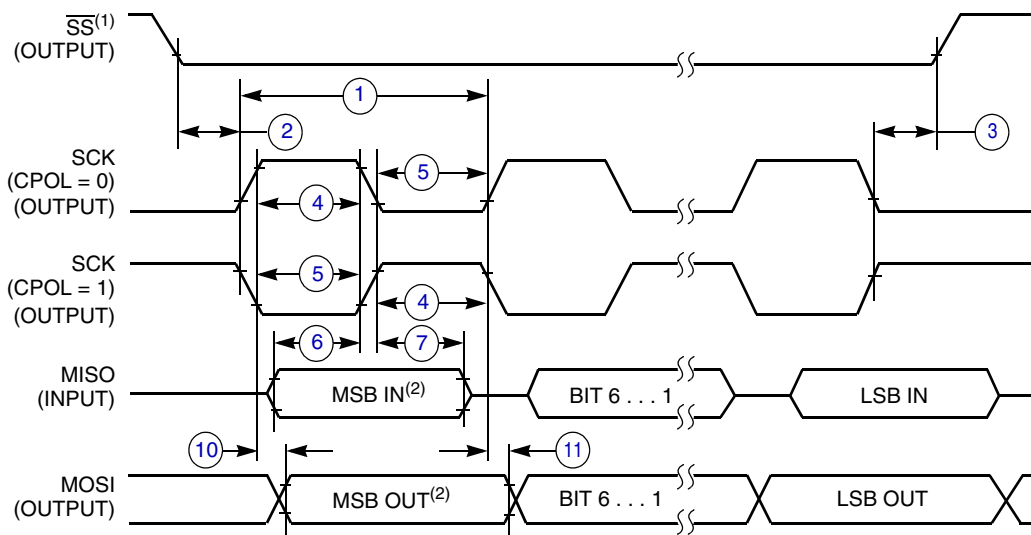
Function	Symbol	Min	Max	Unit
External clock frequency	$f_{TPMext}$	dc	$f_{Bus}/4$	MHz
External clock period	$t_{TPMext}$	4	—	$t_{cyc}$
External clock high time	$t_{clkh}$	1.5	—	$t_{cyc}$
External clock low time	$t_{clkl}$	1.5	—	$t_{cyc}$
Input capture pulse width	$t_{CPW}$	1.5	—	$t_{cyc}$



NOTES:

1.  $\overline{SS}$  output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 3-15. SPI Master Timing (CPHA = 0)**

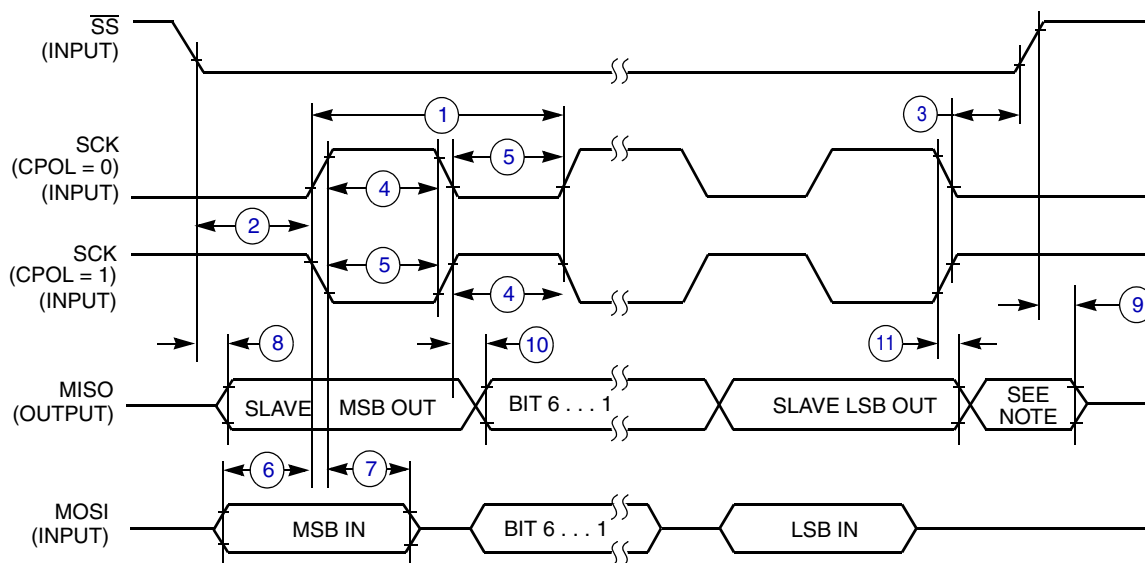


NOTES:

1.  $\overline{SS}$  output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 3-16. SPI Master Timing (CPHA = 1)**

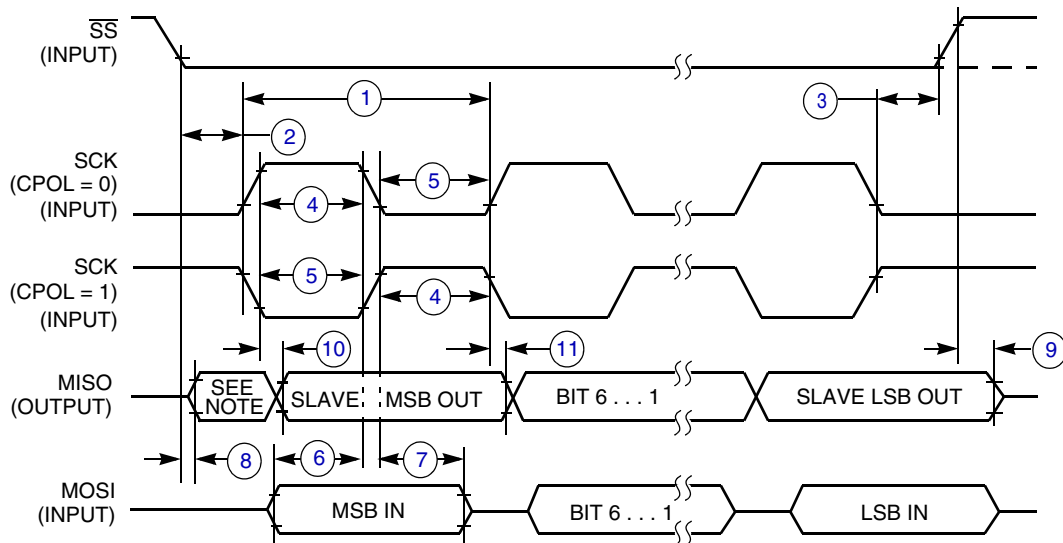




NOTE:

1. Not defined but normally MSB of character just received

**Figure 3-17. SPI Slave Timing (CPHA = 0)**



NOTE:

1. Not defined but normally LSB of character just received

**Figure 3-18. SPI Slave Timing (CPHA = 1)**

## 3.12 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal  $V_{DD}$  supply.

**Table 3-15. Flash Characteristics**

Num	C	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	P	Supply voltage for program/erase	$V_{\text{prog/erase}}$	2.7		5.5	V
2	P	Supply voltage for read operation	$V_{\text{Read}}$	2.7		5.5	V
3	P	Internal FCLK frequency <sup>2</sup>	$f_{\text{FCLK}}$	150		200	kHz
4	P	Internal FCLK period (1/FCLK)	$t_{\text{Fcyc}}$	5		6.67	$\mu\text{s}$
5	P	Byte program time (random location) <sup>(2)</sup>	$t_{\text{prog}}$	9			$t_{\text{Fcyc}}$
6	C	Byte program time (burst mode) <sup>(2)</sup>	$t_{\text{Burst}}$	4			$t_{\text{Fcyc}}$
7	P	Page erase time <sup>3</sup>	$t_{\text{Page}}$	4000			$t_{\text{Fcyc}}$
8	P	Mass erase time <sup>(2)</sup>	$t_{\text{Mass}}$	20,000			$t_{\text{Fcyc}}$
9	C	Program/erase endurance <sup>4</sup> $T_L$ to $T_H = -40^\circ\text{C}$ to $+125^\circ\text{C}$ $T = 25^\circ\text{C}$		10,000 —	— 100,000	— —	cycles
10	C	Data retention <sup>5</sup>	$t_{\text{D\_ret}}$	15	100	—	years

<sup>1</sup> Typical values are based on characterization data at  $V_{DD} = 5.0\text{ V}$ ,  $25^\circ\text{C}$  unless otherwise stated.

<sup>2</sup> The frequency of this clock is controlled by a software setting.

<sup>3</sup> These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

<sup>4</sup> **Typical endurance for Flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

<sup>5</sup> **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to  $25^\circ\text{C}$  using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory*.





