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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08ac96cfue

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

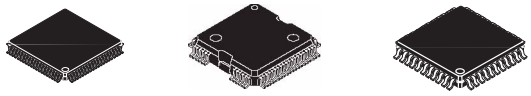
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08AC128
Rev. 4, 8/2011

MC9S08AC128 8-Bit Microcontroller Data Sheet

MC9S08AC128

917A-03 840B-01 824D-02



8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 20-MHz internal bus frequency
- HC08 instruction set with added BGND, CALL and RTC instructions
- Memory Management Unit to support paged memory.
- Linear Address Pointer to allow direct page data accesses of the entire memory map

Development Support

- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip in-circuit emulator (ICE) Debug module containing three comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Supports both tag and force breakpoints.

Memory Options

- Up to 128K FLASH — read/program/erase over full operating voltage and temperature
- Up to 8K Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and FLASH contents

Clock Source Options

- Clock source options include crystal, resonator, external clock, or internally generated clock with precision NVM trimming using ICG module

System Protection

- Optional computer operating properly (COP) reset with option to run from independent internal clock source or bus clock
- CRC module to support fast cyclic redundancy checks on system memory
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Master reset pin and power-on reset (POR)

Power-Saving Modes

- Wait plus two stops

Peripherals

- **ADC** — 16-channel, 10-bit resolution, 2.5 μs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel
- **SCIx** — Two serial communications interface modules supporting LIN 2.0 Protocol and SAE J2602 protocols; Full duplex non-return to zero (NRZ); Master extended break generation; Slave extended break detection; Wakeup on active edge
- **SPIx** — One full and one master-only serial peripheral interface modules; Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Inter-integrated circuit bus module; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- **TPMx** — One 2-channel and two 6-channel 16-bit timer/pulse-width modulator (TPM) modules: Selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels
- **KBI** — 8-pin keyboard interrupt module

Input/Output

- Up to 70 general-purpose input/output pins
- Software selectable pullups on input port pins
- Software selectable drive strength and slew rate control on ports when used as outputs

Package Options

- 80-pin low-profile quad flat package (LQFP)
- 64-pin quad flat package (QFP)
- 48-pin quad flat no-lead package (QFN)
- 44-pin low-profile quad flat package (LQFP)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

freescale™ semiconductor

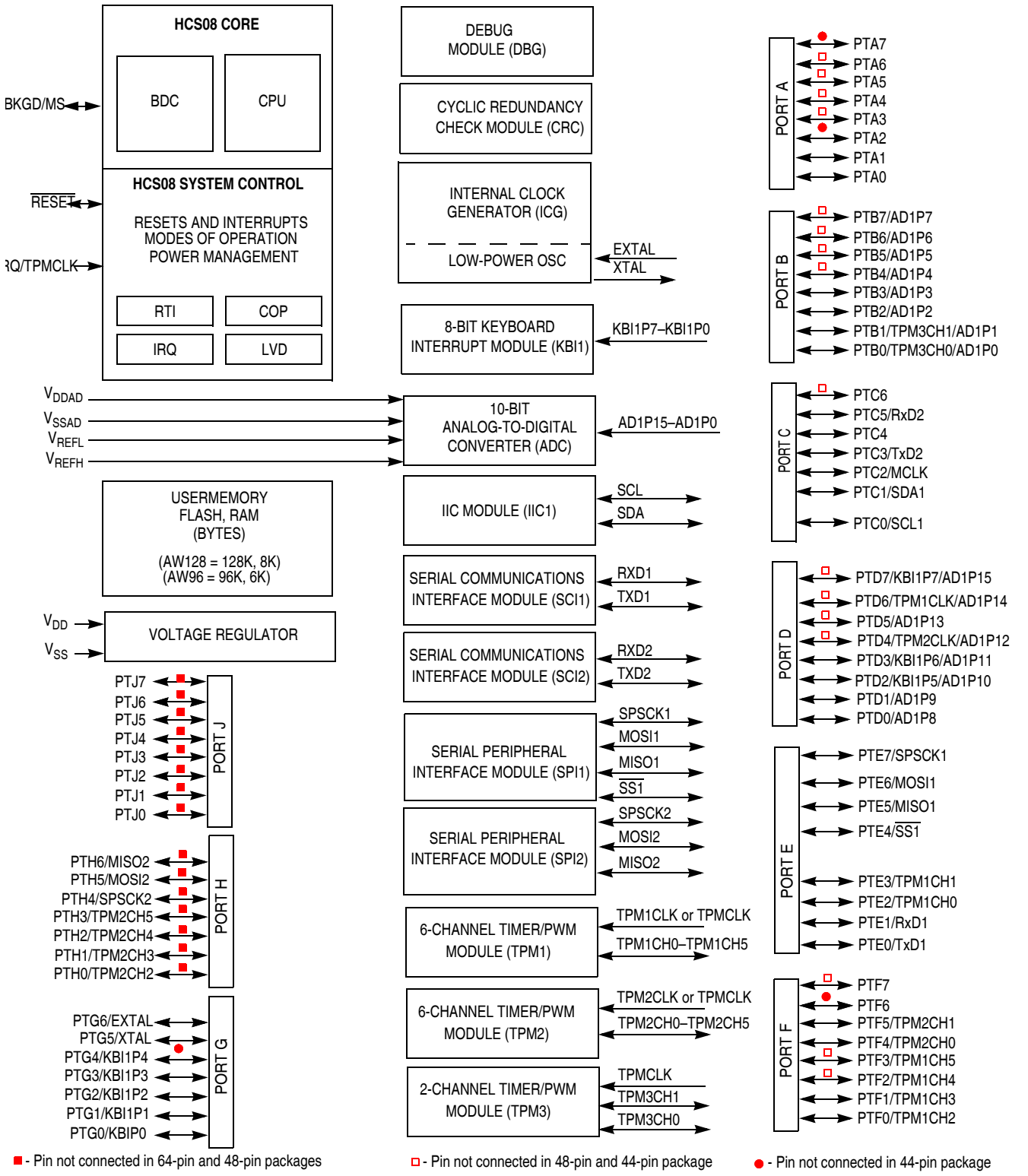
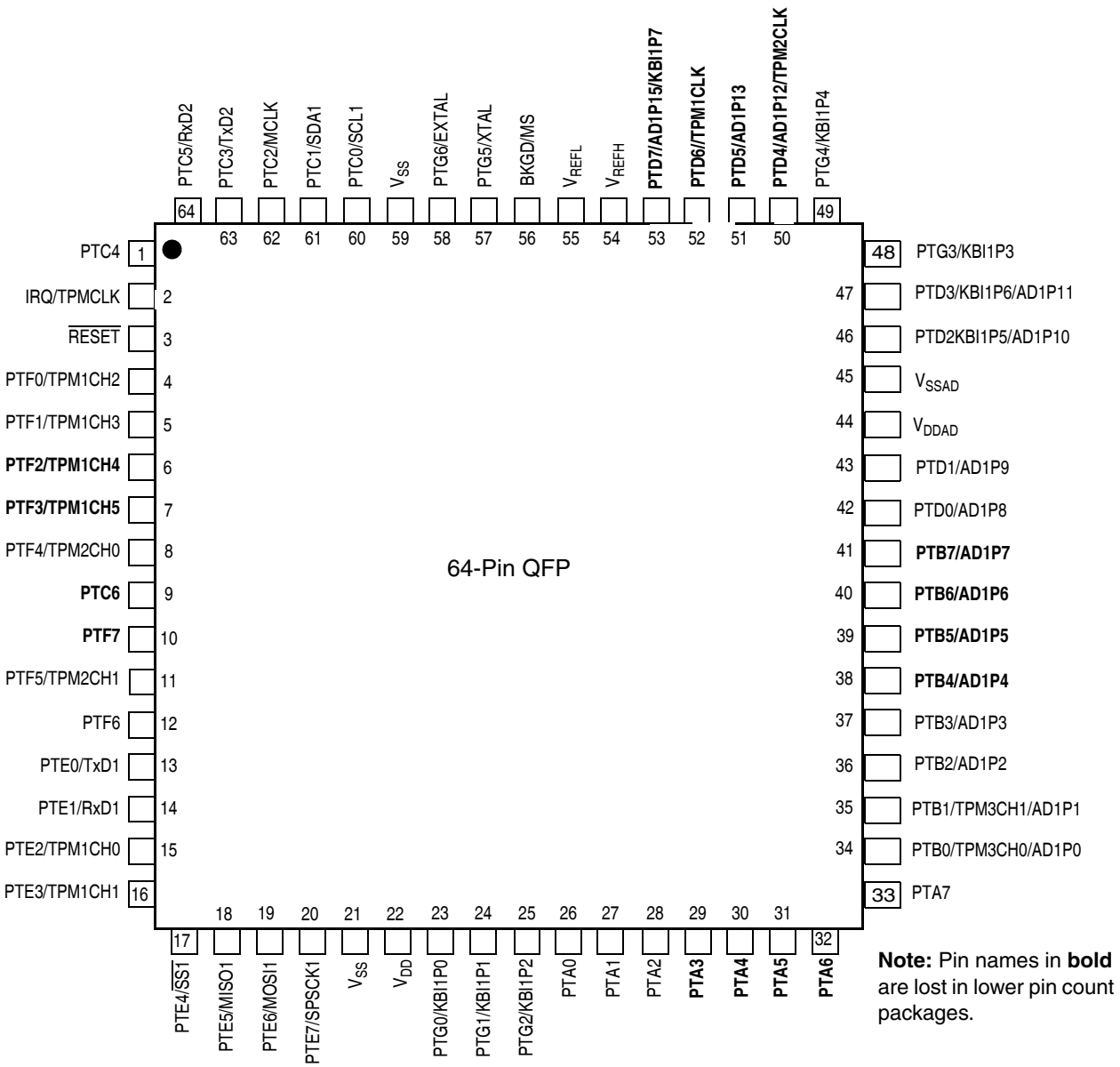


Figure 1-1. MC9S08AC128 Series Block Diagram

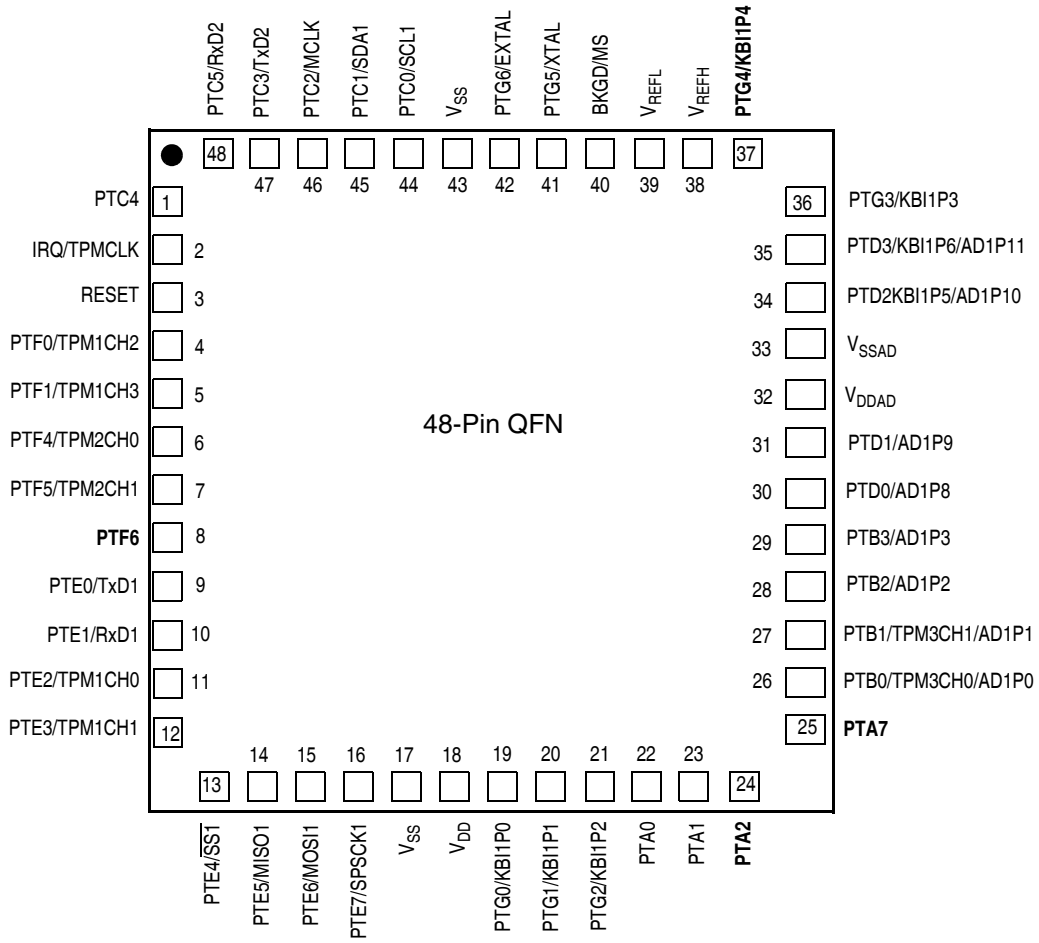
Figure 2-2 shows the 64-pin package assignments for the MC9S08AC128 Series devices.



Note: Pin names in **bold** are lost in lower pin count packages.

Figure 2-2. MC9S08AC128 Series in 64-Pin QFP Package

Figure 2-1 shows the 48-pin package assignments for the MC9S08AC128 Series devices.



Note: Pin names in **bold** are lost in lower pin count packages.

Figure 2-1. MC9S08AC128 Series in 48-Pin QFN Package

Figure 2-3 shows the 44-pin LQFP pin assignments for the MC9S08AC128 Series device.

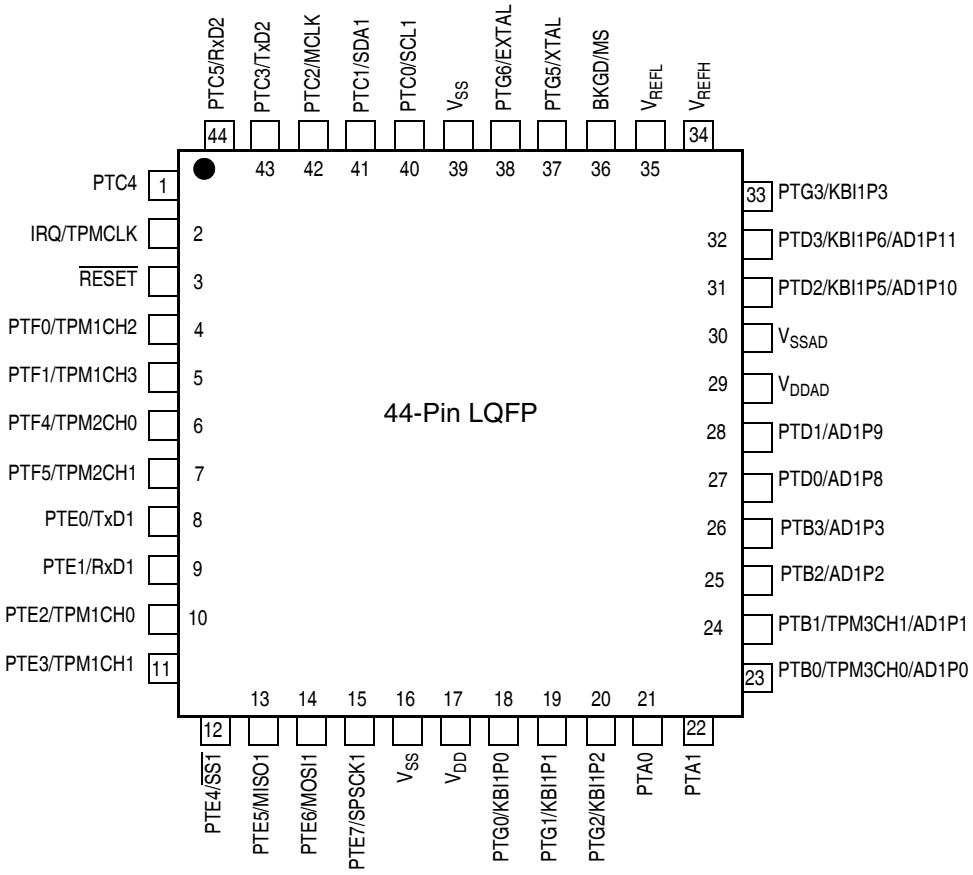


Figure 2-3. MC9S08AC128 Series in 44-Pin LQFP Package

Table 2-4. Pin Availability by Package Pin-Count

Pin Number				Lowest <-- Priority --> Highest		
80	64	48	44	Port Pin	Alt 1	Alt 2
1	1	1	1	PTC4		
2	2	2	2	IRQ	TPMCLK[1]	
3	3	3	3	$\overline{\text{RESET}}$		
4	4	4	4	PTF0	TPM1CH2	
5	5	5	5	PTF1	TPM1CH3	
6	6	—	—	PTF2	TPM1CH4	
7	7	—	—	PTF3	TPM1CH5	
8	8	6	6	PTF4	TPM2CH0	
9	9	—	—	PTC6		
10	10	—	—	PTF7		
11	11	7	7	PTF5	TPM2CH1	
12	12	8	—	PTF6		

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <-- Priority --> Highest		
80	**64**	**48**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
13	—	—	—	PTJ0		
14	—	—	—	PTJ1		
15	—	—	—	PTJ2		
16	—	—	—	PTJ3		
17	13	9	8	PTE0	TxD1	
18	14	10	9	PTE1	RxD1	
19	15	11	10	PTE2	TPM1CH0	
20	16	12	11	PTE3	TPM1CH1	
21	17	13	12	PTE4	$\overline{SS1}$	
22	18	14	13	PTE5	MISO1	
23	19	15	14	PTE6	MOSI1	
24	20	16	15	PTE7	SPSCK1	
25	21	17	16	V_{SS}		
26	22	18	17	V_{DD}		
27	—	—	—	PTJ4		
28	—	—	—	PTJ5		
29	—	—	—	PTJ6		
30	—	—	—	PTJ7		
31	23	19	18	PTG0	KBI1P0	
32	24	20	19	PTG1	KBI1P1	
33	25	21	20	PTG2	KBI1P2	
34	26	22	21	PTA0		
35	27	23	22	PTA1		
36	28	24	—	PTA2		
37	29	—	—	PTA3		
38	30	—	—	PTA4		
39	31	—	—	PTA5		
40	32	—	—	PTA6		
41	33	25	—	PTA7		
42	—	—	—	PTH0	TPM2CH2	
43	—	—	—	PTH1	TPM2CH3	
44	—	—	—	PTH2	TPM2CH4	
45	—	—	—	PTH3	TPM2CH5	
46	34	26	23	PTB0	TPM3CH0	AD1P0
47	35	27	24	PTB1	TPM3CH1	AD1P1
48	36	28	25	PTB2	AD1P2	
49	37	29	26	PTB3	AD1P3	
50	38	—	—	PTB4	AD1P4	
51	39	—	—	PTB5	AD1P5	
52	40	—	—	PTB6	AD1P6	
53	41	—	—	PTB7	AD1P7	

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <-- Priority --> Highest		
80	**64**	**48**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
54	42	30	27	PTD0	AD1P8	
55	43	31	28	PTD1	AD1P9	
56	44	32	29	V_{DDAD}		
57	45	33	30	V_{SSAD}		
58	46	34	31	PTD2	KBI1P5	AD1P10
59	47	35	32	PTD3	KBI1P6	AD1P11
60	48	36	33	PTG3	KBI1P3	
61	49	37	—	PTG4	KBI1P4	
62	50	—	—	PTD4	TPM2CLK	AD1P12
63	51	—	—	PTD5	AD1P13	
64	52	—	—	PTD6	TPM1CLK	AD1P14
65	53	—	—	PTD7	KBI1P7	AD1P15
66	54	38	34	V_{REFH}		
67	55	39	35	V_{REFL}		
68	56	40	36	BKGD	MS	
69	57	41	37	PTG5	XTAL	
70	58	42	38	PTG6	EXTAL	
71	59	43	39	V_{SS}		
72	—	—	—	V_{DD}(NC)		
73	60	44	40	PTC0	SCL1	
74	61	45	41	PTC1	SDA1	
75	—	—	—	PTH4	SPSCK2	
76	—	—	—	PTH5	MOSI2	
77	—	—	—	PTH6	MISO2	
78	62	46	42	PTC2	MCLK	
79	63	47	43	PTC3	TxD2	
80	64	48	44	PTC5	RxD2	

[1] TPMCLK, TPM1CLK, and TPM2CLK options are configured via software; out of reset, TPM1CLK, TPM2CLK, and TPMCLK are available to TPM1, TPM2, and TPM3 respectively.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 3-3. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H –40 to 125	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s		61	
	2s2p		47	
64-pin QFP				
	1s		57	
	2s2p	θ_{JA}	43	°C/W
48-pin QFN				
	1s		81	
	2s2p		28	
44-pin LQFP				
	1s		73	
	2s2p		56	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s - Single Layer Board, one signal layer

4 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

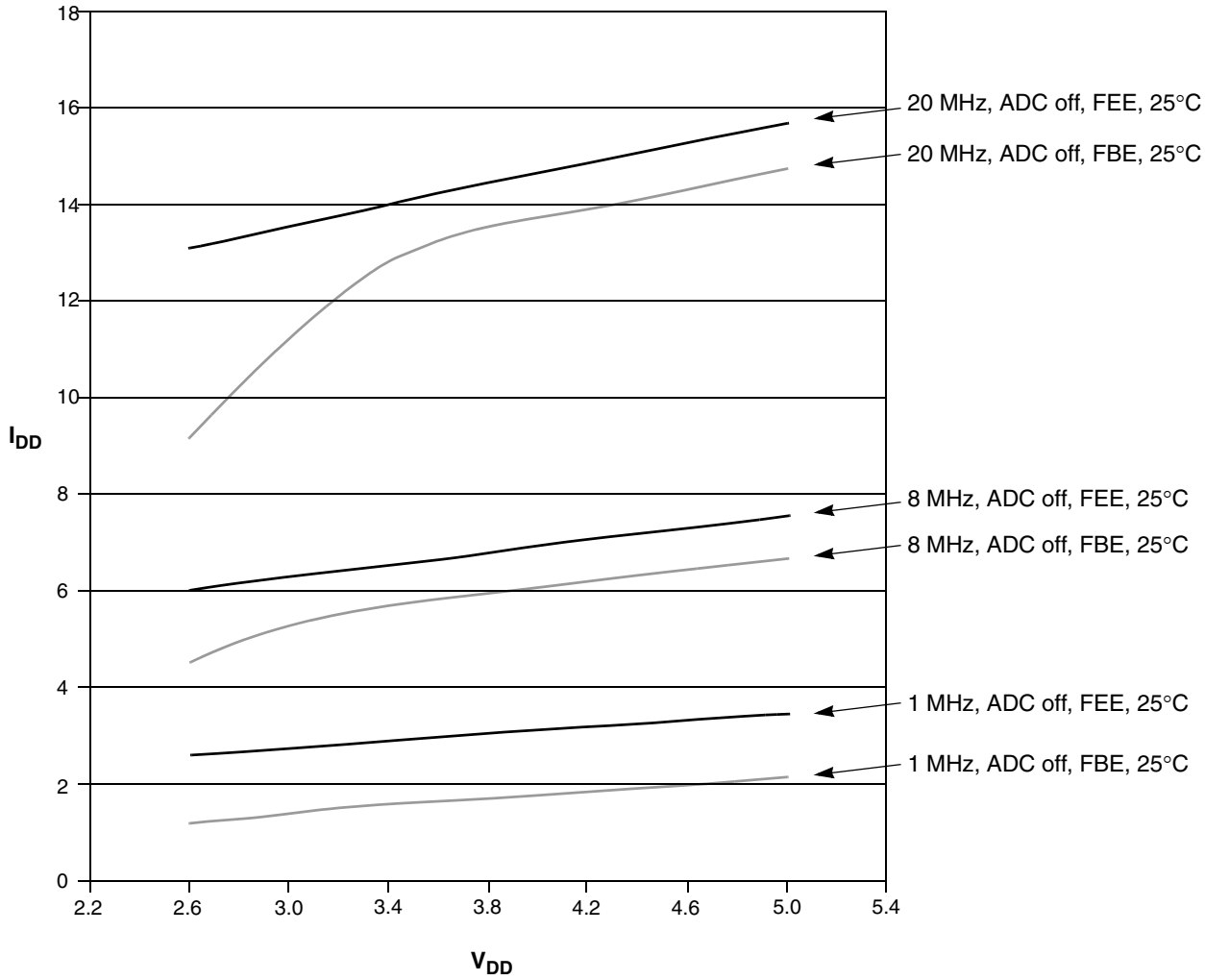
$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 3-1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 3-2}$$



Note: External clock is square wave supplied by function generator. For FEE mode, external reference frequency is 4 MHz

Figure 3-5. Typical Run I_{DD} for FBE and FEE Modes, I_{DD} vs. V_{DD}

3 Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.

4 Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

7 This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{ICGOUT}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDA} and V_{SSA} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

9 See Figure 3-9

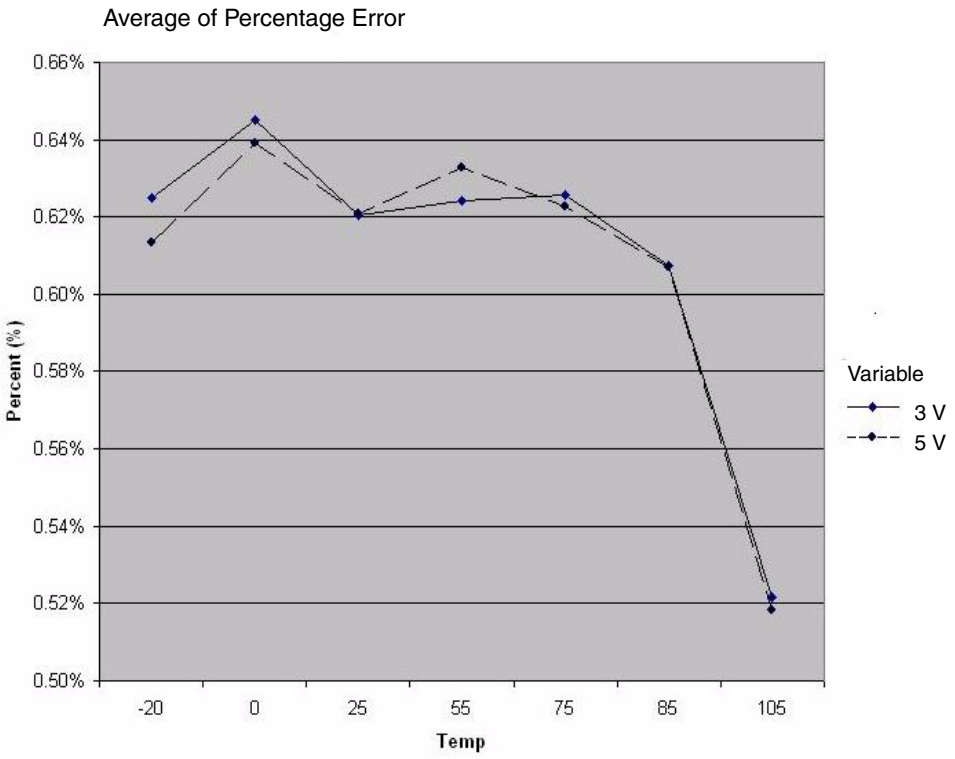


Figure 3-9. Internal Oscillator Deviation from Trimmed Frequency

3.10 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 3-12. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2		Real-time interrupt internal oscillator period	t_{RTI}	600		1500	µs
3		External reset pulse width[2] (t_{cyc} = 1/f_{Self_reset})	t_{extrst}	1.5 x t_{Self_reset}		—	ns
4		Reset low drive[3]	t_{rstdrv}	34 x t_{cyc}		—	ns
5		Active background debug mode latch setup time	t_{MSSU}	25		—	ns
6		Active background debug mode latch hold time	t_{MSH}	25		—	ns
7		IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8		KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9		Port rise and fall time (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 3 30	 	ns

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 When any reset is initiated, internal circuitry drives the reset pin low for about 34 bus cycles and then samples the level on the reset pin about 38 bus cycles later to distinguish external reset requests from internal requests.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 125°C.

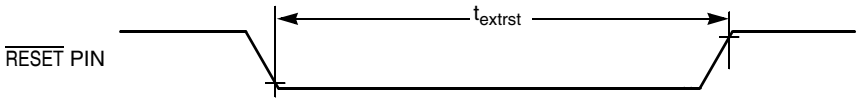


Figure 3-10. Reset Timing

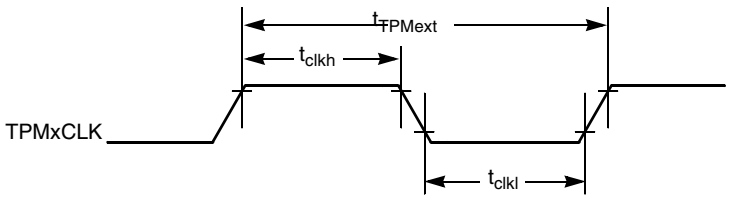


Figure 3-13. Timer External Clock

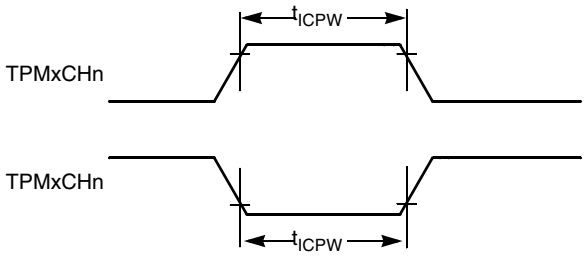


Figure 3-14. Timer Input Capture Pulse

3.11 SPI Characteristics

Table 3-14 and Figure 3-15 through Figure 3-18 describe the timing requirements for the SPI system.

Table 3-14. SPI Electrical Characteristic

Num[1]	C	Characteristic[2]	Symbol	Min	Max	Unit
		Operating frequency[3] Master Slave	 f_{op} f_{op}	 $f_{Bus}/2048$ dc	 $f_{Bus}/2$ $f_{Bus}/4$	Hz
1		Cycle time Master Slave	 t_{SCK} t_{SCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
2		Enable lead time Master Slave	 t_{Lead} t_{Lead}	 — 1/2	 1/2 —	 t_{SCK} t_{SCK}
3		Enable lag time Master Slave	 t_{Lag} t_{Lag}	 — 1/2	 1/2 —	 t_{SCK} t_{SCK}
4		Clock (SPSCK) high time Master and Slave	t_{SCKH}	1/2 t_{SCK} – 25	—	ns
5		Clock (SPSCK) low time Master and Slave	t_{SCKL}	1/2 t_{SCK} – 25	—	ns
6		Data setup time (inputs) Master Slave	 $t_{SI(M)}$ $t_{SI(S)}$	 30 30	 — —	 ns ns
7		Data hold time (inputs) Master Slave	 $t_{HI(M)}$ $t_{HI(S)}$	 30 30	 — —	 ns ns
8		Access time, slave[4]	t_A	0	40	ns
9		Disable time, slave[5]	t_{dis}	—	40	ns
10		Data setup time (outputs) Master Slave	 t_{SO} t_{SO}	 25 25	 — —	 ns ns
11		Data hold time (outputs) Master Slave	 t_{HO} t_{HO}	 –10 –10	 — —	 ns ns

1 Refer to Figure 3-15 through Figure 3-18.

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Maximum baud rate must be limited to 5 MHz due to pad input characteristics.

4 Time to data active from high-impedance state.

5 Hold time to high-impedance state.

3.12 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 3-15. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	P	Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2	P	Supply voltage for read operation	V_{Read}	2.7		5.5	V
3	P	Internal FCLK frequency[2]	f_{FCLK}	150		200	kHz
4	P	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
5	P	Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
6	C	Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to + 125°C T = 25°C		10,000 —	— 100,000	— —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25°C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 **Typical endurance for Flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

3.13 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 3-16. Radiated Emissions

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field and magnetic field	V_{RE_TEM}	V_{DD} = 5.0 V T_A = +25°C package type 80 LQFP	0.15 – 50 MHz	32kHz crystal 20MHz Bus	30	dBμV
			50 – 150 MHz		32	
			150 – 500 MHz		19	
			500 – 1000 MHz		7	
			IEC Level		I^2	—
			SAE Level		I^2	—

1 Data based on laboratory test results.

2 IEC and SAE Level Maximums: I=36 dBuV.

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