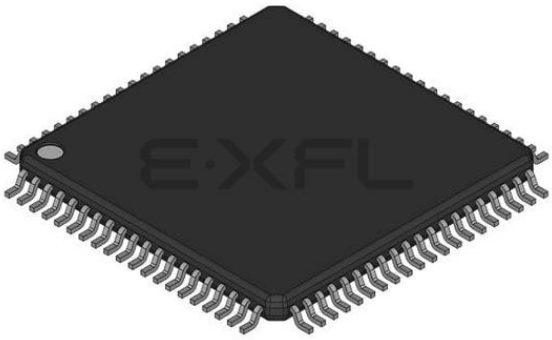

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08ac96clke

Table of Contents

Related Documentation

MC9S08AC128 Series Reference Manual (MC9S08AC128RM)
contains extensive product information including modes of operartion, memory, resets and interrupts, register definitions, port pins, CPU, and all peripheral module information.

For the latest version of the documentation, check our website at:
http://www.freescale.com

Figure 2-3 shows the 44-pin LQFP pin assignments for the MC9S08AC128 Series device.

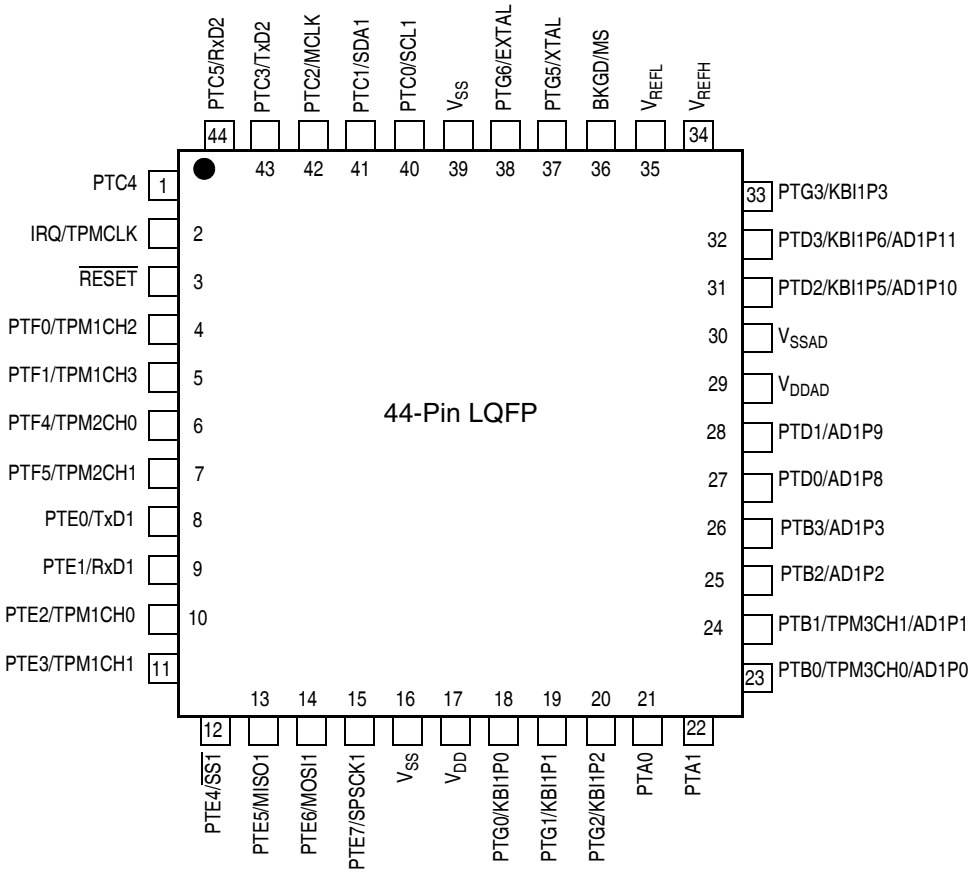


Figure 2-3. MC9S08AC128 Series in 44-Pin LQFP Package

Table 2-4. Pin Availability by Package Pin-Count

Pin Number				Lowest <-- Priority --> Highest		
80	64	48	44	Port Pin	Alt 1	Alt 2
1	1	1	1	PTC4		
2	2	2	2	IRQ	TPMCLK[1]	
3	3	3	3	$\overline{\text{RESET}}$		
4	4	4	4	PTF0	TPM1CH2	
5	5	5	5	PTF1	TPM1CH3	
6	6	—	—	PTF2	TPM1CH4	
7	7	—	—	PTF3	TPM1CH5	
8	8	6	6	PTF4	TPM2CH0	
9	9	—	—	PTC6		
10	10	—	—	PTF7		
11	11	7	7	PTF5	TPM2CH1	
12	12	8	—	PTF6		

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <-- Priority --> Highest		
80	**64**	**48**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
13	—	—	—	PTJ0		
14	—	—	—	PTJ1		
15	—	—	—	PTJ2		
16	—	—	—	PTJ3		
17	13	9	8	PTE0	TxD1	
18	14	10	9	PTE1	RxD1	
19	15	11	10	PTE2	TPM1CH0	
20	16	12	11	PTE3	TPM1CH1	
21	17	13	12	PTE4	$\overline{SS1}$	
22	18	14	13	PTE5	MISO1	
23	19	15	14	PTE6	MOSI1	
24	20	16	15	PTE7	SPSCK1	
25	21	17	16	V_{SS}		
26	22	18	17	V_{DD}		
27	—	—	—	PTJ4		
28	—	—	—	PTJ5		
29	—	—	—	PTJ6		
30	—	—	—	PTJ7		
31	23	19	18	PTG0	KBI1P0	
32	24	20	19	PTG1	KBI1P1	
33	25	21	20	PTG2	KBI1P2	
34	26	22	21	PTA0		
35	27	23	22	PTA1		
36	28	24	—	PTA2		
37	29	—	—	PTA3		
38	30	—	—	PTA4		
39	31	—	—	PTA5		
40	32	—	—	PTA6		
41	33	25	—	PTA7		
42	—	—	—	PTH0	TPM2CH2	
43	—	—	—	PTH1	TPM2CH3	
44	—	—	—	PTH2	TPM2CH4	
45	—	—	—	PTH3	TPM2CH5	
46	34	26	23	PTB0	TPM3CH0	AD1P0
47	35	27	24	PTB1	TPM3CH1	AD1P1
48	36	28	25	PTB2	AD1P2	
49	37	29	26	PTB3	AD1P3	
50	38	—	—	PTB4	AD1P4	
51	39	—	—	PTB5	AD1P5	
52	40	—	—	PTB6	AD1P6	
53	41	—	—	PTB7	AD1P7	

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <-- Priority --> Highest		
80	**64**	**48**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
54	42	30	27	PTD0	AD1P8	
55	43	31	28	PTD1	AD1P9	
56	44	32	29	V_{DDAD}		
57	45	33	30	V_{SSAD}		
58	46	34	31	PTD2	KBI1P5	AD1P10
59	47	35	32	PTD3	KBI1P6	AD1P11
60	48	36	33	PTG3	KBI1P3	
61	49	37	—	PTG4	KBI1P4	
62	50	—	—	PTD4	TPM2CLK	AD1P12
63	51	—	—	PTD5	AD1P13	
64	52	—	—	PTD6	TPM1CLK	AD1P14
65	53	—	—	PTD7	KBI1P7	AD1P15
66	54	38	34	V_{REFH}		
67	55	39	35	V_{REFL}		
68	56	40	36	BKGD	MS	
69	57	41	37	PTG5	XTAL	
70	58	42	38	PTG6	EXTAL	
71	59	43	39	V_{SS}		
72	—	—	—	V_{DD}(NC)		
73	60	44	40	PTC0	SCL1	
74	61	45	41	PTC1	SDA1	
75	—	—	—	PTH4	SPSCK2	
76	—	—	—	PTH5	MOSI2	
77	—	—	—	PTH6	MISO2	
78	62	46	42	PTC2	MCLK	
79	63	47	43	PTC3	TxD2	
80	64	48	44	PTC5	RxD2	

[1] TPMCLK, TPM1CLK, and TPM2CLK options are configured via software; out of reset, TPM1CLK, TPM2CLK, and TPMCLK are available to TPM1, TPM2, and TPM3 respectively.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 3-3. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H –40 to 125	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s		61	
	2s2p		47	
64-pin QFP				
	1s		57	
	2s2p	θ_{JA}	43	°C/W
48-pin QFN				
	1s		81	
	2s2p		28	
44-pin LQFP				
	1s		73	
	2s2p		56	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s - Single Layer Board, one signal layer

4 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 3-1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 3-2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3-3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits and JEDEC Standard for Non-Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3-4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		– 2.5	V
	Maximum input voltage limit		7.5	V

Table 3-5. ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	± 2000	–	V
2	C	Machine Model (MM)	V_{MM}	± 200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	± 500	–	V
4	C	Latch-up Current at T_A = 125°C	I_{LAT}	± 100	–	mA

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

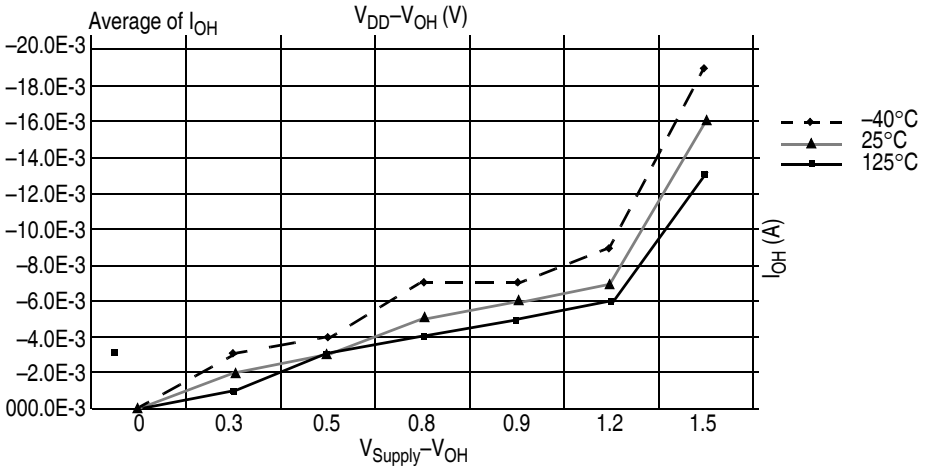


Figure 3-2. Typical I_{OH} (High Drive) vs $V_{DD}–V_{OH}$ at V_{DD} = 3 V

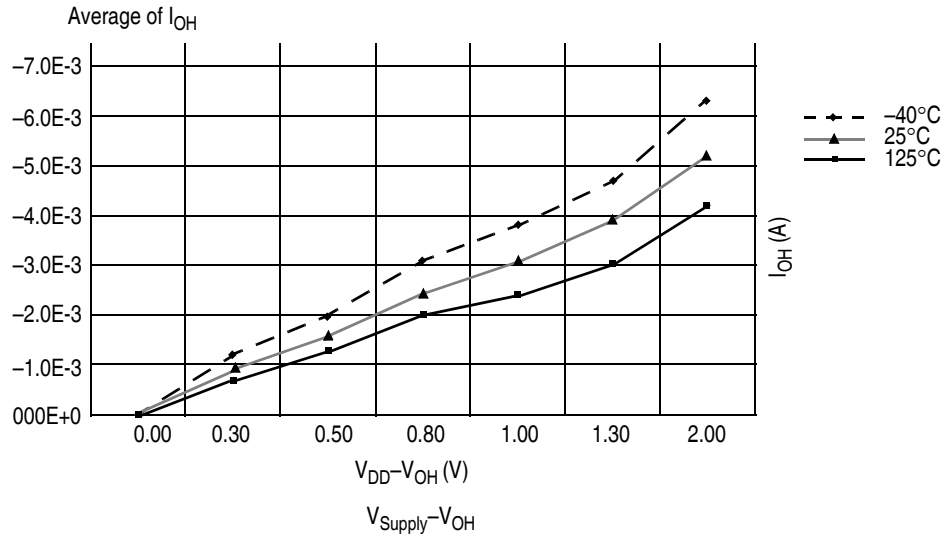


Figure 3-3. Typical I_{OH} (Low Drive) vs $V_{DD}–V_{OH}$ at V_{DD} = 5 V

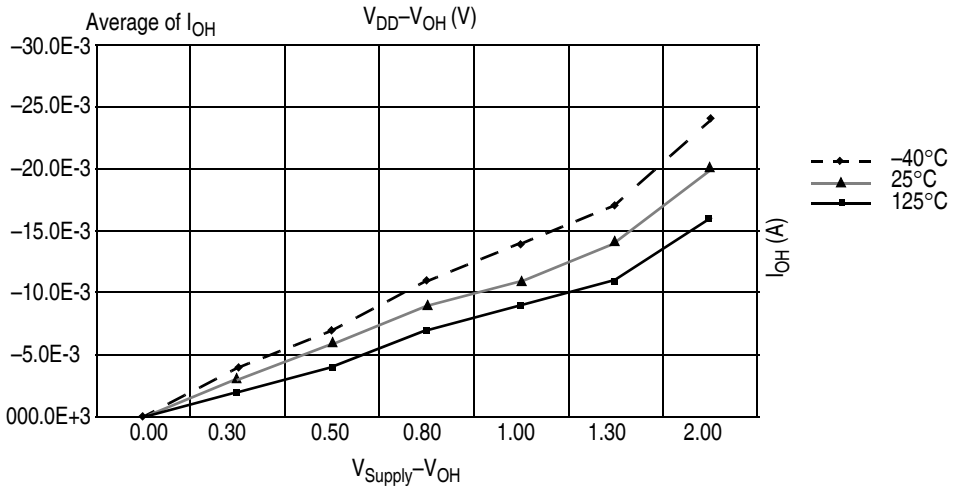


Figure 3-4. Typical I_{OH} (High Drive) vs $V_{DD}–V_{OH}$ at V_{DD} = 5 V

3.7 Supply Current Characteristics

Table 3-7. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	C	Run supply current[2] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	RI_{DD}	5	1.1	1.4[3]	mA	–40 to 125°C
				3	1.0	1.2		
2	C	Run supply current[4] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)	RI_{DD}	5	6.7	8.0[5]	mA	–40 to 125°C
				3	6	7.5		
3	C	Stop2 mode supply current	$S2I_{DD}$	5	1.0	25 160	µA	–40 to 85°C –40 to 125°C
				3	0.8	23 150	µA	–40 to 85°C –40 to 125°C
4	C	Stop3 mode supply current	$S3I_{DD}$	5	1.2	27 180[3]	µA	–40 to 85°C –40 to 125°C
				3	1.0	25 170	µA	–40 to 85°C –40 to 125°C
5	C	RTI adder to stop2 or stop3[6]	$S23I_{DDRTI}$	5	300	500 500	nA	–40 to 85°C –40 to 125°C
				3	300	500 500	nA	–40 to 85°C –40 to 125°C
6	C	LVD adder to stop3 (LVDE = LVDSE = 1)	$S3I_{DDLVD}$	5	110	180 180	µA	–40 to 85°C –40 to 125°C
				3	90	160 160	µA	–40 to 85°C –40 to 125°C
7	C	Adder to stop3 for oscillator enabled[7] (OSCSTEN =1)	$S3I_{DDOSC}$	5,3	5	8 8	µA µA	–40 to 85°C –40 to 125°C

1 Typical values are based on characterization data at 25°C unless otherwise stated. See Figure 3-5 through Figure 3-7 for typical curves across voltage/temperature.

2 All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

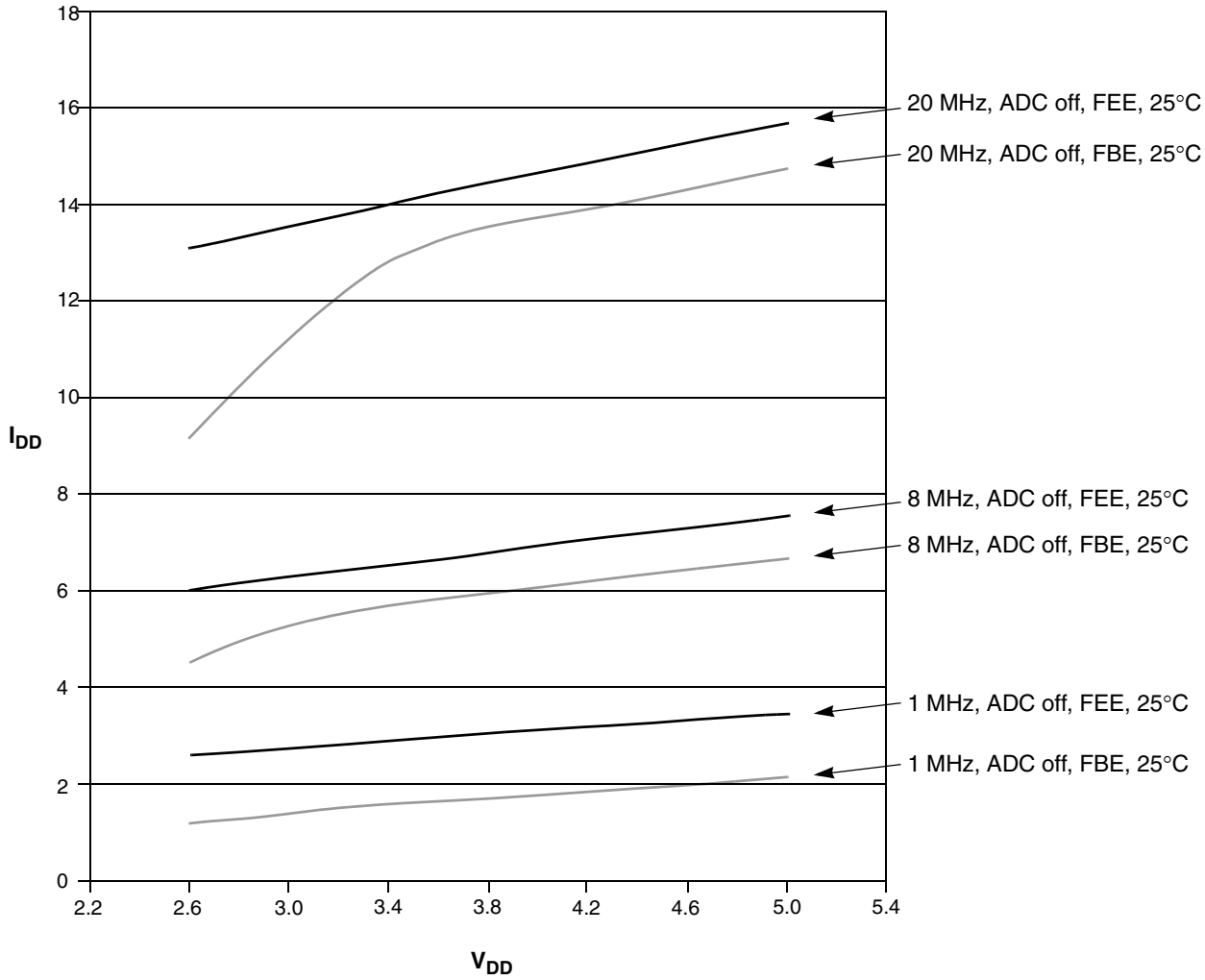
3 Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

4 All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

5 Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

6 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 560 µA at 3 V with f_{Bus} = 1 MHz.

7 Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal, low power mode (HGO = 0), clock monitor disabled (LOCD = 1).



Note: External clock is square wave supplied by function generator. For FEE mode, external reference frequency is 4 MHz

Figure 3-5. Typical Run I_{DD} for FBE and FEE Modes, I_{DD} vs. V_{DD}

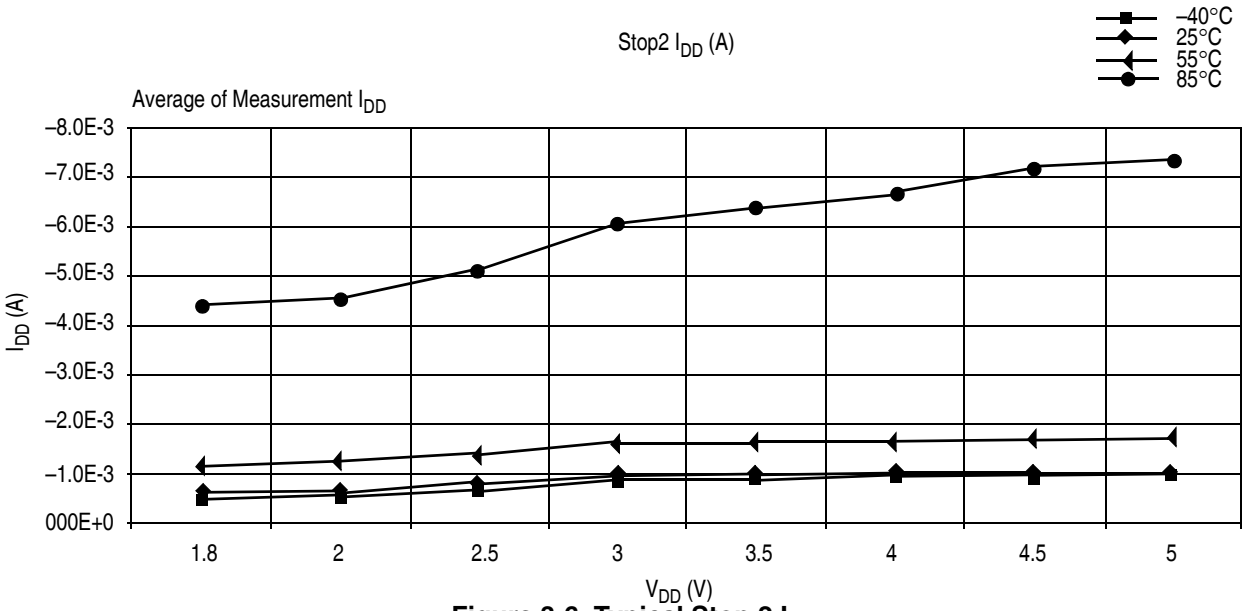


Figure 3-6. Typical Stop 2 I_{DD}

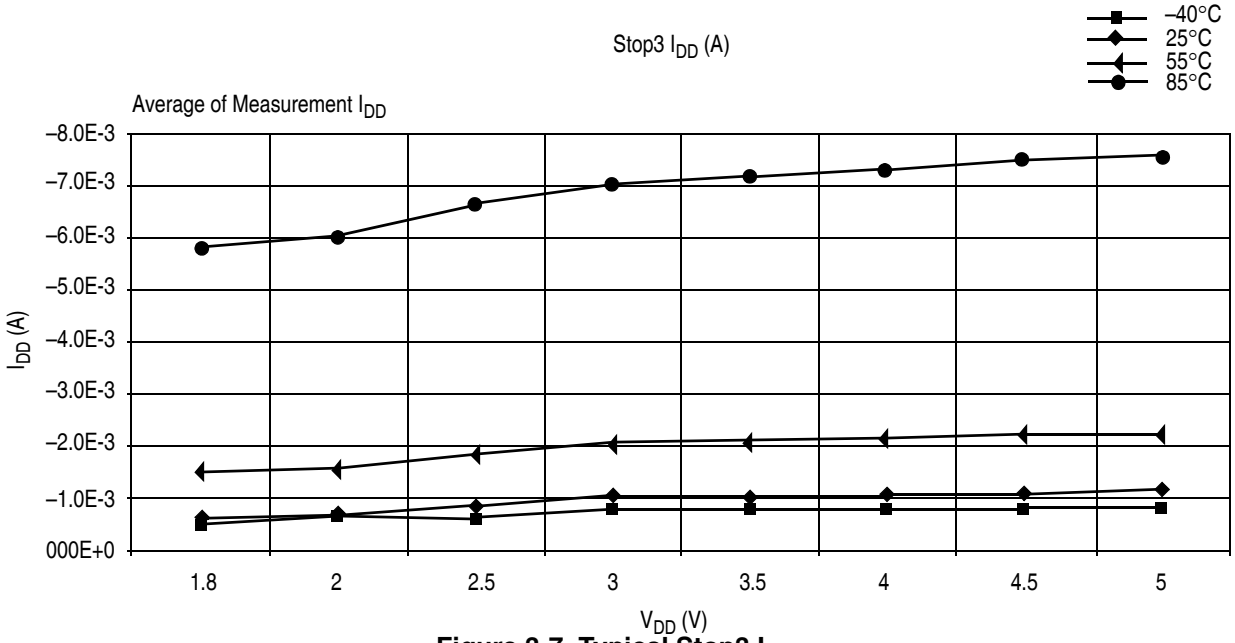


Figure 3-7. Typical Stop3 I_{DD}

3.8 ADC Characteristics

Table 3-8. 5 Volt 10-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V
	Delta to V_{DD} (V_{DD}–V_{DDAD})[2]	ΔV_{DDAD}	–100	0	+100	mV
Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSAD})[2]	ΔV_{SSAD}	–100	0	+100	mV
Ref voltage high		V_{REFH}	2.7	V_{DDAD}	V_{DDAD}	V
Ref voltage low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V
Supply current	Stop, reset, module off	I_{DDAD}	—	0.011	1	μA
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input capacitance		C_{ADIN}	—	4.5	5.5	pF
Input resistance		R_{ADIN}	—	3	5	kΩ
Analog source resistance External to MCU	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ
	8-bit mode (all valid f_{ADCK})		—	—	10	
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz
	Low power (ADLPC = 1)		0.4	—	4.0	
Temp Sensor Slope	–40°C to 25°C	m	—	3.266	—	mV/°C
	25°C to 125°C			3.638	—	
Temp Sensor Voltage	25°C	V_{TEMP25}	—	1.396	—	V

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 dc potential difference.

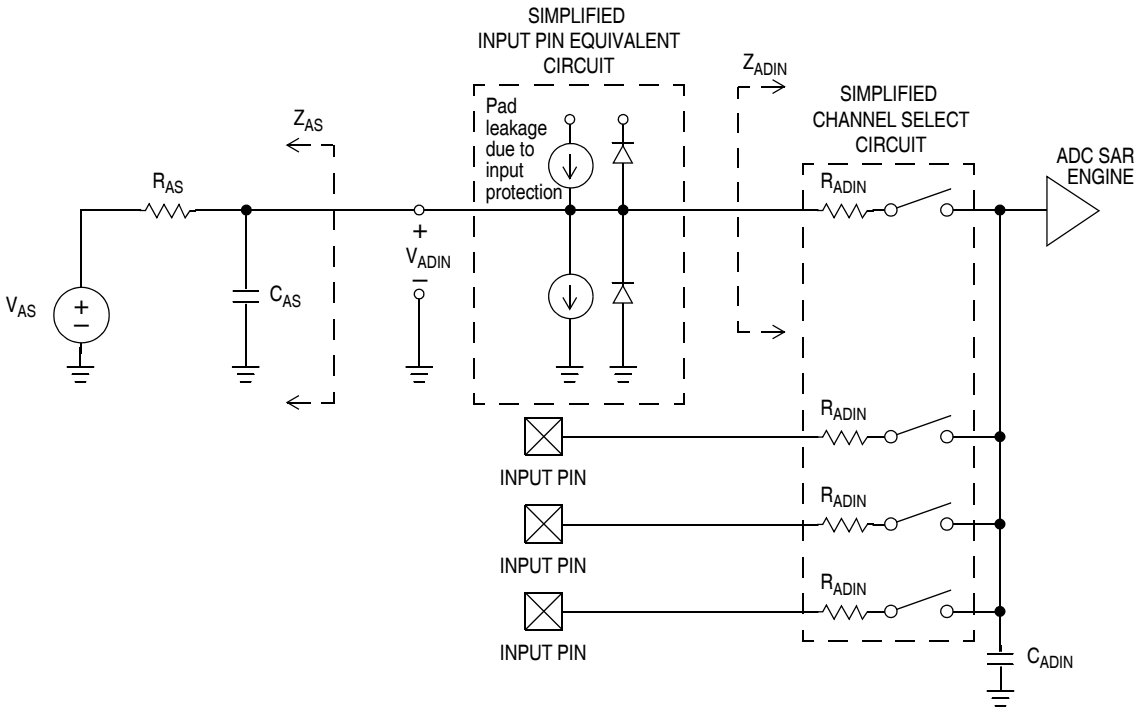


Figure 3-8. ADC Input Impedance Equivalency Diagram

Table 3-9. 5 Volt 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDAD}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDAD}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	—	μA
	$V_{DDAD} \leq 5.5$ V	P		—	—	1	mA
ADC asynchronous clock source $t_{ADACK} = 1/f_{ADACK}$	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (Including sample time)	Short sample (ADLSMP = 0)	P	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	P	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted error Includes quantization	10-bit mode	P	E_{TUE}	—	±1	±2.5	LSB[2]
	8-bit mode			—	±0.5	±1.0	
Differential non-linearity	10-bit mode	P	DNL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
	Monotonicity and no-missing-codes guaranteed						
Integral non-linearity	10-bit mode	C	INL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
Zero-scale error $V_{ADIN} = V_{SSA}$	10-bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Full-scale error $V_{ADIN} = V_{DDA}$	10-bit mode	P	E_{FS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Quantization error	10-bit mode	D	E_Q	—	—	±0.5	LSB[2]
	8-bit mode			—	—	±0.5	

3 Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.

4 Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

7 This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{ICGOUT}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDA} and V_{SSA} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

9 See Figure 3-9

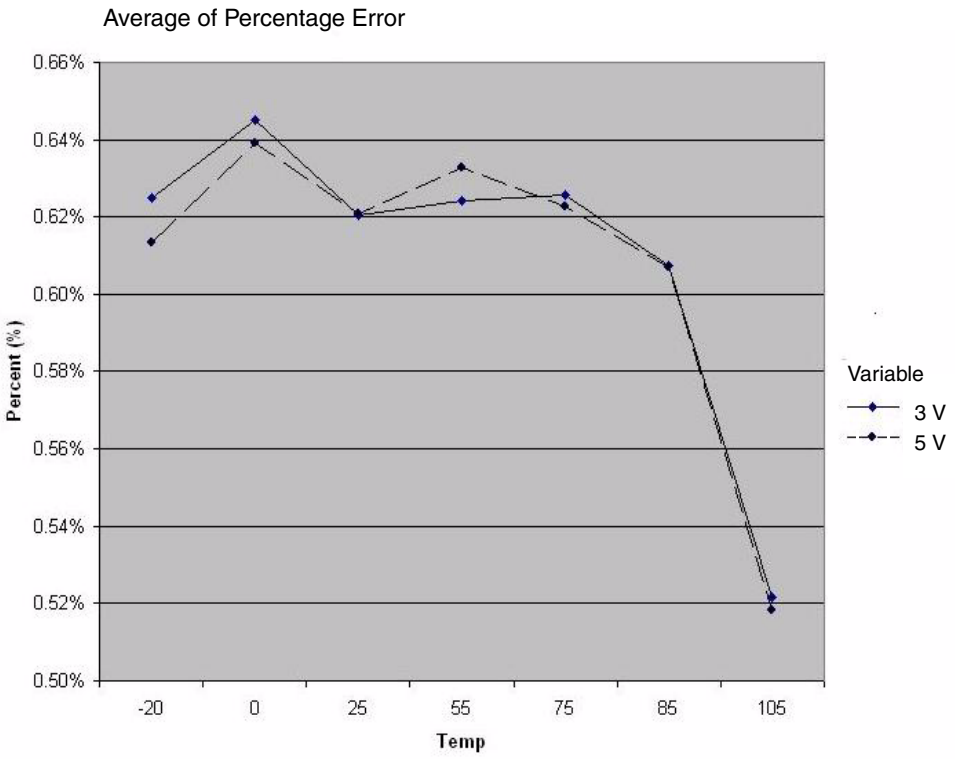


Figure 3-9. Internal Oscillator Deviation from Trimmed Frequency

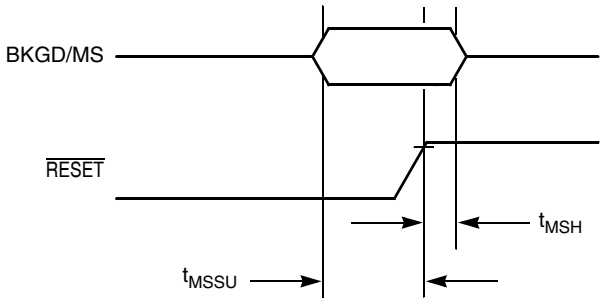


Figure 3-11. Active Background Debug Mode Latch Timing

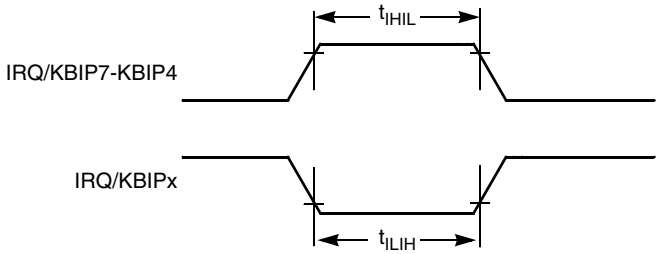


Figure 3-12. IRQ/KBIPx Timing

3.10.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 3-13. TPM Input Timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
External clock period	t_{TPMext}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

3.12 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 3-15. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	P	Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2	P	Supply voltage for read operation	V_{Read}	2.7		5.5	V
3	P	Internal FCLK frequency[2]	f_{FCLK}	150		200	kHz
4	P	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
5	P	Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
6	C	Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to + 125°C T = 25°C		10,000 —	— 100,000	— —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25°C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 **Typical endurance for Flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

Chapter 4
Ordering Information and Mechanical Drawings

4.1 Ordering Information

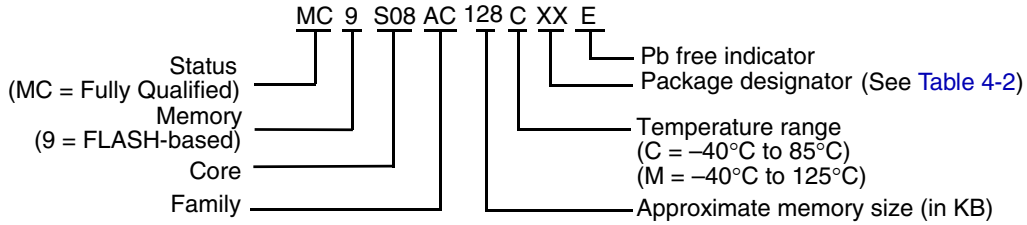
This section contains ordering numbers for MC9S08AC128 Series devices. See below for an example of the device numbering system.

Table 4-1. Device Numbering System

Device Number	Memory		Available Packages[1]
	FLASH	RAM	Type
MC9S08AC128	128K	8K	80 LQFP, 64 QFP, 48-QFN, 44-LQFP
MC9S08AC96	96K	6K	80 LQFP, 64 QFP, 48-QFN, 44-LQFP

1 See Table 4-2 for package information.

4.2 Orderable Part Numbering System



4.3 Mechanical Drawings

Table 4-2 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08AC128 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 4-2, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 4-2) in the "Enter Keyword" search box at the top of the page.

Table 4-2. Package Information

Pin Count	Type	Designator	Document No.
80	LQFP	LK	98ASS23237W
64	QFP	FU	98ASB42844B
48	QFN	FT	98ARH99048A
44	LQFP	FG	98ASS23225W

Chapter 5
Revision History

To provide the most up-to-date information, the version of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	9/2008	Initial release of a separate data sheet and reference manual. Removed PTH7, clarified SPI as one full and one master-only, added missing RoHS logo, updated back cover addresses, and incorporated general release edits and updates. Added some finalized electrical characteristics.
2	6/2009	Added the parameter “Bandgap Voltage Reference” in Table 3-6 Updated Section 3.13, “EMC Performance” and corrected Table 3-16. Updated disclaimer page.
3	9/2010	Added 48-pin QFN package information.
4	8/2011	Updated the t_{RTI} in the Table 3-12. Updated the RI_{DD} in the Table 3-7.