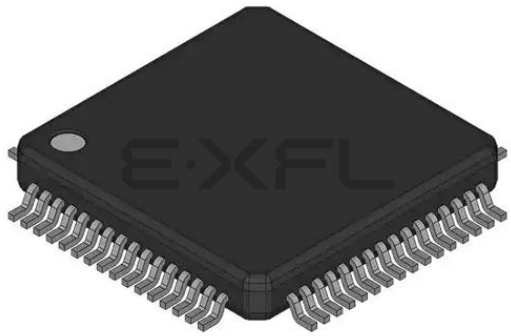

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08ac96mfue

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Table of Contents

Related Documentation

MC9S08AC128 Series Reference Manual (MC9S08AC128RM)
contains extensive product information including modes of operartion, memory, resets and interrupts, register definitions, port pins, CPU, and all peripheral module information.

For the latest version of the documentation, check our website at:
http://www.freescale.com

Chapter 2
Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

2.1 Device Pin Assignment

Figure 2-1 shows the 80-pin LQFP package pin assignments for the MC9S08AC128 Series device.

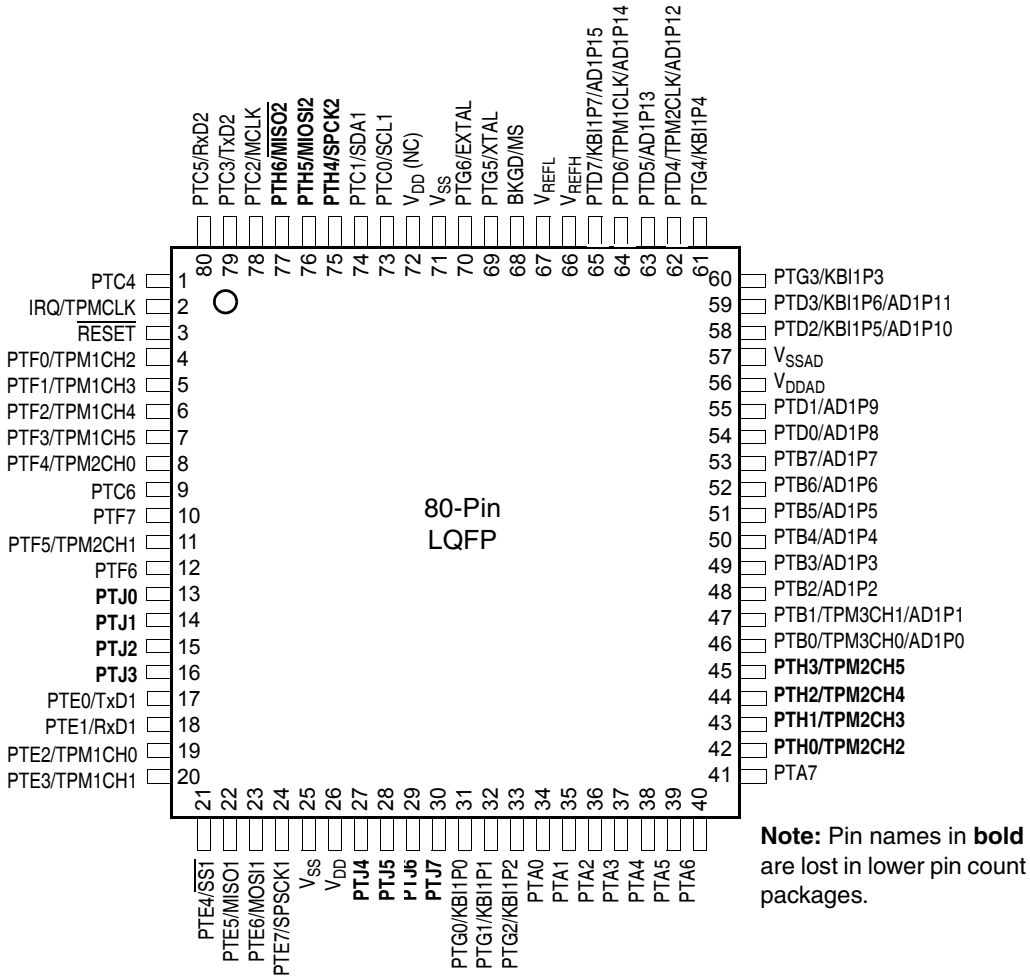


Figure 2-1. MC9S08AC128 Series in 80-Pin LQFP Package

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <-- Priority --> Highest		
80	**64**	**48**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
54	42	30	27	PTD0	AD1P8	
55	43	31	28	PTD1	AD1P9	
56	44	32	29	V_{DDAD}		
57	45	33	30	V_{SSAD}		
58	46	34	31	PTD2	KBI1P5	AD1P10
59	47	35	32	PTD3	KBI1P6	AD1P11
60	48	36	33	PTG3	KBI1P3	
61	49	37	—	PTG4	KBI1P4	
62	50	—	—	PTD4	TPM2CLK	AD1P12
63	51	—	—	PTD5	AD1P13	
64	52	—	—	PTD6	TPM1CLK	AD1P14
65	53	—	—	PTD7	KBI1P7	AD1P15
66	54	38	34	V_{REFH}		
67	55	39	35	V_{REFL}		
68	56	40	36	BKGD	MS	
69	57	41	37	PTG5	XTAL	
70	58	42	38	PTG6	EXTAL	
71	59	43	39	V_{SS}		
72	—	—	—	V_{DD}(NC)		
73	60	44	40	PTC0	SCL1	
74	61	45	41	PTC1	SDA1	
75	—	—	—	PTH4	SPSCK2	
76	—	—	—	PTH5	MOSI2	
77	—	—	—	PTH6	MISO2	
78	62	46	42	PTC2	MCLK	
79	63	47	43	PTC3	TxD2	
80	64	48	44	PTC5	RxD2	

[1] TPMCLK, TPM1CLK, and TPM2CLK options are configured via software; out of reset, TPM1CLK, TPM2CLK, and TPMCLK are available to TPM1, TPM2, and TPM3 respectively.

Chapter 3
Electrical Characteristics and Timing Specifications

3.1 Introduction

This section contains electrical and timing specifications.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3-1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3-2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 3-3. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H –40 to 125	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s		61	
	2s2p		47	
64-pin QFP				
	1s		57	
	2s2p	θ_{JA}	43	°C/W
48-pin QFN				
	1s		81	
	2s2p		28	
44-pin LQFP				
	1s		73	
	2s2p		56	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s - Single Layer Board, one signal layer

4 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 3-1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 3-2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3-3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits and JEDEC Standard for Non-Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3-4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		– 2.5	V
	Maximum input voltage limit		7.5	V

Table 3-5. ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	± 2000	–	V
2	C	Machine Model (MM)	V_{MM}	± 200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	± 500	–	V
4	C	Latch-up Current at T_A = 125°C	I_{LAT}	± 100	–	mA

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 3-6. DC Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	—	Operating Voltage	V_{DD}	2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA 5 V, I_{Load} = –0.4 mA 3 V, I_{Load} = –0.24 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
	P	Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA 5 V, I_{Load} = 0.4 mA 3 V, I_{Load} = 0.24 mA	V_{OL}	 — — — —	 — — — —	 1.5 1.5 0.8 0.8	V
	P	Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.4 mA		 — — — —	 — — — —	 1.5 1.5 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5V 3V	I_{OLT}	 — —	 — —	 100 60	mA
6	P	Input high voltage; all digital inputs 2.7v ≤ V_{DD} 4.5v	V_{IH}	0.70xV_{DD}	—	—	V
		4.5v ≤ V_{DD} ≤ 5.5v	V_{IH}	0.65xV_{DD}	—	—	
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 x V_{DD}	
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}			mV
9	P	Input leakage current; input only pins[2]	$\|I_{In}\|$	—	0.1	1	µA
10	P	High Impedance (off-state) leakage current[2]	$\|I_{OZ}\|$	—	0.1	1	µA
11	P	Internal pullup resistors[3]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V
15	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
16	D	POR rearm time	t_{POR}	10	—	—	µs
17	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVDH}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
18	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVDL}	 2.48 2.54	 2.56 2.62	 2.64 2.7	V

3.7 Supply Current Characteristics

Table 3-7. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	C	Run supply current[2] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	RI_{DD}	5	1.1	1.4[3]	mA	–40 to 125°C
				3	1.0	1.2		
2	C	Run supply current[4] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)	RI_{DD}	5	6.7	8.0[5]	mA	–40 to 125°C
				3	6	7.5		
3	C	Stop2 mode supply current	$S2I_{DD}$	5	1.0	25 160	µA	–40 to 85°C –40 to 125°C
				3	0.8	23 150	µA	–40 to 85°C –40 to 125°C
4	C	Stop3 mode supply current	$S3I_{DD}$	5	1.2	27 180[3]	µA	–40 to 85°C –40 to 125°C
				3	1.0	25 170	µA	–40 to 85°C –40 to 125°C
5	C	RTI adder to stop2 or stop3[6]	$S23I_{DDRTI}$	5	300	500 500	nA	–40 to 85°C –40 to 125°C
				3	300	500 500	nA	–40 to 85°C –40 to 125°C
6	C	LVD adder to stop3 (LVDE = LVDSE = 1)	$S3I_{DDLVD}$	5	110	180 180	µA	–40 to 85°C –40 to 125°C
				3	90	160 160	µA	–40 to 85°C –40 to 125°C
7	C	Adder to stop3 for oscillator enabled[7] (OSCSTEN =1)	$S3I_{DDOSC}$	5,3	5	8 8	µA µA	–40 to 85°C –40 to 125°C

1 Typical values are based on characterization data at 25°C unless otherwise stated. See Figure 3-5 through Figure 3-7 for typical curves across voltage/temperature.

2 All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

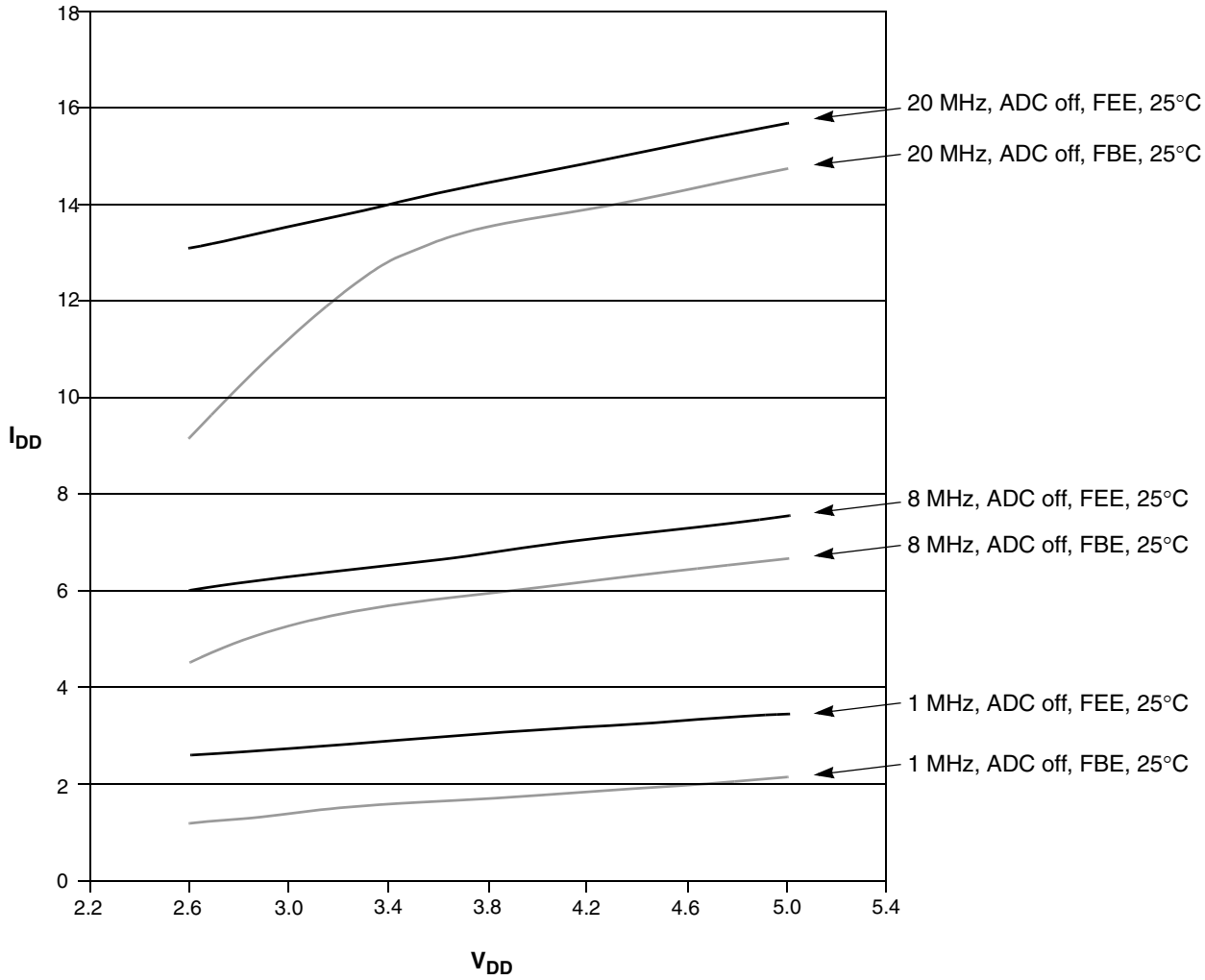
3 Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

4 All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

5 Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

6 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 560 µA at 3 V with f_{Bus} = 1 MHz.

7 Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal, low power mode (HGO = 0), clock monitor disabled (LOCD = 1).



Note: External clock is square wave supplied by function generator. For FEE mode, external reference frequency is 4 MHz

Figure 3-5. Typical Run I_{DD} for FBE and FEE Modes, I_{DD} vs. V_{DD}

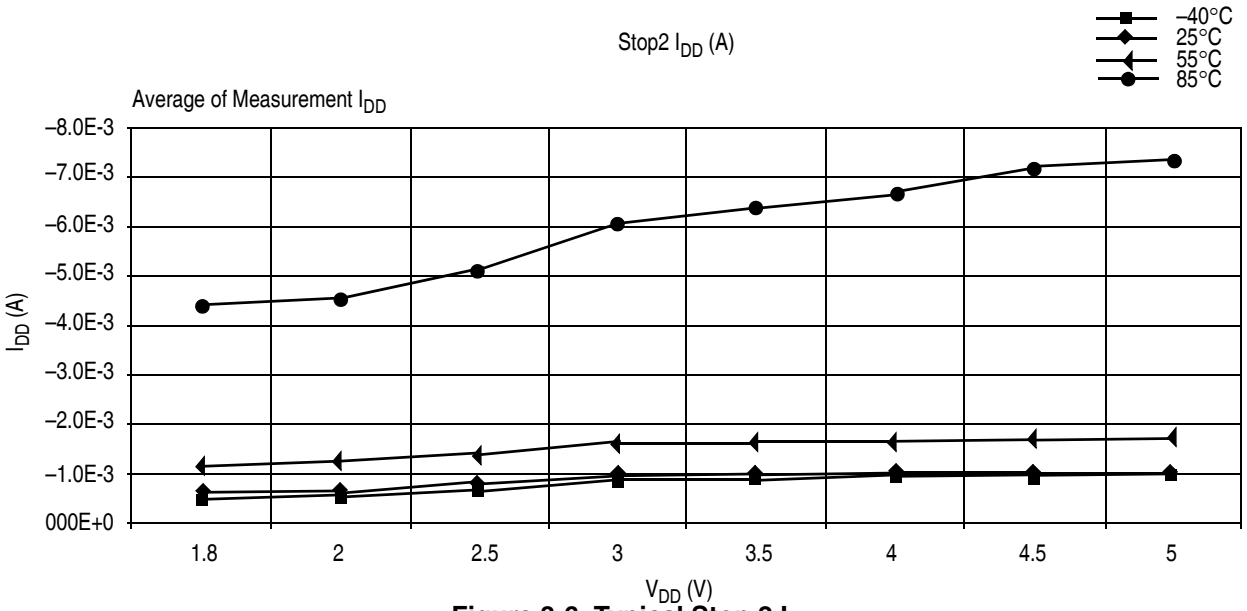


Figure 3-6. Typical Stop 2 I_{DD}

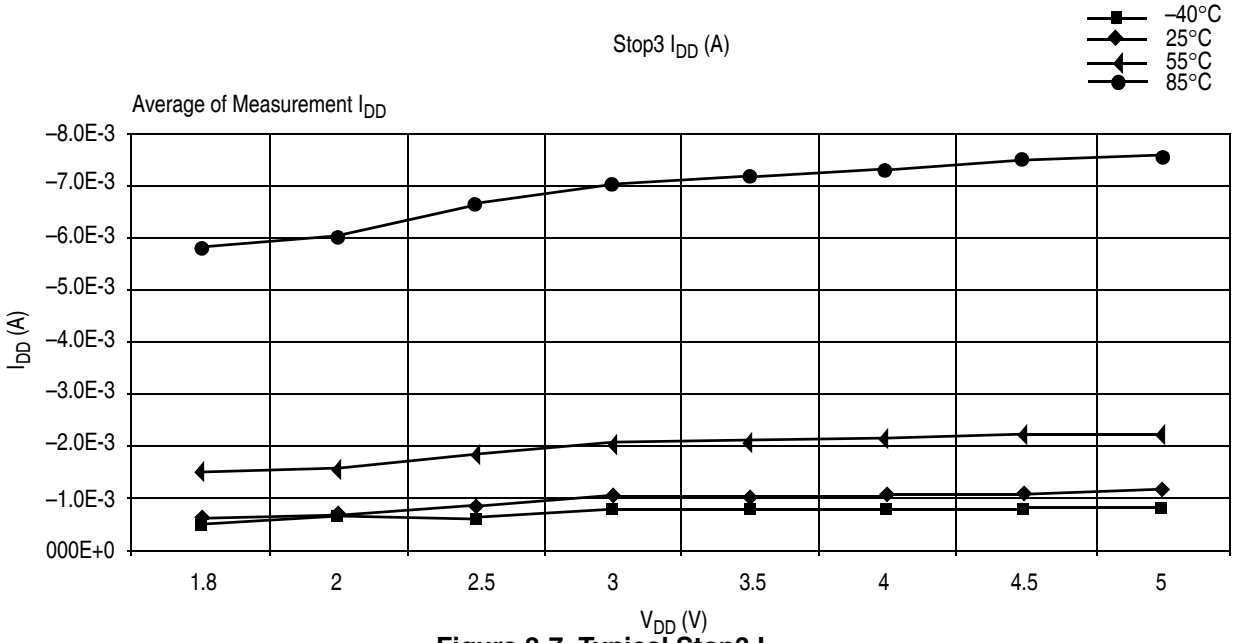


Figure 3-7. Typical Stop3 I_{DD}

3.8 ADC Characteristics

Table 3-8. 5 Volt 10-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V
	Delta to V_{DD} (V_{DD}–V_{DDAD})[2]	ΔV_{DDAD}	–100	0	+100	mV
Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSAD})[2]	ΔV_{SSAD}	–100	0	+100	mV
Ref voltage high		V_{REFH}	2.7	V_{DDAD}	V_{DDAD}	V
Ref voltage low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V
Supply current	Stop, reset, module off	I_{DDAD}	—	0.011	1	μA
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input capacitance		C_{ADIN}	—	4.5	5.5	pF
Input resistance		R_{ADIN}	—	3	5	kΩ
Analog source resistance External to MCU	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ
	8-bit mode (all valid f_{ADCK})		—	—	10	
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz
	Low power (ADLPC = 1)		0.4	—	4.0	
Temp Sensor Slope	–40°C to 25°C	m	—	3.266	—	mV/°C
	25°C to 125°C			3.638	—	
Temp Sensor Voltage	25°C	V_{TEMP25}	—	1.396	—	V

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 dc potential difference.

Table 3-9. 5 Volt 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDAD}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDAD}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	—	μA
	$V_{DDAD} \leq 5.5$ V	P		—	—	1	mA
ADC asynchronous clock source $t_{ADACK} = 1/f_{ADACK}$	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (Including sample time)	Short sample (ADLSMP = 0)	P	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	P	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted error Includes quantization	10-bit mode	P	E_{TUE}	—	±1	±2.5	LSB[2]
	8-bit mode			—	±0.5	±1.0	
Differential non-linearity	10-bit mode	P	DNL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
	Monotonicity and no-missing-codes guaranteed						
Integral non-linearity	10-bit mode	C	INL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
Zero-scale error $V_{ADIN} = V_{SSA}$	10-bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Full-scale error $V_{ADIN} = V_{DDA}$	10-bit mode	P	E_{FS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Quantization error	10-bit mode	D	E_Q	—	—	±0.5	LSB[2]
	8-bit mode			—	—	±0.5	

Table 3-9. 5 Volt 10-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Input leakage error Pad leakage[3] * R_{AS}	10-bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[2]
	8-bit mode			—	±0.1	±1	

1 Typical values assume V_{DDAD} = 5.0V, Temp = 25C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electricals.

3.9 Internal Clock Generation Module Characteristics

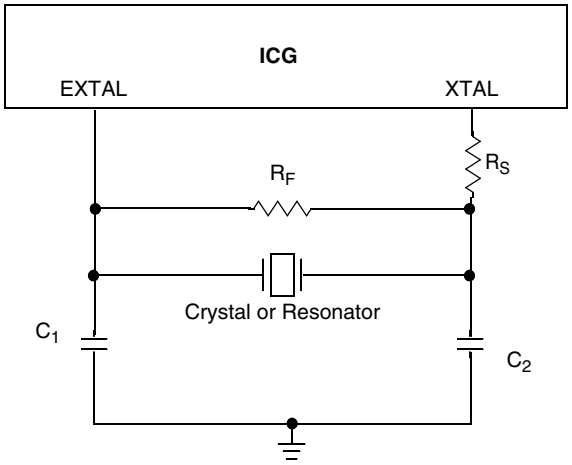


Table 3-10. ICG DC Electrical Specifications (Temperature Range = –40 to 125°C Ambient)

Characteristic	Symbol	Min	Typ[1]	Max	Unit
Load capacitors	C_1 C_2	See Note [2]			
Feedback resistor Low range (32k to 100 kHz) High range (1M – 16 MHz)	R_F		10 1		MΩ MΩ
Series resistor Low range Low Gain (HGO = 0) High Gain (HGO = 1) High range Low Gain (HGO = 0) High Gain (HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 10 20	 — — — — — —	 kΩ

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C or is typical recommended value.

2 See crystal or resonator manufacturer's recommendation.

3 Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.

4 Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

7 This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{ICGOUT}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDA} and V_{SSA} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

9 See Figure 3-9

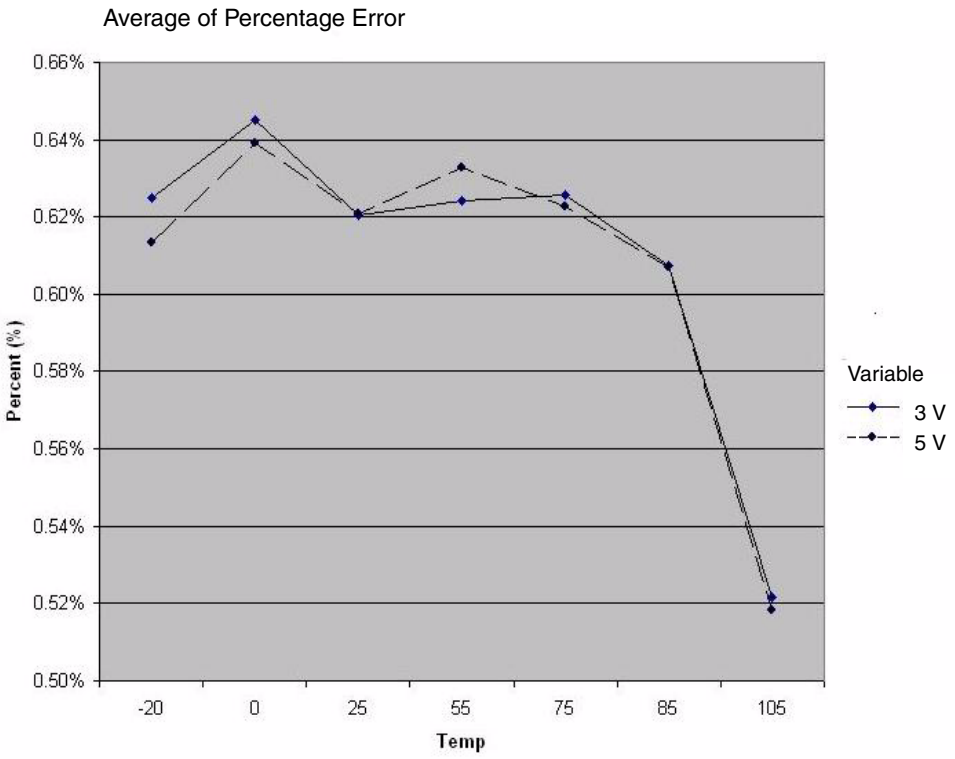


Figure 3-9. Internal Oscillator Deviation from Trimmed Frequency

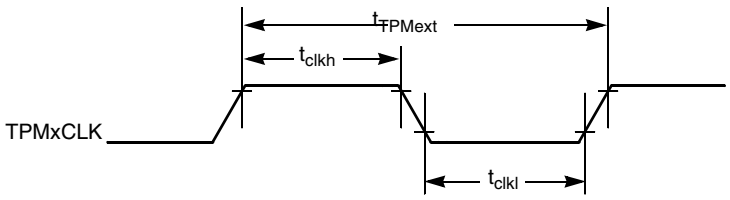


Figure 3-13. Timer External Clock

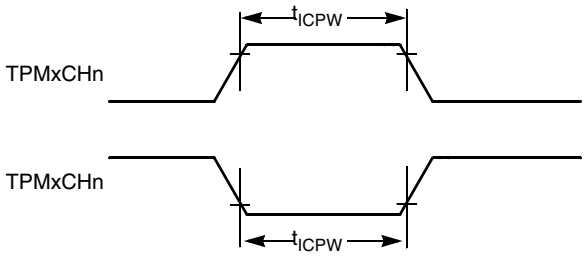
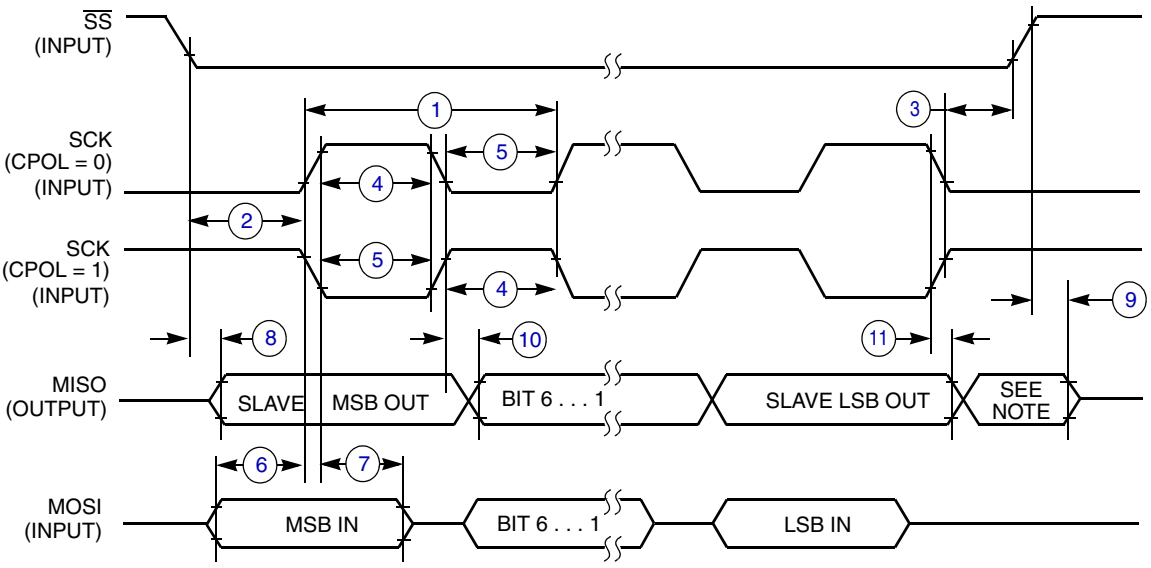
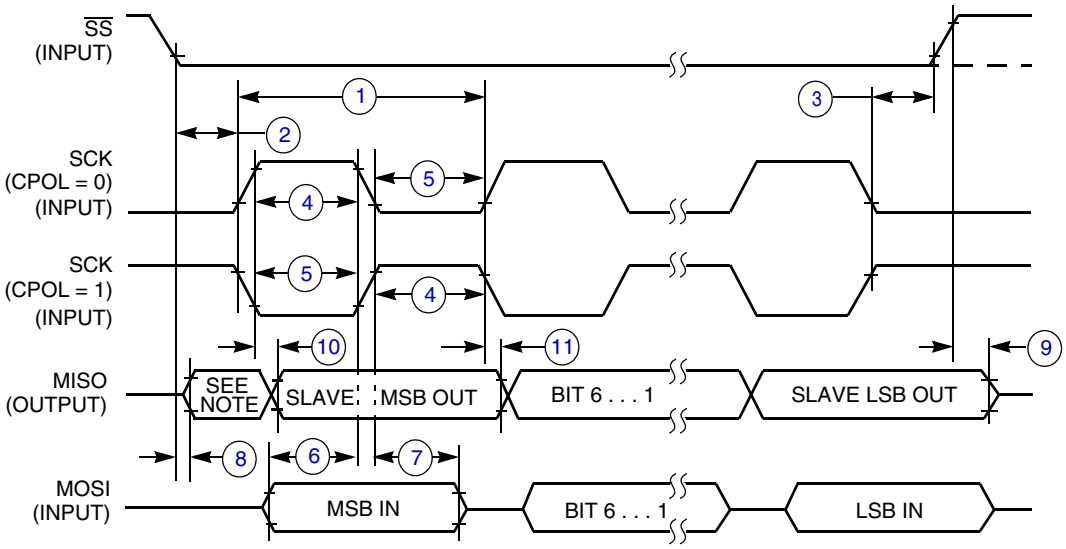


Figure 3-14. Timer Input Capture Pulse



NOTE:
1. Not defined but normally MSB of character just received

Figure 3-17. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 3-18. SPI Slave Timing (CPHA = 1)

3.13 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 3-16. Radiated Emissions

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field and magnetic field	V_{RE_TEM}	V_{DD} = 5.0 V T_A = +25°C package type 80 LQFP	0.15 – 50 MHz	32kHz crystal 20MHz Bus	30	dBμV
			50 – 150 MHz		32	
			150 – 500 MHz		19	
			500 – 1000 MHz		7	
			IEC Level		I^2	—
			SAE Level		I^2	—

1 Data based on laboratory test results.

2 IEC and SAE Level Maximums: I=36 dBuV.

Chapter 4
Ordering Information and Mechanical Drawings

4.1 Ordering Information

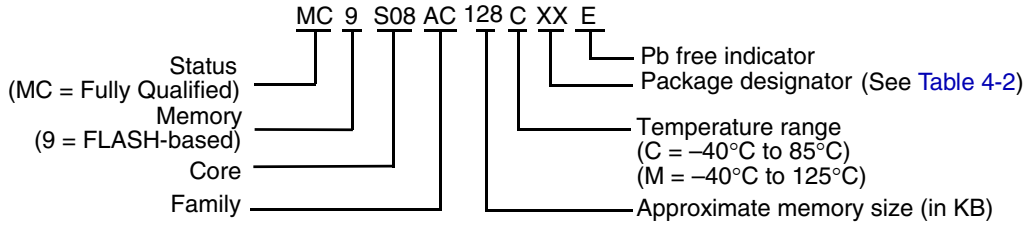
This section contains ordering numbers for MC9S08AC128 Series devices. See below for an example of the device numbering system.

Table 4-1. Device Numbering System

Device Number	Memory		Available Packages[1]
	FLASH	RAM	Type
MC9S08AC128	128K	8K	80 LQFP, 64 QFP, 48-QFN, 44-LQFP
MC9S08AC96	96K	6K	80 LQFP, 64 QFP, 48-QFN, 44-LQFP

1 See Table 4-2 for package information.

4.2 Orderable Part Numbering System



4.3 Mechanical Drawings

Table 4-2 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08AC128 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 4-2, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 4-2) in the "Enter Keyword" search box at the top of the page.

Table 4-2. Package Information

Pin Count	Type	Designator	Document No.
80	LQFP	LK	98ASS23237W
64	QFP	FU	98ASB42844B
48	QFN	FT	98ARH99048A
44	LQFP	FG	98ASS23225W