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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-WFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb21f16a-c-qfn20

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1. Feature List

The EFM8BB2 highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 50 MHz maximum operating frequency
- Memory:
 - Up to 16 KB flash memory, in-system re-programmable from firmware, including 1 KB of 64-byte sectors and 15 KB of 512-byte sectors.
 - Up to 2304 bytes RAM (including 256 bytes standard 8051 RAM and 2048 bytes on-chip XRAM)
- Power:
 - 5 V-input LDO regulator
 - Internal LDO regulator for CPU core voltage
 - Power-on reset circuit and brownout detectors
- I/O: Up to 22 total multifunction I/O pins:
 - All pins 5 V tolerant under bias
 - Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
 - Internal 49 MHz oscillator with accuracy of ±1.5%
 - + Internal 24.5 MHz oscillator with $\pm 2\%$ accuracy
 - Internal 80 kHz low-frequency oscillator
 - External CMOS clock option

- Timers/Counters and PWM:
 - 3-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 5 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- Communications and Digital Peripherals:
 - 2 x UART, up to 3 Mbaud
 - SPI[™] Master / Slave, up to 12 Mbps
 - SMBus™/I2C™ Master / Slave, up to 400 kbps
 - I²C High-Speed Slave, up to 3.4 Mbps
 - 16-bit CRC unit, supporting automatic CRC of flash at 256byte boundaries
- Analog:
 - 12-Bit Analog-to-Digital Converter (ADC)
 - 2 x Low-current analog comparators with adjustable reference
- On-Chip, Non-Intrusive Debugging
 - Full memory and register inspection
 - · Four hardware breakpoints, single-stepping
- · Pre-loaded UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C
 - Automotive grade available (requires PPAP)
- Single power supply of 2.2 to 3.6 V or 3.0 to 5.25 V
- · QFN28, QSOP24, and QFN20 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB2 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.2 to 3.6 V operation (or up to 5.25 V with the 5 V regulator option) and is available in 28-pin QFN, 20-pin QFN, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

Ordering Part Number	Flash Memory (KB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	5-to-3.3 V Regulator	Temperature Range	Package
EFM8BB21F16I-C-QFN20	16	2304	16	15	10	7	Yes	—	-40 to +125 °C	QFN20
EFM8BB22F16A-C-QFN28	16	2304	22	20	10	12	Yes	Yes	-40 to +125 °C	QFN28
EFM8BB21F16A-C-QFN20	16	2304	16	15	10	7	Yes	_	-40 to +125 °C	QFN20

The A-grade (i.e. EFM8BB21F16A-C-QFN20) devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account.

3. System Overview

3.1 Introduction



Figure 3.1. Detailed EFM8BB2 Block Diagram

This section describes the EFM8BB2 family at a high level. For more information on each module including register definitions, see the EFM8BB2 Reference Manual.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- · Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- · Automatic parity generation and checking.
- · Four byte FIFO on transmit and receive.
- Auto-baud detection.
- LIN break and sync field detection.
- CTS / RTS hardware flow control.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disable to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- · Supports 3- or 4-wire master or slave modes.
- · Supports external clock frequencies up to 12 Mbps in master or slave mode.
- · Support for all clock phase and polarity modes.
- · 8-bit programmable clock rate (master).
- · Programmable receive timeout (slave).
- Four byte FIFO on transmit and receive.
- · Can operate in suspend or snooze modes and wake the CPU on reception of a byte.
- Support for multiple masters on the same data lines.

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- · Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- · Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- · Clock low extending (clock stretching) to interface with faster masters
- · Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- · Ability to inhibit all slave states
- Programmable data setup/hold times
- · Transmit and receive FIFOs (one byte) to help increase throughput in faster applications

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- · Up to 10 (CMP0) or 12 (CMP1) external positive inputs
- · Up to 10 (CMP0) or 12 (CMP1) external negative inputs
- Additional input options:
 - Internal connection to LDO output
 - Direct connection to GND
 - Direct connection to VDD
 - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ±20 mV
- Programmable response time
- · Interrupts generated on rising, falling, or both edges
- PWM output kill feature

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- · Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- · Supply monitor reset (monitors VDD supply)
- · Watchdog timer reset
- · Missing clock detector reset
- · Flash error reset

3.9 Debugging

The EFM8BB2 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

4.1.2 Power Consumption

Parameter Symbol Test Condition		Min	Тур	Max	Unit	
Digital Core Supply Current (G-grade devices, -40 °C to +85 °C)						
Normal Mode-Full speed with code	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²		9.4	10.1	mA
		F_{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	4.5	5.2	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²		600	900	μA
		F _{SYSCLK} = 80 kHz ³		145	410	μA
Idle Mode-Core halted with periph-	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²		6.3	6.8	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	2.9	3.3	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	440	750	μA
		F _{SYSCLK} = 80 kHz ³		130	420	μA
Suspend Mode-Core halted and	I _{DD}	LFO Running	_	125	400	μA
Supply monitor off.		LFO Stopped		120	390	μA
Snooze Mode-Core halted and	I _{DD}	LFO Running		25	300	μA
Regulator in low-power state, Sup- ply monitor off.		LFO Stopped		20	290	μA
Stop Mode—Core halted and all clocks stopped,Internal LDO On, Supply monitor off.	I _{DD}		_	120	390	μΑ
Shutdown Mode—Core halted and I _{DD} all clocks stopped,Internal LDO Off, Supply monitor off.			_	0.2	3	μA
Digital Core Supply Current (I-gra	de or A-gra	de devices, -40 °C to +125 °C)				
Normal Mode-Full speed with code	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²		9.4	10.9	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²		4.5	5.6	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	600	1555	μA
		F _{SYSCLK} = 80 kHz ³	_	145	1070	μA
Idle Mode-Core halted with periph-	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²		6.3	7.4	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²		2.9	3.9	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²		440	1400	μA
		F _{SYSCLK} = 80 kHz ³		130	1050	μA
Suspend Mode-Core halted and	I _{DD}	LFO Running	_	125	1050	μA
Supply monitor off.		LFO Stopped		120	1045	μA
Snooze Mode-Core halted and	I _{DD}	LFO Running	—	25	950	μA
Regulator in low-power state, Sup- ply monitor off.		LFO Stopped	_	20	940	μA

Table 4.2. Power Consumption

4.1.3 Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
VDD Supply Monitor Threshold	V _{VDDM}		1.95	2.05	2.15	V
Power-On Reset (POR) Threshold	V _{POR}	Rising Voltage on VDD	_	1.2	_	V
		Falling Voltage on VDD	0.75	_	1.36	V
VDD Ramp Time	t _{RMP}	Time to V _{DD} > 2.2 V	10	_	_	μs
Reset Delay from POR	t _{POR}	Relative to V _{DD} > V _{POR}	3	10	31	ms
Reset Delay from non-POR source	t _{RST}	Time between release of reset source and code execution	_	50	_	μs
RST Low Time to Generate Reset	t _{RSTL}		15		_	μs
Missing Clock Detector Response Time (final rising edge to reset)	t _{MCD}	F _{SYSCLK} >1 MHz	_	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F _{MCD}		_	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t _{MON}		_	2		μs

Table 4.3. Reset and Supply Monitor

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Тур	Мах	Units
Write Time ^{1,2}	t _{WRITE}	One Byte,	19	20	21	μs
		F _{SYSCLK} = 24.5 MHz				
Erase Time ^{1 ,2}	t _{ERASE}	One Page,	5.2	5.35	5.5	ms
		F _{SYSCLK} = 24.5 MHz				
V _{DD} Voltage During Programming ³	V _{PROG}		2.2		3.6	V
Endurance (Write/Erase Cycles)	N _{WE}		20k	100k	—	Cycles

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.

2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.

3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).

4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.3 Absolute Maximum Ratings

Stresses above those listed in Table 4.16 Absolute Maximum Ratings on page 24 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.16. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Мах	Unit
Ambient Temperature Under Bias	T _{BIAS}		-55	125	°C
Storage Temperature	T _{STG}		-65	150	°C
Voltage on VDD	V _{DD}		GND-0.3	4.2	V
Voltage on VREGIN	V _{REGIN}		GND-0.3	5.8	V
Voltage on I/O pins or RSTb	V _{IN}	V _{DD} > 3.3 V	GND-0.3	5.8	V
		V _{DD} < 3.3 V	GND-0.3	V _{DD} +2.5	V
Total Current Sunk into Supply Pin	I _{VDD}		_	200	mA
Total Current Sourced out of Ground Pin	I _{GND}		200	_	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I _{IO}		-100	100	mA
Operating Junction Temperature	TJ	$T_A = -40 \ ^{\circ}C \text{ to } 85 \ ^{\circ}C$	-40	105	°C
		T_A = -40 °C to 125 °C (I-grade or A- grade parts only)	-40	130	°C
Note:					

1. Exposure to maximum rating conditions for extended periods may affect device reliability.



Figure 4.5. Typical ADC0 Supply Current in Normal (always-on) Mode

6. Pin Definitions

6.1 EFM8BB2x-QFN28 Pin Definitions



Figure 6.1. EFM8BB2x-QFN28 Pinout

Pin	Pin Name	Description	Crossbar Capability	Additional Digital	Analog Functions
Number					
16	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14
				I2C0_SCL	CP1P.6
					CP1N.6
17	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13
				I2C0_SDA	CP1P.5
					CP1N.5
18	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12
					CP1P.4
					CP1N.4
19	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11
					CP1P.3
					CP1N.3
20	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10
					CP1P.2
					CP1N.2
21	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9
					CP1P.1
					CP1N.1
					CMP0P.10
					CMP0N.10
22	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8
					CP1P.0
					CP1N.0
					CMP0P.9
					CMP0N.9
23	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.7
				INT0.7	CMP0P.7
				INT1.7	CMP0N.7
24	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.6
				CNVSTR	CMP0P.6
				INT0.6	CMP0N.6
				INT1.6	
25	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.5
				INT0.5	CMP0P.5
				INT1.5	CMP0N.5
				UART0_RX	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
16	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12
					CMP1P.4
					CMP1N.4
17	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11
					CMP1P.3
					CMP1N.3
18	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10
					CMP1P.2
					CMP1N.2
19	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9
					CMP1P.1
					CMP1N.1
					CMP0P.10
					CMP0N.10
20	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8
					CMP1P.0
					CMP1N.0
					CMP0P.9
					CMP0N.9
21	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.7
				INT0.7	CMP0P.7
				INT1.7	CMP0N.7
22	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.6
				CNVSTR	CMP0P.6
				INT0.6	CMP0N.6
				INT1.6	
23	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.5
				INT0.5	CMP0P.5
				INT1.5	CMP0N.5
				UART0_RX	
24	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.4
				INT0.4	CMP0P.4
				INT1.4	CMP0N.4
				UART0_TX	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
16	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.6
				CNVSTR	CMP0P.6
				INT0.6	CMP0N.6
				INT1.6	
17	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.5
				INT0.5	CMP0P.5
				INT1.5	CMP0N.5
				UART0_RX	
18	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.4
				INT0.4	CMP0P.4
				INT1.4	CMP0N.4
				UART0_TX	
19	P0.3	Multifunction I/O	Yes	P0MAT.3	ADC0.3
				EXTCLK	CMP0P.3
				INT0.3	CMP0N.3
				INT1.3	
20	P0.2	Multifunction I/O	Yes	P0MAT.2	ADC0.2
				INT0.2	CMP0P.2
				INT1.2	CMP0N.2
Center	GND	Ground			

7. QFN28 Package Specifications

7.1 QFN28 Package Dimensions



Figure 7.1. QFN28 Package Drawing

Table 7.1. QFN28 Package Dimensions

Dimension	Min	Тур	Мах			
A	0.70	0.75	0.80			
A1	0.00	_	0.05			
A3		0.20 REF				
b	0.20	0.20 0.25 0.30				
D	5.00 BSC					
D2	3.15	3.25	3.35			
е	0.50 BSC					
E		5.00 BSC				
E2	3.15	3.25	3.35			
L	0.45 0.55 0.65					
ааа	0.10					
bbb	0.10					
ddd		0.05				

Dimension	Min	Тур	Мах			
eee	0.08					
Note:						

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC Solid State Outline MO-220.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Dimension	Min	Тур	Мах
ааа		0.20	
bbb		0.18	
ссс		0.10	
ddd		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC outline MO-137, variation AE.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. QFN20 Package Specifications

9.1 QFN20 Package Dimensions



Figure 9.1. QFN20 Package Drawing

Table 9.1.	QFN20	Package	Dimensions
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Dimension	Min	Тур	Мах	
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A3	0.20 REF			
b	0.18	0.25	0.30	
c	0.25	0.30	0.35	
D	3.00 BSC			
D2	1.6	1.70	1.80	
e	0.50 BSC			

Dimension	Min	Max
Note:		
1. All dimensions shown are in millimeters	(mm) unless otherwise noted.	
2. Dimensioning and Tolerancing is per the	ANSI Y14.5M-1994 specification.	
3. This Land Pattern Design is based on th	e IPC-7351 guidelines.	
 All metal pads are to be non-solder mas minimum, all the way around the pad. 	k defined (NSMD). Clearance between the so	lder mask and the metal pad is to be 60 μm
5. A stainless steel, laser-cut and electro-p	olished stencil with trapezoidal walls should b	be used to assure good solder paste release.
6. The stencil thickness should be 0.125 m	ım (5 mils).	
7. The ratio of stencil aperture to land pad	size should be 1:1 for the perimeter pads.	
8. A 2 x 2 array of 0.75 mm openings on a	0.95 mm pitch should be used for the center	pad to assure proper paste volume.
9. A No-Clean, Type-3 solder paste is reco	mmended.	

10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN20 Package Marking



Figure 9.3. QFN20 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

10. Revision History

10.1 Revision 1.31

November 7, 2016

Updated typical and maximum specifications in 4.1.2 Power Consumption.

Added 4.1.11 1.8 V Internal LDO Voltage Regulator.

10.2 Revision 1.3

August 11, 2016

Added A-grade parts.

Added Thermal Resistance (Junction to Case) for QFN20 packages to 4.2 Thermal Conditions.

Added a note to Table 4.2 Power Consumption on page 13 providing more information about the Comparator Reference specification.

Added a note linking to the Typical VOH and VOL Performance graphs in 4.1.14 Port I/O.

Specified the sizes of the SMBus and I2CSLAVE transmit and receive FIFOs.

Added a note to 3.1 Introduction referencing the Reference Manual.

10.3 Revision 1.2

February 10, 2016

Updated Figure 5.3 Debug Connection Diagram on page 30 to move the pull-up resistor on C2D / RSTb to after the series resistor instead of before.

Added a reference to AN945: EFM8 Factory Bootloader User Guide in 3.10 Bootloader.

Added I-grade parts.

Adjusted and added maximum specifications in 4.1.2 Power Consumption for G-grade devices and added a note on which high frequency oscillator is used for the specification.

Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in 4.3 Absolute Maximum Ratings.

10.4 Revision 1.1

December 16, 2015

Updated 3.2 Power to properly reflect that a comparator falling edge wakes the device from Suspend and Snooze.

Added Note 2 to Table 4.1 Recommended Operating Conditions on page 12.

Added 5.2 Debug.

10.5 Revision 1.0

Updated any TBD numbers in and adjusted various specifications.

Updated VOH and VOL graphs in Figure 4.6 Typical V_{OH} Curves on page 28 and Figure 4.7 Typical V_{OL} Curves on page 28 and updated the VOH and VOL specifications in Table 4.14 Port I/O on page 23.

Added more information to 3.10 Bootloader.

Updated part numbers to Revision C.

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