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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, GFX, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128da106-i-pt

PIC24FJ256DA210 FAMILY

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TABLE 4-21: ADC REGISTER MAP (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
AD1CON1	0320	ADON	—	ADSIDL	—	—	—	FORM1	FORM0	SSRC2	SSRC1	SSRC0	—	—	ASAM	SAMP	DONE	0000
AD1CON2	0322	VCFG2	VCFG1	VCFG0	r	—	CSCNA	—	—	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	0324	ADRC	r	r	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS	0328	CH0NB	—	—	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA	—	—	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	032E	—	—	—	—	CSSL27	CSSL26	CSSL25	CSSL24	CSSL23 ⁽¹⁾	CSSL22 ⁽¹⁾	CSSL21 ⁽¹⁾	CSSL20 ⁽¹⁾	CSSL19 ⁽¹⁾	CSSL18 ⁽¹⁾	CSSL17 ⁽¹⁾	CSSL16 ⁽¹⁾	0000
AD1CSSL	0330	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000

Legend: — = unimplemented, read as '0', r = reserved, maintain as '0'. Reset values are shown in hexadecimal.

Note 1: Unimplemented in 64-pin devices, read as '0'

TABLE 4-22: CTMU REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON	033C	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	EDG2POL	EDG2SEL1	EDG2SEL0	EDG1POL	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT	0000
CTMUICON	033E	ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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4.3.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. **TBLRDL** (Table Read Low): In Word mode, it maps the lower word of the program space location ($P<15:0>$) to a data address ($D<15:0>$). In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

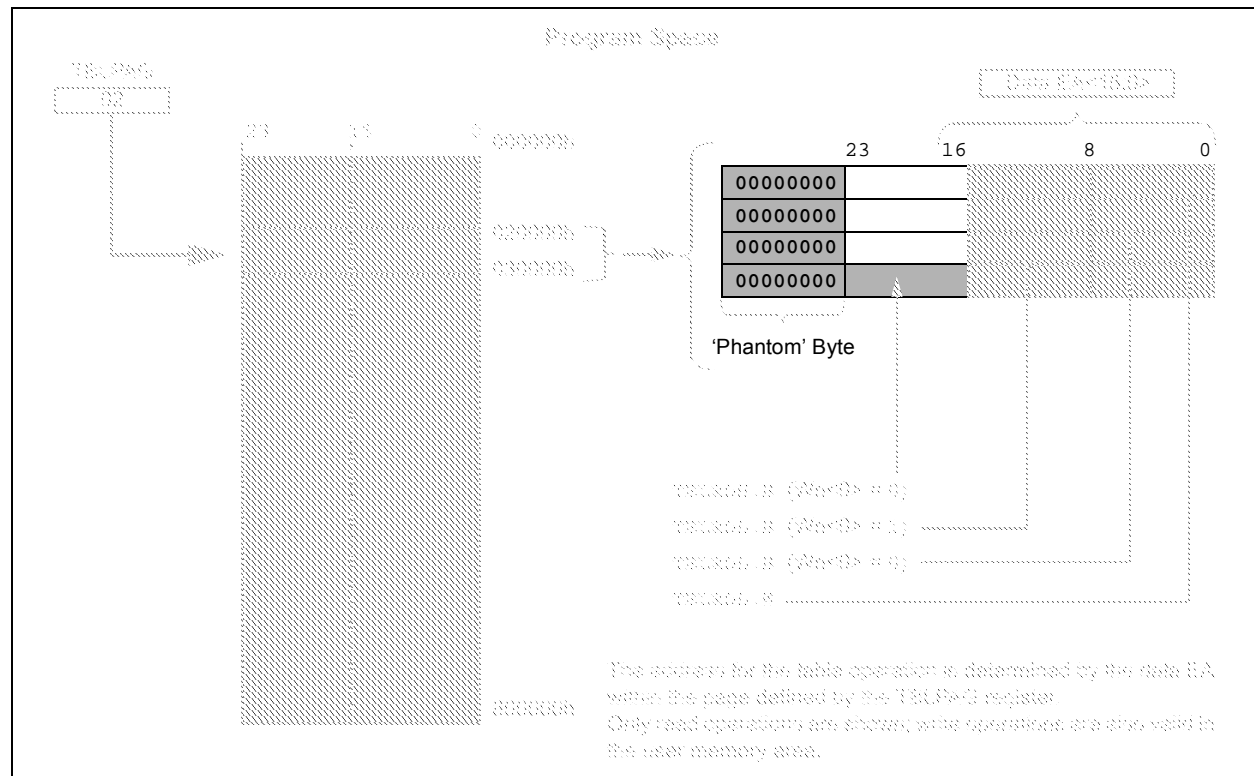
2. **TBLRDH** (Table Read High): In Word mode, it maps the entire upper word of a program address ($P<23:16>$) to a data address. Note that $D<15:8>$, the 'phantom' byte, will always be '0'. In Byte mode, it maps the upper or lower byte of the program word to $D<7:0>$ of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (byte select = 1).

In a similar fashion, two table instructions, `TBLWTH` and `TBLWTL`, are used to write individual bytes or words to a program space address. The details of their operation are described in **Section 5.0 “Flash Program Memory”**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

Note: Only table read operations will execute in the configuration memory space, where Device IDs are located. Table write operations are not allowed.

FIGURE 4-9: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



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6.1 Special Function Register Reset States

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of four registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the FNOSC bits in Flash Configuration Word 2 (CW2) (see Table 6-2). The RCFGAL and NVMCON registers are only affected by a POR.

6.2 Device Reset Times

The Reset times for various types of device Reset are summarized in Table 6-3. Note that the system Reset signal, $\overline{\text{SYSRST}}$, is released after the POR delay time expires.

The time at which the device actually begins to execute code will also depend on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable $\overline{\text{SYSRST}}$ delay times.

The Fail-Safe Clock Monitor (FSCM) delay determines the time at which the FSCM begins to monitor the system clock source after the $\overline{\text{SYSRST}}$ signal is released.

6.3 Clock Source Selection at Reset

If clock switching is enabled, the system clock source at device Reset is chosen, as shown in Table 6-2. If clock switching is disabled, the system clock source is always selected according to the oscillator Configuration bits. Refer to the “PIC24F Family Reference Manual”, Section 8.0 “Oscillator Configuration” for further details.

TABLE 6-2: OSCILLATOR SELECTION vs. TYPE OF RESET (CLOCK SWITCHING ENABLED)

Reset Type	Clock Source Determinant
POR	FNOSC Configuration bits (CW2<10:8>)
BOR	
$\overline{\text{MCLR}}$	COSC Control bits (OSCCON<14:12>)
WDTO	
SWR	

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TABLE 7-2: IMPLEMENTED INTERRUPT VECTORS

Interrupt Source	Vector Number	IVT Address	AIVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
ADC1 Conversion Done	13	00002Eh	00012Eh	IFS0<13>	IEC0<13>	IPC3<6:4>
Comparator Event	18	000038h	000138h	IFS1<2>	IEC1<2>	IPC4<10:8>
CRC Generator	67	00009Ah	00019Ah	IFS4<3>	IEC4<3>	IPC16<14:12>
CTMU Event	77	0000AEh	0001AEh	IFS4<13>	IEC4<13>	IPC19<6:4>
External Interrupt 0	0	000014h	000114h	IFS0<0>	IEC0<0>	IPC0<2:0>
External Interrupt 1	20	00003Ch	00013Ch	IFS1<4>	IEC1<4>	IPC5<2:0>
External Interrupt 2	29	00004Eh	00014Eh	IFS1<13>	IEC1<13>	IPC7<6:4>
External Interrupt 3	53	00007Eh	00017Eh	IFS3<5>	IEC3<5>	IPC13<6:4>
External Interrupt 4	54	000080h	000180h	IFS3<6>	IEC3<6>	IPC13<10:8>
Graphics Controller	100	0000DCh	0001DCh	IFS6<4>	IEC6<4>	IPC25<2:0>
I2C1 Master Event	17	000036h	000136h	IFS1<1>	IEC1<1>	IPC4<6:4>
I2C1 Slave Event	16	000034h	000134h	IFS1<0>	IEC1<0>	IPC4<2:0>
I2C2 Master Event	50	000078h	000178h	IFS3<2>	IEC3<2>	IPC12<10:8>
I2C2 Slave Event	49	000076h	000176h	IFS3<1>	IEC3<1>	IPC12<6:4>
I2C3 Master Event	85	0000BEh	0001BEh	IFS5<5>	IEC5<5>	IPC21<6:4>
I2C3 Slave Event	84	0000BCh	0001BCh	IFS5<4>	IEC5<4>	IPC21<2:0>
Input Capture 1	1	000016h	000116h	IFS0<1>	IEC0<1>	IPC0<6:4>
Input Capture 2	5	00001Eh	00011Eh	IFS0<5>	IEC0<5>	IPC1<6:4>
Input Capture 3	37	00005Eh	00015Eh	IFS2<5>	IEC2<5>	IPC9<6:4>
Input Capture 4	38	000060h	000160h	IFS2<6>	IEC2<6>	IPC9<10:8>
Input Capture 5	39	000062h	000162h	IFS2<7>	IEC2<7>	IPC9<14:12>
Input Capture 6	40	000064h	000164h	IFS2<8>	IEC2<8>	IPC10<2:0>
Input Capture 7	22	000040h	000140h	IFS1<6>	IEC1<6>	IPC5<10:8>
Input Capture 8	23	000042h	000142h	IFS1<7>	IEC1<7>	IPC5<14:12>
Input Capture 9	93	0000CEh	0001CEh	IFS5<13>	IEC5<13>	IPC23<6:4>
Input Change Notification (ICN)	19	00003Ah	00013Ah	IFS1<3>	IEC1<3>	IPC4<14:12>
Low-Voltage Detect (LVD)	72	0000A4h	0001A4h	IFS4<8>	IEC4<8>	IPC18<2:0>
Output Compare 1	2	000018h	000118h	IFS0<2>	IEC0<2>	IPC0<10:8>
Output Compare 2	6	000020h	000120h	IFS0<6>	IEC0<6>	IPC1<10:8>
Output Compare 3	25	000046h	000146h	IFS1<9>	IEC1<9>	IPC6<6:4>
Output Compare 4	26	000048h	000148h	IFS1<10>	IEC1<10>	IPC6<10:8>
Output Compare 5	41	000066h	000166h	IFS2<9>	IEC2<9>	IPC10<6:4>
Output Compare 6	42	000068h	000168h	IFS2<10>	IEC2<10>	IPC10<10:8>
Output Compare 7	43	00006Ah	00016Ah	IFS2<11>	IEC2<11>	IPC10<14:12>
Output Compare 8	44	00006Ch	00016Ch	IFS2<12>	IEC2<12>	IPC11<2:0>
Output Compare 9	92	0000CCh	0001CCh	IFS5<12>	IEC5<12>	IPC23<2:0>
Enhanced Parallel Master Port (EPMP) ⁽¹⁾	45	00006Eh	00016Eh	IFS2<13>	IEC2<13>	IPC11<6:4>
Real-Time Clock and Calendar (RTCC)	62	000090h	000190h	IFS3<14>	IEC3<14>	IPC15<10:8>
SPI1 Error	9	000026h	000126h	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 Event	10	000028h	000128h	IFS0<10>	IEC0<10>	IPC2<10:8>
SPI2 Error	32	000054h	000154h	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 Event	33	000056h	000156h	IFS2<1>	IEC2<1>	IPC8<6:4>
SPI3 Error	90	0000C8h	0001C8h	IFS5<10>	IEC5<10>	IPC22<10:8>
SPI3 Event	91	0000CAh	0001CAh	IFS5<11>	IEC5<11>	IPC22<14:12>

Note 1: Not available in 64-pin devices (PIC24FJXXXDAX06).

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REGISTER 7-23: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14-12	CNIP<2:0>: Input Change Notification Interrupt Priority bits
	111 = Interrupt is priority 7 (highest priority interrupt)
	•
	•
	•
	001 = Interrupt is priority 1
	000 = Interrupt source is disabled
bit 11	Unimplemented: Read as '0'
bit 10-8	CMIP<2:0>: Comparator Interrupt Priority bits
	111 = Interrupt is priority 7 (highest priority interrupt)
	•
	•
	•
	001 = Interrupt is priority 1
	000 = Interrupt source is disabled
bit 7	Unimplemented: Read as '0'
bit 6-4	MI2C1IP<2:0>: Master I2C1 Event Interrupt Priority bits
	111 = Interrupt is priority 7 (highest priority interrupt)
	•
	•
	•
	001 = Interrupt is priority 1
	000 = Interrupt source is disabled
bit 3	Unimplemented: Read as '0'
bit 2-0	SI2C1IP<2:0>: Slave I2C1 Event Interrupt Priority bits
	111 = Interrupt is priority 7 (highest priority interrupt)
	•
	•
	•
	001 = Interrupt is priority 1
	000 = Interrupt source is disabled

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REGISTER 8-4: CLKDIV2: CLOCK DIVIDER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
GCLKDIV6 ⁽¹⁾	GCLKDIV5 ⁽¹⁾	GCLKDIV4 ⁽¹⁾	GCLKDIV3 ⁽¹⁾	GCLKDIV2 ⁽¹⁾	GCLKDIV1 ⁽¹⁾	GCLKDIV0 ⁽¹⁾	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at all Resets

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-9 **GCLKDIV<6:0>**: Display Module Interface Clock Divider Selection bits⁽¹⁾

(Values are based on a 96 MHz clock source set by G1CLKSEL (CLKDIV<4>) = 1. When the 48 MHz clock source is selected, G1CLKSEL (CLKDIV<4>) = 0; all values are divided by 2.)⁽¹⁾

11111111 = (127) 1.50 MHz (divide by 64)

11111110 = (126) 1.52 MHz (divide by 63)

.

.

.

11000011 = (97) 2.82 MHz (divide by 34)

11000010 = (96) 2.91 MHz (divide by 33); from here, increment the divisor by 1.00

10111111 = (95) 2.95 MHz (divide by 32.50)

.

.

.

10000000 = (65) 5.49 MHz (divide by 17.50)

10000001 = (64) 5.65 MHz (divide by 17.00); from here, increment the divisor by 0.50

01111111 = (63) 5.73 MHz (divide by 16.75)

.

.

.

00000111 = (3) 54.86 MHz (divide by 1.75)

00000110 = (2) 64.00 MHz (divide by 1.5)

00000101 = (1) 76.80 MHz (divide by 1.25); from here, increment the divisor by 0.25

00000100 = (0) 96.00 MHz (divide by 1)

bit 8-0 **Unimplemented:** Read as '0'

Note 1: These bits take effect only when the 96 MHz PLL is enabled.

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REGISTER 13-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R-0, HSC	R-0, HSC	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2 ⁽¹⁾	ICM1 ⁽¹⁾	ICM0 ⁽¹⁾
bit 7						bit 0	

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture x Module Stop in Idle Control bit
 1 = Input capture module halts in CPU Idle mode
 0 = Input capture module continues to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture Timer Select bits
 111 = System clock (FOSC/2)
 110 = Reserved
 101 = Reserved
 100 = Timer1
 011 = Timer5
 010 = Timer4
 001 = Timer2
 000 = Timer3

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Select Number of Captures Per Interrupt bits
 11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
 1 = Input capture overflow occurred
 0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture x Buffer Empty Status bit (read-only)
 1 = Input capture buffer is not empty, at least one more capture value can be read
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits⁽¹⁾
 111 = Interrupt mode: input capture functions as an interrupt pin only when the device is in Sleep or Idle mode (rising edge detect only, all other control bits are not applicable)
 110 = Unused (module disabled)
 101 = Prescaler Capture mode: capture on every 16th rising edge
 100 = Prescaler Capture mode: capture on every 4th rising edge
 011 = Simple Capture mode: capture on every rising edge
 010 = Simple Capture mode: capture on every falling edge
 001 = Edge Detect Capture mode: capture on every edge (rising and falling), ICI<1:0> bits do not control interrupt generation for this mode
 000 = Input capture module turned off

Note 1: The ICx input must also be configured to an available RPN/RPIn pin. For more information, see **Section 10.4 "Peripheral Pin Select (PPS)"**.

16.0 INTER-INTEGRATED CIRCUIT™ (I²C™)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “PIC24F Family Reference Manual”, **Section 24. “Inter-Integrated Circuit™ (I²C™)”** (DS39702). The information in this data sheet supersedes the information in the FRM.

The Inter-Integrated Circuit™ (I²C™) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, display drivers, A/D Converters, etc.

The I²C module supports these features:

- Independent master and slave logic
- 7-bit and 10-bit device addresses
- General call address, as defined in the I²C protocol
- Clock stretching to provide delays for the processor to respond to a slave data request
- Both 100 kHz and 400 kHz bus specifications
- Configurable address masking
- Multi-Master modes to prevent loss of messages in arbitration
- Bus Repeater mode, allowing the acceptance of all messages as a slave regardless of the address
- Automatic SCL

A block diagram of the module is shown in Figure 16-1.

16.1 Communicating as a Master in a Single Master Environment

The details of sending a message in Master mode depends on the communications protocol for the device being communicated with. Typically, the sequence of events is as follows:

1. Assert a Start condition on SDAx and SCLx.
2. Send the I²C device address byte to the slave with a write indication.
3. Wait for and verify an Acknowledge from the slave.
4. Send the first data byte (sometimes known as the command) to the slave.
5. Wait for and verify an Acknowledge from the slave.
6. Send the serial memory address low byte to the slave.
7. Repeat steps 4 and 5 until all data bytes are sent.
8. Assert a Repeated Start condition on SDAx and SCLx.
9. Send the device address byte to the slave with a read indication.
10. Wait for and verify an Acknowledge from the slave.
11. Enable master reception to receive serial memory data.
12. Generate an ACK or NACK condition at the end of a received byte of data.
13. Generate a Stop condition on SDAx and SCLx.

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18.4.2 RECEIVING AN IN TOKEN IN DEVICE MODE

1. Attach to a USB host and enumerate as described in *“Chapter 9 of the USB 2.0 Specification”*.
2. Create a data buffer and populate it with the data to send to the host.
3. In the appropriate (even or odd) TX BD for the desired endpoint:
 - a) Set up the status register (BDnSTAT) with the correct data toggle (DATA0/1) value and the byte count of the data buffer.
 - b) Set up the address register (BDnADR) with the starting address of the data buffer.
 - c) Set the UOWN bit of the status register to ‘1’.
4. When the USB module receives an IN token, it automatically transmits the data in the buffer. Upon completion, the module updates the status register (BDnSTAT) and sets the Transfer Complete Interrupt Flag, TRNIF (U1IR<3>).

18.4.3 RECEIVING AN OUT TOKEN IN DEVICE MODE

1. Attach to a USB host and enumerate as described in *“Chapter 9 of the USB 2.0 Specification”*.
2. Create a data buffer with the amount of data you are expecting from the host.
3. In the appropriate (even or odd) TX BD for the desired endpoint:
 - a) Set up the status register (BDnSTAT) with the correct data toggle (DATA0/1) value and the byte count of the data buffer.
 - b) Set up the address register (BDnADR) with the starting address of the data buffer.
 - c) Set the UOWN bit of the status register to ‘1’.
4. When the USB module receives an OUT token, it automatically receives the data sent by the host to the buffer. Upon completion, the module updates the status register (BDnSTAT) and sets the Transfer Complete Interrupt Flag, TRNIF (U1IR<3>).

18.5 Host Mode Operation

The following sections describe how to perform common Host mode tasks. In Host mode, USB transfers are invoked explicitly by the host software. The host software is responsible for the Acknowledge portion of the transfer. Also, all transfers are performed using the Endpoint 0 Control register (U1EP0) and Buffer Descriptors.

18.5.1 ENABLE HOST MODE AND DISCOVER A CONNECTED DEVICE

1. Enable Host mode by setting the HOSTEN bit (U1CON<3>). This causes the Host mode control bits in other USB OTG registers to become available.
2. Enable the D+ and D- pull-down resistors by setting the DPPULDWN and DMPULDWN bits (U1OTGCON<5:4>). Disable the D+ and D-pull-up resistors by clearing the DPPULUP and DMPULUP bits (U1OTGCON<7:6>).
3. At this point, SOF generation begins with the SOF counter loaded with 12,000. Eliminate noise on the USB by clearing the SOFEN bit (U1CON<0>) to disable Start-Of-Frame packet generation.
4. Enable the device attached interrupt by setting the ATTACHIE bit (U1IE<6>).
5. Wait for the device attached interrupt (U1IR<6> = 1). This is signaled by the USB device changing the state of D+ or D- from ‘0’ to ‘1’ (SE0 to J state). After it occurs, wait 100 ms for the device power to stabilize.
6. Check the state of the JSTATE and SE0 bits in U1CON. If the JSTATE bit (U1CON<7>) is ‘0’, the connecting device is low speed. If the connecting device is low speed, set the low LSPDEN and LSPD bits (U1ADDR<7> and U1EP0<7>) to enable low-speed operation.
7. Reset the USB device by setting the USBRST bit (U1CON<4>) for at least 50 ms, sending Reset signaling on the bus. After 50 ms, terminate the Reset by clearing USBRST.
8. In order to keep the connected device from going into suspend, enable the SOF packet generation by setting the SOFEN bit.
9. Wait 10 ms for the device to recover from Reset.
10. Perform enumeration as described by *“Chapter 9 of the USB 2.0 Specification”*.

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18.7 USB OTG Module Registers

There are a total of 37 memory mapped registers associated with the USB OTG module. They can be divided into four general categories:

- USB OTG Module Control (12)
- USB Interrupt (7)
- USB Endpoint Management (16)
- USB VBus Power Control (2)

This total does not include the (up to) 128 BD registers in the BDT. Their prototypes, described in Register 18-1 and Register 18-2, are shown separately in **Section 18.2 “USB Buffer Descriptors and the BDT”**.

With the exception of U1PWMCON and U1PWMRRS, all USB OTG registers are implemented in the Least Significant Byte of the register. Bits in the upper byte are unimplemented and have no function. Note that some registers are instantiated only in Host mode, while other registers have different bit instantiations and functions in Device and Host modes.

The registers described in the following sections are those that have bits with specific control and configuration features. The following registers are used for data or address values only:

- U1BDTP1: Specifies the 256-word page in data RAM used for the BDT; 8-bit value with bit 0 fixed as '0' for boundary alignment.
- U1FRML and U1FRMH: Contains the 11-bit byte counter for the current data frame.
- U1PWMRRS: Contains the 8-bit value for PWM duty cycle bits<15:8> and PWM period bits<7:0> for the VBus boost assist PWM module.

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REGISTER 18-8: U1CON: USB CONTROL REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x, HSC	R-x, HSC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
JSTATE	SE0	TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	SOFEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'						
R = Readable bit	W = Writable bit		HSC = Hardware Settable/Clearable bit				
-n = Value at POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **JSTATE:** Live Differential Receiver J State Flag bit
 1 = J state (differential '0' in low speed, differential '1' in full speed) is detected on the USB
 0 = No J state is detected
- bit 6 **SE0:** Live Single-Ended Zero Flag bit
 1 = Single-ended zero is active on the USB bus
 0 = No single-ended zero is detected
- bit 5 **TOKBUSY:** Token Busy Status bit
 1 = Token is being executed by the USB module in On-The-Go state
 0 = No token is being executed
- bit 4 **USBRST:** Module Reset bit
 1 = USB Reset has been generated; for software Reset, application must set this bit for 50 ms, then clear it
 0 = USB Reset is terminated
- bit 3 **HOSTEN:** Host Mode Enable bit
 1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
 0 = USB host capability is disabled
- bit 2 **RESUME:** Resume Signaling Enable bit
 1 = Resume signaling is activated; software must set bit for 10 ms and then clear to enable remote wake-up
 0 = Resume signaling is disabled
- bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
 1 = Reset all Ping-Pong Buffer Pointers to the even BD banks
 0 = Ping-Pong Buffer Pointers are not reset
- bit 0 **SOFEN:** Start-Of-Frame Enable bit
 1 = Start-Of-Frame token is sent every one 1 ms
 0 = Start-Of-Frame token is disabled

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20.2 Calibration

The real-time crystal input can be calibrated using the periodic auto-adjust feature. When properly calibrated, the RTCC can provide an error of less than 3 seconds per month. This is accomplished by finding the number of error clock pulses for one minute and storing the value into the lower half of the RCFGAL register. The 8-bit signed value loaded into the lower half of RCFGAL is multiplied by four and will either be added or subtracted from the RTCC timer, once every minute. Refer to the following steps for RTCC calibration:

1. Using another timer resource on the device, the user must find the error of the 32.768 kHz crystal.
2. Once the error is known, it must be converted to the number of error clock pulses per minute and loaded into the RCFGAL register.

EQUATION 20-1: RTCC CALIBRATION

Error (clocks per minute) = (Ideal Frequency[†] – Measured Frequency) x 60

[†]Ideal Frequency = 32,768Hz

3. a) If the oscillator is faster than ideal (negative result from Step 2), the RCFGAL register value needs to be negative. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.
b) If the oscillator is slower than ideal (positive result from Step 2), the RCFGAL register value needs to be positive. This causes the specified number of clock pulses to be added to the timer counter, once every minute.
4. Divide the number of error clocks per minute by 4 to get the correct CAL value and load the RCFGAL register with the correct value.
(Each 1-bit increment in CAL adds or subtracts 4 pulses).

Writes to the lower half of the RCFGAL register should only occur when the timer is turned off or immediately after the rising edge of the seconds pulse.

Note: It is up to the user to include in the error value the initial error of the crystal, drift due to temperature and drift due to crystal aging.

20.3 Alarm

- Configurable from half second to one year
- Enabled using the ALRMEN bit (ALCFGRPT<15>, Register 20-3)
- One-time alarm and repeat alarm options available

20.3.1 CONFIGURING THE ALARM

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. Writes to ALRMVAL should only take place when ALRMEN = 0.

As shown in Figure 20-2, the interval selection of the alarm is configured through the AMASK bits (ALCFGRPT<13:10>). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur.

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs, once the alarm is enabled, is stored in the ARPT bits, ARPT<7:0> (ALCFGRPT<7:0>). When the value of the ARPT bits equals 00h and the CHIME bit (ALCFGRPT<14>) is cleared, the repeat function is disabled and only a single alarm will occur. The alarm can be repeated up to 255 times by loading ARPT<7:0> with FFh.

After each alarm is issued, the value of the ARPT bits is decremented by one. Once the value has reached 00h, the alarm will be issued one last time, after which the ALRMEN bit will be cleared automatically and the alarm will turn off.

Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the value of the ARPT bits reaches 00h, it rolls over to FFh and continues counting indefinitely while CHIME is set.

20.3.2 ALARM INTERRUPT

At every alarm event, an interrupt is generated. In addition, an alarm pulse output is provided that operates at half the frequency of the alarm. This output is completely synchronous to the RTCC clock and can be used as a trigger clock to other peripherals.

Note: Changing any of the registers, other than the RCFGAL and ALCFGRPT registers and the CHIME bit while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = 0). It is recommended that the ALCFGRPT register and CHIME bit be changed when RTCSYNC = 0.

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REGISTER 22-12: G1W2ADRH: GPU WORK AREA 2 START ADDRESS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
W2ADR23	W2ADR22	W2ADR21	W2ADR20	W2ADR19	W2ADR18	W2ADR17	W2ADR16
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'
bit 7-0 **W2ADR<23:16>:** GPU Work Area 2 Start Address High bits
Work area address must point to an even byte address in memory.

REGISTER 22-13: G1PUW: GPU WORK AREA WIDTH REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PUW10	PUW9	PUW8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PUW7	PUW6	PUW5	PUW4	PUW3	PUW2	PUW1	PUW0
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'
bit 10-0 **PUW<10:0>:** GPU Work Area Width bits (in pixels)

REGISTER 22-14: G1PUH: GPU WORK AREA HEIGHT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PUH10	PUH9	PUH8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PUH7	PUH6	PUH5	PUH4	PUH3	PUH2	PUH1	PUH0
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'
bit 10-0 **PUH<10:0>:** GPU Work Area Height bits (in pixels)

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REGISTER 22-15: G1DPADRL: DISPLAY BUFFER START ADDRESS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DPADR15	DPADR14	DPADR13	DPADR12	DPADR11	DPADR10	DPADR9	DPADR8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DPADR7	DPADR6	DPADR5	DPADR4	DPADR3	DPADR2	DPADR1	DPADR0
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15-0 **DPADR<15:0>**: Display Buffer Start Address Low bits
Display buffer start address must point to an even byte address in memory.

REGISTER 22-16: G1DPADRH: DISPLAY BUFFER START ADDRESS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DPADR23	DPADR22	DPADR21	DPADR20	DPADR19	DPADR18	DPADR17	DPADR16
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15-8 **Unimplemented**: Read as '0'
bit 7-0 **DPADR<23:16>**: Display Buffer Start Address High bits
Display buffer start address must point to an even byte address in memory.

REGISTER 22-17: G1DPW: DISPLAY BUFFER WIDTH REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	DPW10	DPW9	DPW8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DPW7	DPW6	DPW5	DPW4	DPW3	DPW2	DPW1	DPW0
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15-11 **Unimplemented**: Read as '0'
bit 10-0 **DPW<10:0>**: Display Frame Width bits (in pixels)

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TABLE 30-15: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
F20	FRC Accuracy @ 8 MHz ^(1,2)	-1	± 0.15	1	%	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	$2.2\text{V} \leq V_{DD} \leq 3.6\text{V}$
F21	LPRC @ 31 kHz	-20	—	20	%	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	VCAP (on-chip regulator output voltage) = 1.8V

- Note 1:** Frequency calibrated at 25°C and 3.3V. OSCTUN bits can be used to compensate for temperature drift.
Note 2: To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.

TABLE 30-16: RC OSCILLATOR START-UP TIME

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions
	TFRC	—	15	—	μs	
	TLPRC	—	50	—	μs	

TABLE 30-17: RESET AND BROWN-OUT RESET REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
SY10	TMCL	MCLR Pulse width (Low)	2	—	—	μs	
SY12	TPOR	Power-on Reset Delay	—	2	—	μs	
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	—	100	ns	
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	μs	$V_{DD} \leq V_{BOR}$
	TRST	Internal State Reset Time	—	50	—	μs	

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