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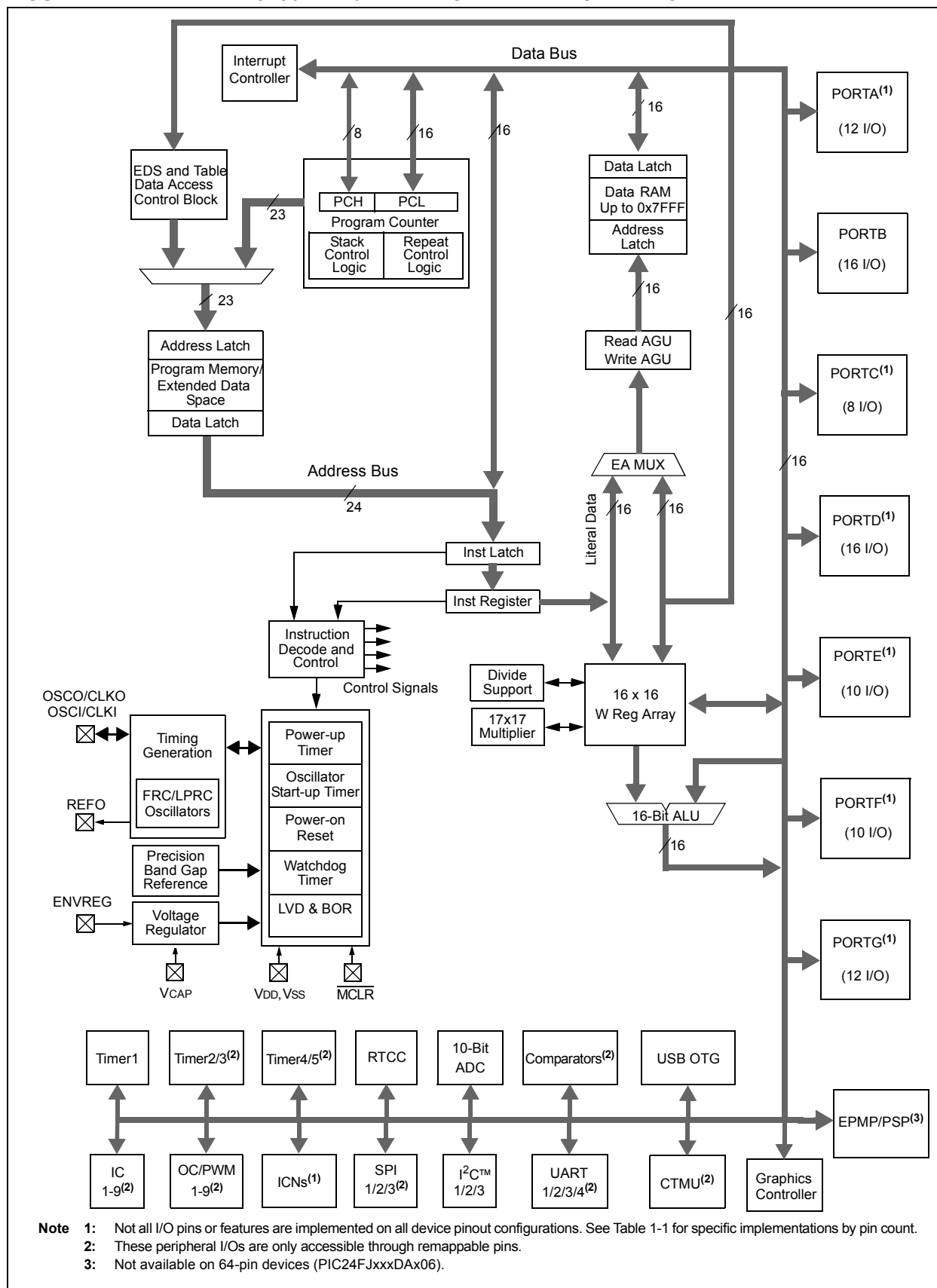
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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, GFX, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256da106-i-pt

PIC24FJ256DA210 FAMILY

FIGURE 1-1: PIC24FJ256DA210 FAMILY GENERAL BLOCK DIAGRAM



PIC24FJ256DA210 FAMILY

TABLE 1-3: PIC24FJ256DA210 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
TCK	27	38	J6	I	ST	JTAG Test Clock Input.
TDI	28	60	G11	I	ST	JTAG Test Data Input.
TDO	24	61	G9	O	—	JTAG Test Data Output.
TMS	23	17	G3	I	ST	JTAG Test Mode Select Input.
USBID	33	51	K10	I	ST	USB OTG ID (OTG mode only).
USBOEN	12	21	H2	O	—	USB Output Enable Control (for external transceiver).
VBUS	34	54	H8	I	ANA	USB Voltage, Host mode (5V).
VBUSCHG	49	76	A11	O	—	External USB Vbus Charge Output.
VBUSON	11	20	H1	O	—	USB OTG External Charge Pump Control.
VBUSST	58	87	B6	I	ANA	USB OTG Internal Charge Pump Feedback Control.
VBUSVLD	58	87	B6	I	ST	USB Vbus Boost Generator, Comparator Input 1.
VCAP	56	85	B7	P	—	External Filter Capacitor Connection (regulator enabled).
VCMPST1	58	87	B6	I	ST	USB Vbus Boost Generator, Comparator Input 1.
VCMPST2	59	88	A6	I	ST	USB Vbus Boost Generator, Comparator Input 2.
VCPCON	49	76	A11	O	—	USB OTG Vbus PWM/Charge Output.
VDD	10, 26, 38	2, 16, 37, 46, 62	C2, C9, F8, G5, H6, K8, H4, E5	P	—	Positive Supply for Peripheral Digital Logic and I/O Pins.
VMIO	14	23	J2	I	ST	USB Differential Minus Input/Output (external transceiver).
VPIO	13	22	J1	I	ST	USB Differential Plus Input/Output (external transceiver).
VREF-	15	28, 24 ⁽⁴⁾	L2, K1 ⁽⁴⁾	I	ANA	A/D and Comparator Reference Voltage (low) Input.
VREF+	16	29, 25 ⁽⁴⁾	K3, K2 ⁽⁴⁾	I	ANA	A/D and Comparator Reference Voltage (high) Input.
VSS	9, 25, 41	15, 36, 45, 65, 75	B10, F5, F10, G6, G7, H3, D4, D5	P	—	Ground Reference for Logic and I/O Pins.
VSYN	1	96	C3	O	—	Graphics Display Vertical Sync Pulse.
VUSB	35	55	H9	P	—	USB Voltage (3.3V).

Legend: TTL = TTL input buffer
ANA = Analog level input/output

ST = Schmitt Trigger input buffer
I²C™ = I²C/SMBus input buffer

- Note**
- 1: The alternate EPM pins are selected when the $\overline{\text{ALTPMP}}$ (CW3<12>) bit is programmed to '0'.
 - 2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.
 - 3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.
 - 4: The alternate VREF pins selected when the $\overline{\text{ALT VREF}}$ (CW1<5>) bit is programmed to '0'.

TABLE 4-26: ENHANCED PARALLEL MASTER/SLAVE PORT REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON1	0600	PMPEN	—	PSIDL	ADMUX1	ADMUX0	—	MODE1	MODE0	CSF1	CSF0	ALP	ALMODE	—	BUSKEEP	IRQM1	IRQM0	0000
PMCON2	0602	BUSY	—	ERROR	TIMEOUT	AMREQ	CURMST	MSTSEL1	MSTSEL0	RADDR23	RADDR22	RADDR21	RADDR20	RADDR19	RADDR18	RADDR17	RADDR16	0000
PMCON3	0604	PTWREN	PTRDEN	PTBE1EN	PTBE0EN	—	AWAITM1	AWAITM0	AWAITE	—	PTEN22	PTEN21	PTEN20	PTEN19	PTEN18	PTEN17	PTEN16	0000
PMCON4	0606	PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8	PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0	0000
PMCS1CF	0608	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS1BS	060A	BASE23	BASE22	BASE21	BASE20	BASE19	BASE18	BASE17	BASE16	BASE15	—	—	—	BASE11	—	—	—	0200
PMCS1MD	060C	ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMCS2CF	060E	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS2BS	0610	BASE23	BASE22	BASE21	BASE20	BASE19	BASE18	BASE17	BASE16	BASE15	—	—	—	BASE11	—	—	—	0600
PMCS2MD	0612	ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMDOUT1	0614	EPMP Data Out Register 1<15:8>									EPMP Data Out Register 1<7:0>							xxxx
PMDOUT2	0616	EPMP Data Out Register 2<15:8>									EPMP Data Out Register 2<7:0>							xxxx
PMDIN1	0618	EPMP Data In Register 1<15:8>									EPMP Data In Register 1<7:0>							xxxx
PMDIN2	061A	EPMP Data In Register 2<15:8>									EPMP Data In Register 2<7:0>							xxxx
PMSTAT	061C	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Unimplemented in 64-pin devices, read as '0'.

TABLE 4-27: REAL-TIME CLOCK AND CALENDAR REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ALRMVAL	0620	Alarm Value Register Window Based on ALRMPTR<1:0>																xxxx
ALCFGRPT	0622	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	0000
RTCVAL	0624	RTCC Value Register Window Based on RTCPTR<1:0>																xxxx
RCFGCAL	0626	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTR1	RTCPTR0	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	(Note 1)

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The status of the RCFGCAL register on POR is '0000' and on other Resets is unchanged.

TABLE 4-30: PERIPHERAL PIN SELECT REGISTER MAP (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	06C0	—	—	RP1R5	RP1R4	RP1R3	RP1R2	RP1R1	RP1R0	—	—	RP0R5	RP0R4	RP0R3	RP0R2	RP0R1	RP0R0	0000
RPOR1	06C2	—	—	RP3R5	RP3R4	RP3R3	RP3R2	RP3R1	RP3R0	—	—	RP2R5	RP2R4	RP2R3	RP2R2	RP2R1	RP2R0	0000
RPOR2	06C4	—	—	RP5R5 ⁽¹⁾	RP5R4 ⁽¹⁾	RP5R3 ⁽¹⁾	RP5R2 ⁽¹⁾	RP5R1 ⁽¹⁾	RP5R0 ⁽¹⁾	—	—	RP4R5	RP4R4	RP4R3	RP4R2	RP4R1	RP4R0	0000
RPOR3	06C6	—	—	RP7R5	RP7R4	RP7R3	RP7R2	RP7R1	RP7R0	—	—	RP6R5	RP6R4	RP6R3	RP6R2	RP6R1	RP6R0	0000
RPOR4	06C8	—	—	RP9R5	RP9R4	RP9R3	RP9R2	RP9R1	RP9R0	—	—	RP8R5	RP8R4	RP8R3	RP8R2	RP8R1	RP8R0	0000
RPOR5	06CA	—	—	RP11R5	RP11R4	RP11R3	RP11R2	RP11R1	RP11R0	—	—	RP10R5	RP10R4	RP10R3	RP10R2	RP10R1	RP10R0	0000
RPOR6	06CC	—	—	RP13R5	RP13R4	RP13R3	RP13R2	RP13R1	RP13R0	—	—	RP12R5	RP12R4	RP12R3	RP12R2	RP12R1	RP12R0	0000
RPOR7	06CE	—	—	RP15R5 ⁽¹⁾	RP15R4 ⁽¹⁾	RP15R3 ⁽¹⁾	RP15R2 ⁽¹⁾	RP15R1 ⁽¹⁾	RP15R0 ⁽¹⁾	—	—	RP14R5	RP14R4	RP14R3	RP14R2	RP14R1	RP14R0	0000
RPOR8	06D0	—	—	RP17R5	RP17R4	RP17R3	RP17R2	RP17R1	RP17R0	—	—	RP16R5	RP16R4	RP16R3	RP16R2	RP16R1	RP16R0	0000
RPOR9	06D2	—	—	RP19R5	RP19R4	RP19R3	RP19R2	RP19R1	RP19R0	—	—	RP18R5	RP18R4	RP18R3	RP18R2	RP18R1	RP18R0	0000
RPOR10	06D4	—	—	RP21R5	RP21R4	RP21R3	RP21R2	RP21R1	RP21R0	—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0	0000
RPOR11	06D6	—	—	RP23R5	RP23R4	RP23R3	RP23R2	RP23R1	RP23R0	—	—	RP22R5	RP22R4	RP22R3	RP22R2	RP22R1	RP22R0	0000
RPOR12	06D8	—	—	RP25R5	RP25R4	RP25R3	RP25R2	RP25R1	RP25R0	—	—	RP24R5	RP24R4	RP24R3	RP24R2	RP24R1	RP24R0	0000
RPOR13	06DA	—	—	RP27R5	RP27R4	RP27R3	RP27R2	RP27R1	RP27R0	—	—	RP26R5	RP26R4	RP26R3	RP26R2	RP26R1	RP26R0	0000
RPOR14	06DC	—	—	RP29R5	RP29R4	RP29R3	RP29R2	RP29R1	RP29R0	—	—	RP28R5	RP28R4	RP28R3	RP28R2	RP28R1	RP28R0	0000
RPOR15 ⁽¹⁾	06DE	—	—	RP31R5 ⁽¹⁾	RP31R4 ⁽¹⁾	RP31R3 ⁽¹⁾	RP31R2 ⁽¹⁾	RP31R1 ⁽¹⁾	RP31R0 ⁽¹⁾	—	—	RP30R5 ⁽¹⁾	RP30R4 ⁽¹⁾	RP30R3 ⁽¹⁾	RP30R2 ⁽¹⁾	RP30R1 ⁽¹⁾	RP30R0 ⁽¹⁾	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits are unimplemented in 64-pin devices; read as '0'.

4.3.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDH and TBLWTH instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDH and TBLWTH access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDH (Table Read High): In Word mode, it maps the lower word of the program space location ($P<15:0>$) to a data address ($D<15:0>$). In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

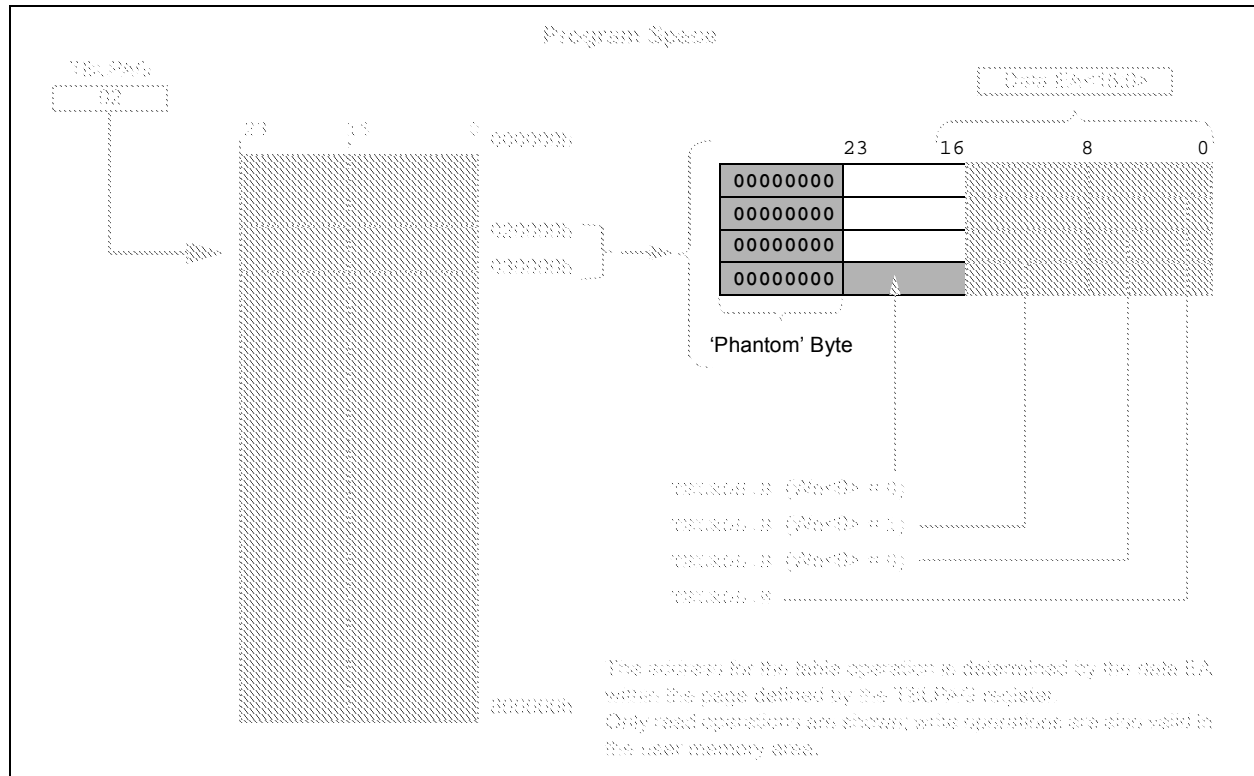
2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address ($P<23:16>$) to a data address. Note that $D<15:8>$, the 'phantom' byte, will always be '0'. In Byte mode, it maps the upper or lower byte of the program word to $D<7:0>$ of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (byte select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are described in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When $TBLPAG<7> = 0$, the table page is located in the user memory space. When $TBLPAG<7> = 1$, the page is located in configuration space.

Note: Only table read operations will execute in the configuration memory space, where Device IDs are located. Table write operations are not allowed.

FIGURE 4-9: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



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REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

R/S-0, HC ⁽¹⁾	R/W-0 ⁽¹⁾	R-0, HSC ⁽¹⁾	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0 ⁽¹⁾	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
—	ERASE	—	—	NVMOP3 ⁽²⁾	NVMOP2 ⁽²⁾	NVMOP1 ⁽²⁾	NVMOP0 ⁽²⁾
bit 7							bit 0

Legend:	S = Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
HC = Hardware Clearable bit		x = Bit is unknown

- bit 15 **WR:** Write Control bit⁽¹⁾
 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
 0 = Program or erase operation is complete and inactive
- bit 14 **WREN:** Write Enable bit⁽¹⁾
 1 = Enable Flash program/erase operations
 0 = Inhibit Flash program/erase operations
- bit 13 **WRERR:** Write Sequence Error Flag bit⁽¹⁾
 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
 0 = The program or erase operation completed normally
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **ERASE:** Erase/Program Enable bit⁽¹⁾
 1 = Perform the erase operation specified by NVMOP<3:0> on the next WR command
 0 = Perform the program operation specified by NVMOP<3:0> on the next WR command
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits^(1,2)
 1111 = Memory bulk erase operation (ERASE = 1) or no operation (ERASE = 0)⁽³⁾
 0011 = Memory word program operation (ERASE = 0) or no operation (ERASE = 1)
 0010 = Memory page erase operation (ERASE = 1) or no operation (ERASE = 0)
 0001 = Memory row program operation (ERASE = 0) or no operation (ERASE = 1)

- Note 1:** These bits can only be reset on POR.
- Note 2:** All other combinations of NVMOP<3:0> are unimplemented.
- Note 3:** Available in ICSP™ mode only; refer to the device programming specification.

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REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

R/W-0, HS	R/W-0, HS	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
TRAPR	IOPUWR	—	—	—	—	CM	VREGS ⁽³⁾
bit 15							bit 8

R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred
- bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or uninitialized W register is used as an Address Pointer and caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred
- bit 13-10 **Unimplemented:** Read as '0'
- bit 9 **CM:** Configuration Word Mismatch Reset Flag bit
1 = A Configuration Word Mismatch Reset has occurred
0 = A Configuration Word Mismatch Reset has not occurred
- bit 8 **VREGS:** Voltage Regulator Standby Enable bit⁽³⁾
1 = Program memory and regulator remain active during Sleep/Idle
0 = Program memory power is removed and regulator goes to standby during Sleep/Idle
- bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred
- bit 6 **SWR:** Software Reset (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed
- bit 5 **SWDTEN:** Software Enable/Disable of WDT bit⁽²⁾
1 = WDT is enabled
0 = WDT is disabled
- bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred
- bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

- Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the SWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.
- 3:** Re-enabling the regulator after it enters Standby mode will add a delay, TVREG, when waking up from Sleep. Applications that do not use the voltage regulator should set this bit to prevent this delay from occurring.

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REGISTER 7-12: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPF1IE	T3IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **AD1IE:** A/D Conversion Complete Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 12 **U1TXIE:** UART1 Transmitter Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 11 **U1RXIE:** UART1 Receiver Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 10 **SPI1IE:** SPI1 Transfer Complete Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 9 **SPF1IE:** SPI1 Fault Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 8 **T3IE:** Timer3 Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 7 **T2IE:** Timer2 Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 6 **OC2IE:** Output Compare Channel 2 Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 5 **IC2IE:** Input Capture Channel 2 Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **T1IE:** Timer1 Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 2 **OC1IE:** Output Compare Channel 1 Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled

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REGISTER 7-13: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1 (CONTINUED)

bit 6	IC7IE: Input Capture Channel 7 Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 5	Unimplemented: Read as '0'
bit 4	INT1IE: External Interrupt 1 Enable bit ⁽¹⁾ 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 3	CNIE: Input Change Notification Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 2	CMIE: Comparator Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 1	MI2C1IE: Master I2C1 Event Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 0	SI2C1IE: Slave I2C1 Event Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled

Note 1: If an external interrupt is enabled, the interrupt input must also be configured to an available RPx or RPlx pin. See **Section 10.4 “Peripheral Pin Select (PPS)”** for more information.

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REGISTER 7-33: IPC15: INTERRUPT PRIORITY CONTROL REGISTER 15

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	RTCIP2	RTCIP1	RTCIP0
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **RTCIP<2:0>:** Real-Time Clock and Calendar Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

.

.

.

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 10-6: ANSF: PORTF ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
—	—	—	—	—	—	—	ANSF0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **ANSF0:** Analog Function Selection bits

1 = Pin is configured in Analog mode; I/O port read is disabled

0 = Pin is configured in Digital mode; I/O port read is enabled

REGISTER 10-7: ANSG: PORTG ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1
—	—	—	—	—	—	ANSG9	ANSG8
bit 15							bit 8

R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
ANSG7	ANSG6	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-6 **ANSG<9:6>:** Analog Function Selection bits

1 = Pin is configured in Analog mode; I/O port read is disabled

0 = Pin is configured in Digital mode; I/O port read is enabled

bit 5-0 **Unimplemented:** Read as '0'

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REGISTER 10-39: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP21R5	RP21R4	RP21R3	RP21R2	RP21R1	RP21R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP21R<5:0>:** RP21 Output Pin Mapping bits
Peripheral output number n is assigned to pin, RP21 (see Table 10-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP20R<5:0>:** RP20 Output Pin Mapping bits
Peripheral output number n is assigned to pin, RP20 (see Table 10-4 for peripheral function numbers).

REGISTER 10-40: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP23R5	RP23R4	RP23R3	RP23R2	RP23R1	RP23R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP22R5	RP22R4	RP22R3	RP22R2	RP22R1	RP22R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP23R<5:0>:** RP23 Output Pin Mapping bits
Peripheral output number n is assigned to pin, RP23 (see Table 10-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP22R<5:0>:** RP22 Output Pin Mapping bits
Peripheral output number n is assigned to pin, RP22 (see Table 10-4 for peripheral function numbers).

14.0 OUTPUT COMPARE WITH DEDICATED TIMERS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “PIC24F Family Reference Manual”, **Section 35. “Output Compare with Dedicated Timer”** (DS39723). The information in this data sheet supersedes the information in the FRM.

Devices in the PIC24FJ256DA210 family feature all of the 9 independent output compare modules. Each of these modules offers a wide range of configuration and operating options for generating pulse trains on internal device events, and can produce pulse-width modulated waveforms for driving power applications.

Key features of the output compare module include:

- Hardware configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 31 user-selectable trigger/sync sources available
- Two separate period registers (a main register, OCxR, and a secondary register, OCxRS) for greater flexibility in generating pulses of varying widths
- Configurable for single pulse or continuous pulse generation on an output event, or continuous PWM waveform generation
- Up to 6 clock sources available for each module, driving a separate internal 16-bit counter

14.1 General Operating Modes

14.1.1 SYNCHRONOUS AND TRIGGER MODES

When the output compare module operates in a free-running mode, the internal 16-bit counter, OCxTMR, runs counts up continuously, wrapping around from 0xFFFF to 0x0000 on each overflow, with its period synchronized to the selected external clock source. Compare or PWM events are generated each time a match between the internal counter and one of the period registers occurs.

In Synchronous mode, the module begins performing its compare or PWM operation as soon as its selected clock source is enabled. Whenever an event occurs on the selected sync source, the module's internal counter is reset. In Trigger mode, the module waits for a sync event from another internal module to occur before allowing the counter to run.

Free-running mode is selected by default or any time that the SYNCSEL bits (OCxCON2<4:0>) are set to '00000'. Synchronous or Trigger modes are selected any time the SYNCSEL bits are set to any value except '00000'. The OCTRIG bit (OCxCON2<7>) selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSEL bits determine the sync/trigger source.

14.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own set of 16-bit timer and duty cycle registers. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, Modules 1 and 2 are paired, as are Modules 3 and 4, and so on.) The odd numbered module (OCx) provides the Least Significant 16 bits of the 32-bit register pairs and the even module (OCy) provides the Most Significant 16 bits. Wrap-arounds of the OCx registers cause an increment of their corresponding OCy registers.

Cascaded operation is configured in hardware by setting the OC32 bit (OCxCON2<8>) for both modules. For more details on cascading, refer to the “PIC24F Family Reference Manual”, **Section 35. “Output Compare with Dedicated Timer”**.

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18.5.3 SEND A FULL-SPEED BULK DATA TRANSFER TO A TARGET DEVICE

1. Follow the procedure described in **Section 18.5.1 “Enable Host Mode and Discover a Connected Device”** and **Section 18.5.2 “Complete a Control Transaction to a Connected Device”** to discover and configure a device.
2. To enable transmit and receive transfers with handshaking enabled, write 1Dh to U1EP0. If the target device is a low-speed device, also set the LSPD (U1EP0<7>) bit. If you want the hardware to automatically retry indefinitely if the target device asserts a NAK on the transfer, clear the Retry Disable bit, RETRYDIS (U1EP0<6>).
3. Set up the BD for the current (even or odd) TX EP0 to transfer up to 64 bytes.
4. Set the USB device address of the target device in the address register (U1ADDR<6:0>).
5. Write an OUT token to the desired endpoint to U1TOK. This triggers the module's transmit state machines to begin transmitting the token and the data.
6. Wait for the Transfer Done Interrupt Flag, TRNIF. This indicates that the BD has been released back to the microprocessor and the transfer has completed. If the retry disable bit is set, the handshake (ACK, NAK, STALL or ERROR (0Fh)) is returned in the BD PID field. If a STALL interrupt occurs, the pending packet must be dequeued and the error condition in the target device cleared. If a detach interrupt occurs (SE0 for more than 2.5 μ s), then the target has detached (U1IR<0> is set).
7. Once the transfer done interrupt occurs (TRNIF is set), the BD can be examined and the next data packet queued by returning to step 2.

Note: USB speed, transceiver and pull-ups should only be configured during the module setup phase. It is not recommended to change these settings while the module is enabled.

18.6 OTG Operation

18.6.1 SESSION REQUEST PROTOCOL (SRP)

An OTG A-device may decide to power down the VBUS supply when it is not using the USB link through the Session Request Protocol (SRP). Software may do this by clearing VBUSON (U1OTGCON<3>). When the VBUS supply is powered down, the A-device is said to have ended a USB session.

An OTG A-device or embedded host may repower the VBUS supply at any time (initiate a new session). An OTG B-device may also request that the OTG A-device repower the VBUS supply (initiate a new session). This is accomplished via Session Request Protocol (SRP).

Prior to requesting a new session, the B-device must first check that the previous session has definitely ended. To do this, the B-device must check for two conditions:

1. VBUS supply is below the session valid voltage, and
2. Both D+ and D- have been low for at least 2 ms.

The B-device will be notified of Condition 1 by the SESENDIF (U1OTGIR<2>) interrupt. Software will have to manually check for Condition 2.

Note: When the A-device powers down the VBUS supply, the B-device must disconnect its pull-up resistor from power. If the device is self-powered, it can do this by clearing DPPULUP (U1OTGCON<7>) and DMPULUP (U1OTGCON<6>).

The B-device may aid in achieving Condition 1 by discharging the VBUS supply through a resistor. Software may do this by setting VBUSDIS (U1OTGCON<0>).

After these initial conditions are met, the B-device may begin requesting the new session. The B-device begins by pulsing the D+ data line. Software should do this by setting DPPULUP (U1OTGCON<7>). The data line should be held high for 5 to 10 ms.

The B-device then proceeds by pulsing the VBUS supply. Software should do this by setting PUVBUS (U1CNFG2<4>). When an A-device detects SRP signaling (either via the ATTACHIF (U1IR<6>) interrupt or via the SESVDIF (U1OTGIR<3>) interrupt), the A-device must restore the VBUS supply by either setting VBUSON (U1OTGCON<3>) or by setting the I/O port controlling the external power source.

The B-device should not monitor the state of the VBUS supply while performing VBUS supply pulsing. When the B-device does detect that the VBUS supply has been restored (via the SESVDIF (U1OTGIR<3>) interrupt), the B-device must reconnect to the USB link by pulling up D+ or D- (via the DPPULUP or DMPULUP).

The A-device must complete the SRP by driving USB Reset signaling.

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REGISTER 18-13: U1CNFG2: USB CONFIGURATION REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	UVCMPSEL	PUVBUS	EXTI2CEN	UVBUSDIS ⁽¹⁾	UVCMPDIS ⁽¹⁾	UTRDIS ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **UVCMPSEL:** VBUS Comparator External Interface Selection bit
 1 = Use VBUSVLD, SESSVLD and SESSEND as comparator interface pins
 0 = Use VCMPS1 and VCMPS2 as comparator interface pins

bit 4 **PUVBUS:** VBUS Pull-Up Enable bit
 1 = Pull-up on VBUS pin is enabled
 0 = Pull-up on VBUS pin is disabled

bit 3 **EXTI2CEN:** I²C™ Interface For External Module Control Enable bit
 1 = External module(s) is controlled via the I²C™ interface
 0 = External module(s) controlled via the dedicated pins

bit 2 **UVBUSDIS:** On-Chip 5V Boost Regulator Builder Disable bit⁽¹⁾
 1 = On-chip boost regulator builder is disabled; digital output control interface is enabled
 0 = On-chip boost regulator builder is active

bit 1 **UVCMPDIS:** On-Chip VBUS Comparator Disable bit⁽¹⁾
 1 = On-chip charge VBUS comparator is disabled; digital input status interface is enabled
 0 = On-chip charge VBUS comparator is active

bit 0 **UTRDIS:** On-Chip Transceiver Disable bit⁽¹⁾
 1 = On-chip transceiver is disabled; digital transceiver interface is enabled
 0 = On-chip transceiver is active

Note 1: Never change these bits while the USBPWR bit is set (U1PWRC<0> = 1).

22.0 GRAPHICS CONTROLLER MODULE (GFX)

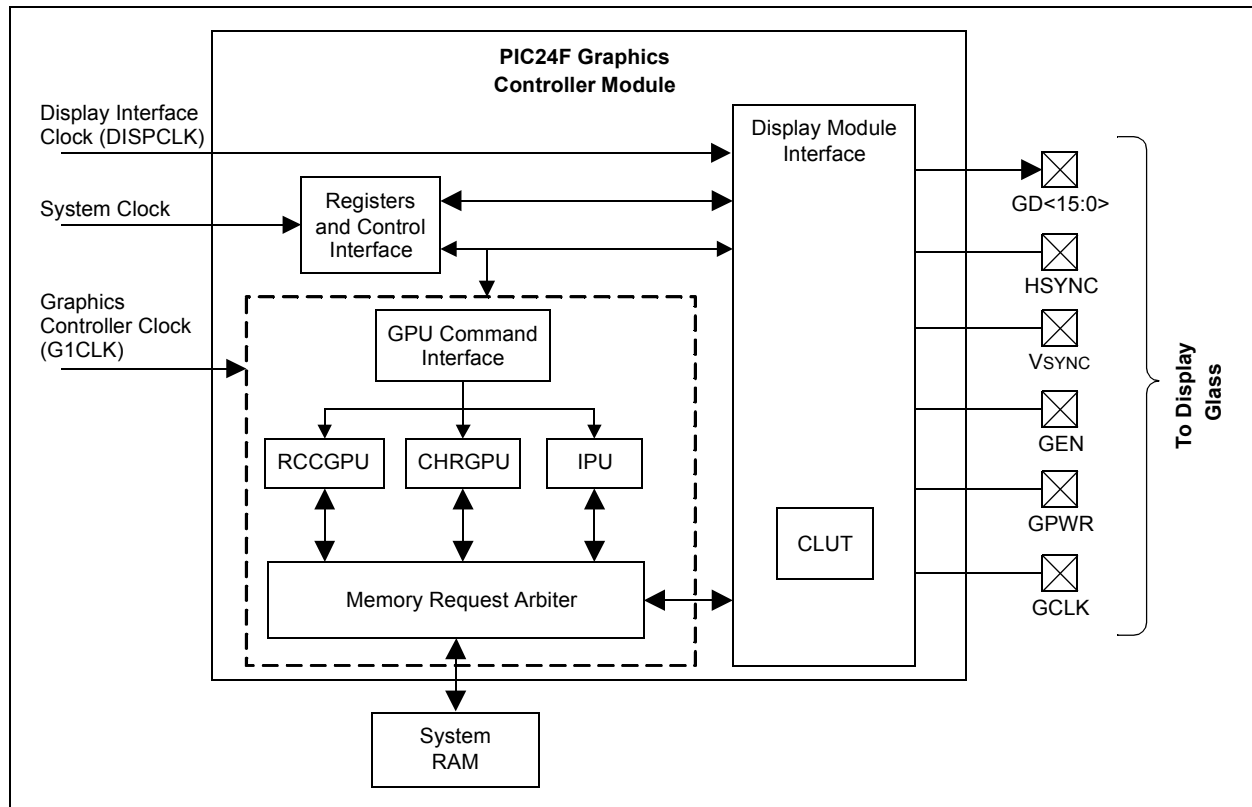
Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “PIC24F Family Reference Manual”, **Section 43. “Graphics Controller Module (GFX)”** (DS39731). The information in this data sheet supersedes the information in the FRM.

The Graphics Controller (GFX) module is specifically designed to directly interface with the display glasses, with a built-in analog drive, to individually control pixels in the screen. The module also provides an accelerated rendering of vertical and horizontal lines, rectangles, copying of rectangular area between different locations on the screen, drawing texts and decompressing packed data. The use of the accelerated rendering is performed using command registers. Once initiated, the hardware will perform the rendering, and the software can either poll the status, or use the interrupts to continue rendering of the succeeding shapes.

Key features of the GFX module include:

- Direct interface to three categories of display glasses:
 - Monochrome STN
 - Color STN
 - Color TFT
- Programmable vertical and horizontal synchronization signals' timing and display clock frequency to meet display's frame rates
- Optional internal or external display buffer to accommodate different types of display resolution
- Graphic hardware accelerators:
 - Character Graphics Processing Unit (CHRGPU)
 - Rectangle Copy Graphics Processing Unit (RCCGPU)
 - Inflate Processing Unit (IPU)
- 256 Entries Color Look-up Table (CLUT)
- Supports 1/2/4/8/16 bits-per-pixel (bpp) color depth
- Programmable display resolution
- Supports multiple display interfaces:
 - 4/8/16-bit Monochrome STN
 - 4/8/16-bit Color STN
 - 9/12/18/24-bit color TFT (18 and 24-bit displays are connected as 16-bit 5-6-5 RGB color format)

FIGURE 22-1: GRAPHICS MODULE OVERVIEW



23.0 10-BIT HIGH-SPEED A/D CONVERTER

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “PIC24F Family Reference Manual”, **Section 17. “10-Bit A/D Converter”** (DS39705). The information in this data sheet supersedes the information in the FRM.

The 10-bit A/D Converter has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 500 ksp/s
- 24 analog input pins (PIC24FJXXDAX10 devices) and 16 analog input pins (PIC24FJXXDAX06 devices)
- External voltage reference input pins
- Internal band gap reference inputs
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 32-word conversion result buffer
- Selectable Buffer Fill modes
- Four result alignment options
- Operation during CPU Sleep and Idle modes

On all PIC24FJ256DA210 family devices, the 10-bit A/D Converter has 24 analog input pins, designated AN0 through AN23. In addition, there are two analog input pins for external voltage reference connections (VREF+ and VREF-). These voltage reference inputs may be shared with other analog input pins.

A block diagram of the A/D Converter is shown in Figure 23-1.

To perform an A/D conversion:

1. Configure the A/D module:
 - a) Configure the port pins as analog inputs and/or select band gap reference inputs (ANCFG registers).
 - b) Select the voltage reference source to match the expected range on analog inputs (AD1CON2<15:13>).
 - c) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
 - d) Select the appropriate sample/conversion sequence (AD1CON1<7:5> and AD1CON3<12:8>).
 - e) Select how the conversion results are presented in the buffer (AD1CON1<9:8>).
 - f) Select the interrupt rate (AD1CON2<6:2>).
 - g) Turn on the A/D module (AD1CON1<15>).
2. Configure the A/D interrupt (if required):
 - a) Clear the AD1IF bit.
 - b) Select the A/D interrupt priority.

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REGISTER 27-6: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23				bit 16			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R	R	R	R
—	—	—	—	REV3	REV2	REV1	REV0
bit 7				bit 0			

Legend: R = Readable bit	U = Unimplemented bit
---------------------------------	-----------------------

bit 23-4 **Unimplemented:** Read as '0'
bit 3-0 **REV<3:0>:** Device revision identifier bits

27.2 On-Chip Voltage Regulator

All PIC24FJ256DA210 family devices power their core digital logic at a nominal 1.8V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the PIC24FJ256DA210 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator is controlled by the ENVREG pin. Tying VDD to the pin enables the regulator, which in turn, provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR capacitor (such as ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor (CEFC) is provided in **Section 30.1 “DC Characteristics”**.

27.2.1 VOLTAGE REGULATOR LOW-VOLTAGE DETECTION

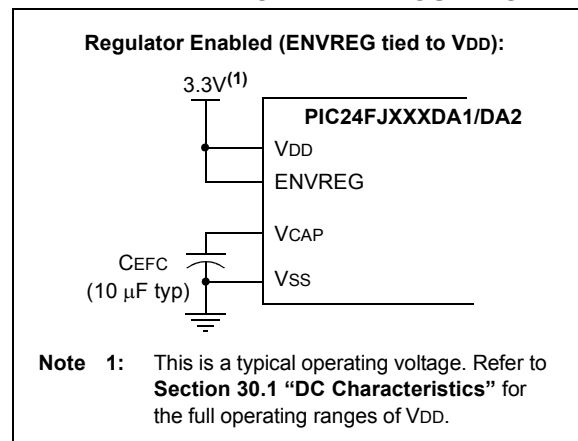
When the on-chip regulator is enabled, it provides a constant voltage of 1.8V nominal to the digital core logic.

The regulator can provide this level from a VDD of about 2.1V, all the way up to the device's VDDMAX. It does not have the capability to boost VDD levels. In order to prevent “brown-out” conditions when the voltage drops too low for the regulator, the Brown-out Reset occurs. Then the regulator output follows VDD with a typical voltage drop of 300 mV.

To provide information about when the regulator voltage starts reducing, the on-chip regulator includes a simple Low-Voltage Detect circuit, which sets the

Low-Voltage Detect Interrupt Flag, LVDIF (IFS4<8>). This can be used to generate an interrupt to trigger an orderly shutdown.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



27.2.2 ON-CHIP REGULATOR AND POR

When the voltage regulator is enabled, it takes approximately 10 µs for it to generate output. During this time, designated as TVREG, code execution is disabled. TVREG is applied every time the device resumes operation after any power-down, including Sleep mode. TVREG is determined by the status of the VREGS bit (RCON<8>) and the WUTSEL Configuration bits (CW3<11:10>). Refer to **Section 30.0 “Electrical Characteristics”** for more information on TVREG.

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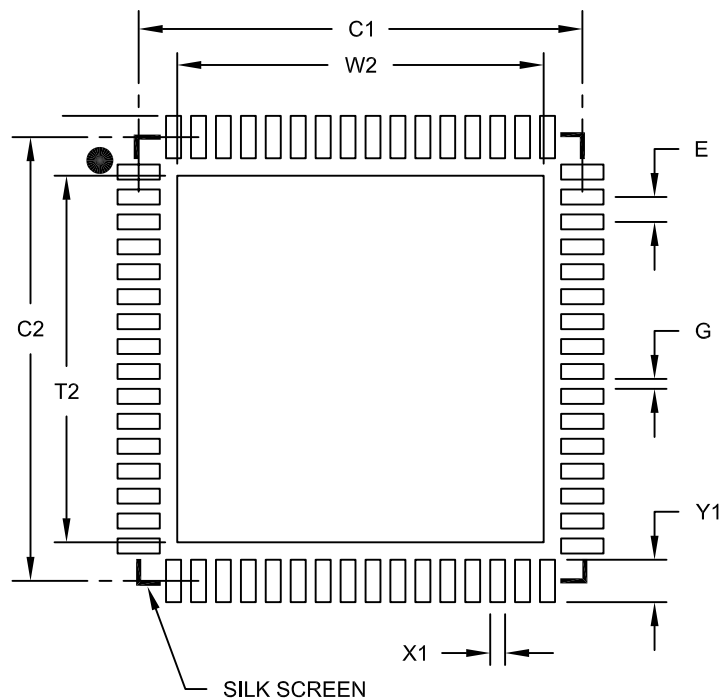
TABLE 29-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
bit4	4-bit Bit Selection field (used in word addressed instructions) $\in \{0...15\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address $\in \{0000h...1FFFh\}$
lit1	1-bit unsigned literal $\in \{0,1\}$
lit4	4-bit unsigned literal $\in \{0...15\}$
lit5	5-bit unsigned literal $\in \{0...31\}$
lit8	8-bit unsigned literal $\in \{0...255\}$
lit10	10-bit unsigned literal $\in \{0...255\}$ for Byte mode, $\{0:1023\}$ for Word mode
lit14	14-bit unsigned literal $\in \{0...16383\}$
lit16	16-bit unsigned literal $\in \{0...65535\}$
lit23	23-bit unsigned literal $\in \{0...8388607\}$; LSB must be '0'
None	Field does not require an entry, may be blank
PC	Program Counter
Slit10	10-bit signed literal $\in \{-512...511\}$
Slit16	16-bit signed literal $\in \{-32768...32767\}$
Slit6	6-bit signed literal $\in \{-16...16\}$
Wb	Base W register $\in \{W0..W15\}$
Wd	Destination W register $\in \{Wd, [Wd], [Wd++] , [Wd--], [++Wd], [--Wd] \}$
Wdo	Destination W register $\in \{Wnd, [Wnd], [Wnd++] , [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] \}$
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wn	One of 16 working registers $\in \{W0..W15\}$
Wnd	One of 16 destination working registers $\in \{W0..W15\}$
Wns	One of 16 source working registers $\in \{W0..W15\}$
WREG	W0 (working register used in file register instructions)
Ws	Source W register $\in \{Ws, [Ws], [Ws++] , [Ws--], [++Ws], [--Ws] \}$
Wso	Source W register $\in \{Wns, [Wns], [Wns++] , [Wns--], [++Wns], [--Wns], [Wns+Wb] \}$

PIC24FJ256DA210 FAMILY

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A