



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, GFX, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256da106t-i-mr

PIC24FJ256DA210 FAMILY

TABLE 1-3: PIC24FJ256DA210 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
RD0	46	72	D9	I/O	ST	PORTD Digital I/O.
RD1	49	76	A11	I/O	ST	
RD2	50	77	A10	I/O	ST	
RD3	51	78	B9	I/O	ST	
RD4	52	81	C8	I/O	ST	
RD5	53	82	B8	I/O	ST	
RD6	54	83	D7	I/O	ST	
RD7	55	84	C7	I/O	ST	
RD8	42	68	E9	I/O	ST	
RD9	43	69	E10	I/O	ST	
RD10	44	70	D11	I/O	ST	
RD11	45	71	C11	I/O	ST	
RD12	—	79	A9	I/O	ST	
RD13	—	80	D8	I/O	ST	
RD14	—	47	L9	I/O	ST	
RD15	—	48	K9	I/O	ST	
RE0	60	93	A4	I/O	ST	PORTE Digital I/O.
RE1	61	94	B4	I/O	ST	
RE2	62	98	B3	I/O	ST	
RE3	63	99	A2	I/O	ST	
RE4	64	100	A1	I/O	ST	
RE5	1	3	D3	I/O	ST	
RE6	2	4	C1	I/O	ST	
RE7	3	5	D2	I/O	ST	
RE8	—	18	G1	I/O	ST	
RE9	—	19	G2	I/O	ST	
REFO	30	44	L8	O	—	Reference Clock Output.
RF0	58	87	B6	I/O	ST	PORTF Digital I/O.
RF1	59	88	A6	I/O	ST	
RF2	—	52	K11	I/O	ST	
RF3	33	51	K10	I/O	ST	
RF4	31	49	L10	I/O	ST	
RF5	32	50	L11	I/O	ST	
RF7	34	54	H8	I/O	ST	
RF8	—	53	J10	I/O	ST	
RF12	—	40	K6	I/O	ST	
RF13	—	39	L6	I/O	ST	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I²C™ = I²C/SMBus input buffer

- Note** 1: The alternate EPMP pins are selected when the ALTPMP (CW3<12>) bit is programmed to '0'.
- 2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.
- 3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.
- 4: The alternate VREF pins selected when the ALTVREF (CW1<5>) bit is programmed to '0'.

TABLE 4-9: OUTPUT COMPARE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0190	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC1CON2	0192	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC1RS	0194	Output Compare 1 Secondary Register																0000
OC1R	0196	Output Compare 1 Register																0000
OC1TMR	0198	Output Compare 1 Timer Value Register																xxxx
OC2CON1	019A	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC2CON2	019C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC2RS	019E	Output Compare 2 Secondary Register																0000
OC2R	01A0	Output Compare 2 Register																0000
OC2TMR	01A2	Output Compare 2 Timer Value Register																xxxx
OC3CON1	01A4	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC3CON2	01A6	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC3RS	01A8	Output Compare 3 Secondary Register																0000
OC3R	01AA	Output Compare 3 Register																0000
OC3TMR	01AC	Output Compare 3 Timer Value Register																xxxx
OC4CON1	01AE	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC4CON2	01B0	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC4RS	01B2	Output Compare 4 Secondary Register																0000
OC4R	01B4	Output Compare 4 Register																0000
OC4TMR	01B6	Output Compare 4 Timer Value Register																xxxx
OC5CON1	01B8	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC5CON2	01BA	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC5RS	01BC	Output Compare 5 Secondary Register																0000
OC5R	01BE	Output Compare 5 Register																0000
OC5TMR	01C0	Output Compare 5 Timer Value Register																xxxx
OC6CON1	01C2	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC6CON2	01C4	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC6RS	01C6	Output Compare 6 Secondary Register																0000
OC6R	01C8	Output Compare 6 Register																0000
OC6TMR	01CA	Output Compare 6 Timer Value Register																xxxx
OC7CON1	01CC	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC7CON2	01CE	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC7RS	01D0	Output Compare 7 Secondary Register																0000
OC7R	01D2	Output Compare 7 Register																0000
OC7TMR	01D4	Output Compare 7 Timer Value Register																xxxx

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: UART REGISTER MAPS

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	UART1 Baud Rate Generator Prescaler Register																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	UART2 Baud Rate Generator Prescaler Register																0000
U3MODE	0250	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U3STA	0252	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U3TXREG	0254	—	—	—	—	—	—	—	UART3 Transmit Register									xxxx
U3RXREG	0256	—	—	—	—	—	—	—	UART3 Receive Register									0000
U3BRG	0258	UART3 Baud Rate Generator Prescaler Register																0000
U4MODE	02B0	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U4STA	02B2	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U4TXREG	02B4	—	—	—	—	—	—	—	UART4 Transmit Register									xxxx
U4RXREG	02B6	—	—	—	—	—	—	—	UART4 Receive Register									0000
U4BRG	02B8	UART4 Baud Rate Generator Prescaler Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-21: ADC REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADC1BUF0	0300	ADC Data Buffer 0																	xxxx
ADC1BUF1	0302	ADC Data Buffer 1																	xxxx
ADC1BUF2	0304	ADC Data Buffer 2																	xxxx
ADC1BUF3	0306	ADC Data Buffer 3																	xxxx
ADC1BUF4	0308	ADC Data Buffer 4																	xxxx
ADC1BUF5	030A	ADC Data Buffer 5																	xxxx
ADC1BUF6	030C	ADC Data Buffer 6																	xxxx
ADC1BUF7	030E	ADC Data Buffer 7																	xxxx
ADC1BUF8	0310	ADC Data Buffer 8																	xxxx
ADC1BUF9	0312	ADC Data Buffer 9																	xxxx
ADC1BUFA	0314	ADC Data Buffer 10																	xxxx
ADC1BUFB	0316	ADC Data Buffer 11																	xxxx
ADC1BUFC	0318	ADC Data Buffer 12																	xxxx
ADC1BUFD	031A	ADC Data Buffer 13																	xxxx
ADC1BUFE	031C	ADC Data Buffer 14																	xxxx
ADC1BUFF	031E	ADC Data Buffer 15																	xxxx
ADC1BUF10	0340	ADC Data Buffer 16																	xxxx
ADC1BUF11	0342	ADC Data Buffer 17																	xxxx
ADC1BUF12	0344	ADC Data Buffer 18																	xxxx
ADC1BUF13	0346	ADC Data Buffer 19																	xxxx
ADC1BUF14	0348	ADC Data Buffer 20																	xxxx
ADC1BUF15	034A	ADC Data Buffer21																	xxxx
ADC1BUF16	034C	ADC Data Buffer 22																	xxxx
ADC1BUF17	034E	ADC Data Buffer 23																	xxxx
ADC1BUF18	0350	ADC Data Buffer 24																	xxxx
ADC1BUF19	0352	ADC Data Buffer 25																	xxxx
ADC1BUF1A	0354	ADC Data Buffer 26																	xxxx
ADC1BUF1B	0356	ADC Data Buffer 27																	xxxx
ADC1BUF1C	0358	ADC Data Buffer 28																	xxxx
ADC1BUF1D	035A	ADC Data Buffer 29																	xxxx
ADC1BUF1E	035C	ADC Data Buffer 30																	xxxx
ADC1BUF1F	035E	ADC Data Buffer 31																	xxxx

Legend: — = unimplemented, read as '0', r = reserved, maintain as '0'. Reset values are shown in hexadecimal.

Note 1: Unimplemented in 64-pin devices, read as '0'

PIC24FJ256DA210 FAMILY

4.2.5 EXTENDED DATA SPACE (EDS)

The enhancement of the data space in PIC24FJ256DA210 family devices has been accomplished by a new technique, called the Extended Data Space (EDS).

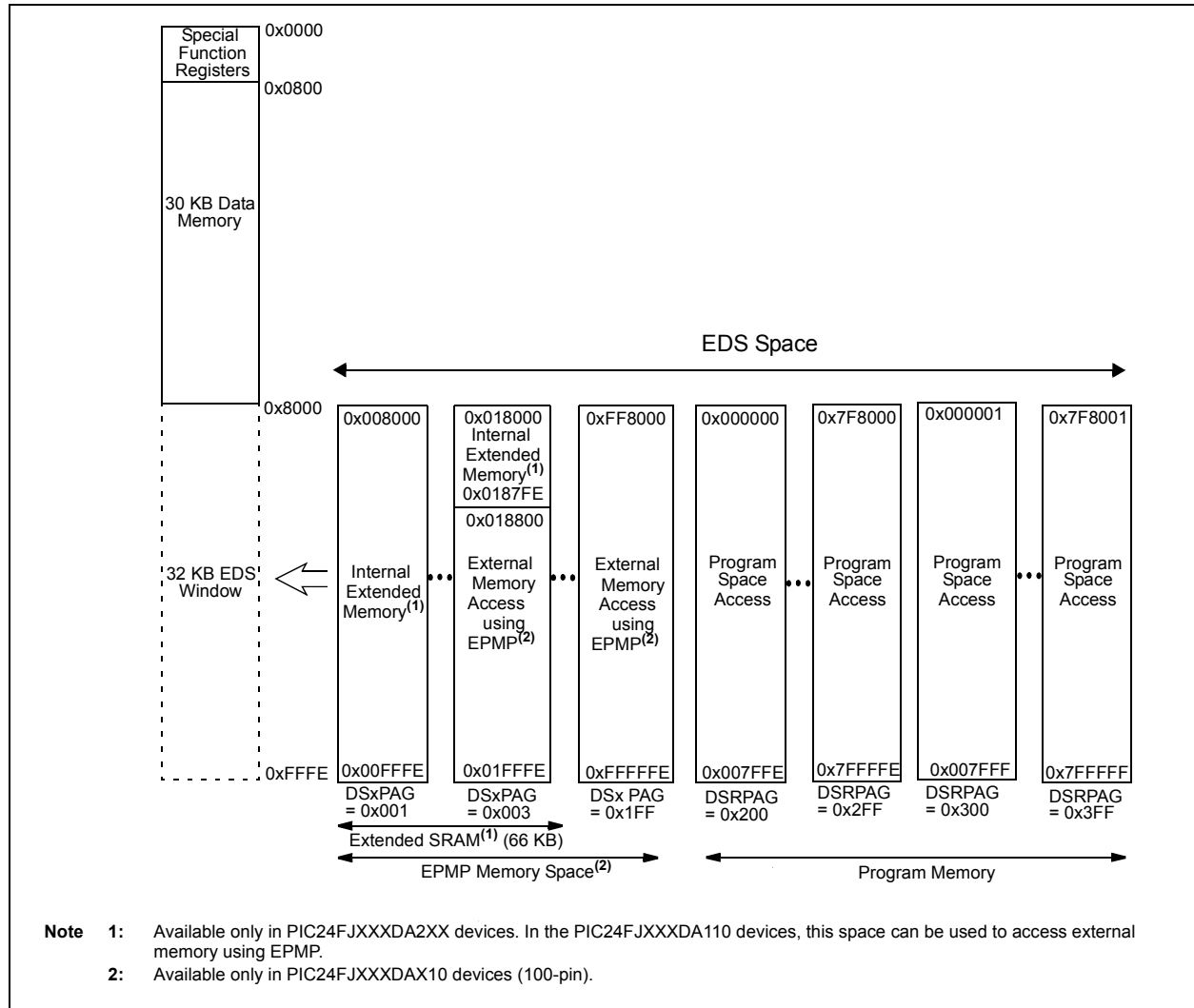
The EDS includes any additional internal extended data memory not accessible by the lower 32 Kbytes data address space, any external memory through EPMP and the Program Space Visibility (PSV).

The extended data space is always accessed through the EDS window, the upper half of data space. The entire extended data space is organized into EDS

pages, each having 32 Kbytes of data. Mapping of the EDS page into the EDS window is done using the Data Space Read register (DSRPAG<9:0>) for read operations and Data Space Write register (DSWPAG<8:0>) for write operations. Figure 4-4 displays the entire EDS space.

Note: Accessing Page 0 in the EDS window will generate an address error trap as Page 0 is the base data memory (data locations, 0x0800 to 0x7FFF, in the lower data space).

FIGURE 4-4: EXTENDED DATA SPACE



PIC24FJ256DA210 FAMILY

EXAMPLE 4-3: EDS READ CODE FROM PROGRAM MEMORY IN ASSEMBLY

```
; Set the EDS page from where the data to be read
mov    #0x0202 , w0
mov    w0 , DSRPAG           ;page 0x202, consisting lower words, is selected for read
mov    #0x000A , w1         ;select the location (0x0A) to be read
bset   w1 , #15             ;set the MSB of the base address, enable EDS mode

;Read a byte from the selected location
mov.b  [w1++] , w2          ;read Low byte
mov.b  [w1++] , w3          ;read High byte

;Read a word from the selected location
mov    [w1] , w2            ;

;Read Double - word from the selected location
mov.d  [w1] , w2            ;two word read, stored in w2 and w3
```

PIC24FJ256DA210 FAMILY

REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)

bit 5	Unimplemented: Read as '0'
bit 4	INT1IF: External Interrupt 1 Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 3	CNIF: Input Change Notification Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 2	CMIF: Comparator Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 1	M12C1IF: Master I2C1 Event Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 0	S12C1IF: Slave I2C1 Event Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred

REGISTER 7-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2

U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
—	—	PMPIF ⁽¹⁾	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF
bit 15							bit 8

R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS
IC5IF	IC4IF	IC3IF	—	—	—	SPI2IF	SPF2IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	PMPIF: Parallel Master Port Interrupt Flag Status bit ⁽¹⁾ 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 12	OC8IF: Output Compare Channel 8 Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 11	OC7IF: Output Compare Channel 7 Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 10	OC6IF: Output Compare Channel 6 Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 9	OC5IF: Output Compare Channel 5 Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred

Note 1: Not available in PIC24FJXXDAX06 devices.

PIC24FJ256DA210 FAMILY

REGISTER 10-6: ANSF: PORTF ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
—	—	—	—	—	—	—	ANSF0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **ANSF0:** Analog Function Selection bits

1 = Pin is configured in Analog mode; I/O port read is disabled

0 = Pin is configured in Digital mode; I/O port read is enabled

REGISTER 10-7: ANSG: PORTG ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1
—	—	—	—	—	—	ANSG9	ANSG8
bit 15							bit 8

R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
ANSG7	ANSG6	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-6 **ANSG<9:6>:** Analog Function Selection bits

1 = Pin is configured in Analog mode; I/O port read is disabled

0 = Pin is configured in Digital mode; I/O port read is enabled

bit 5-0 **Unimplemented:** Read as '0'

PIC24FJ256DA210 FAMILY

REGISTER 10-10: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT4R5	INT4R4	INT4R3	INT4R2	INT4R1	INT4R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **INT4R<5:0>:** Assign External Interrupt 4 (INT4) to Corresponding RPn or RPIIn Pin bits

REGISTER 10-11: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **T3CKR<5:0>:** Assign Timer3 External Clock (T3CK) to Corresponding RPn or RPIIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **T2CKR<5:0>:** Assign Timer2 External Clock (T2CK) to Corresponding RPn or RPIIn Pin bits

PIC24FJ256DA210 FAMILY

REGISTER 17-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0 HC	R/W-0	R-0, HSC	R-1, HSC
UTXISEL1	UTXINV ⁽¹⁾	UTXISEL0	—	UTXBRK	UTXEN ⁽²⁾	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC
URXISEL1	URXISEL0	ADDEN	RIDL	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
HS = Hardware Settable bit	HC = Hardware Clearable bit	x = Bit is unknown

- bit 15,13 **UTXISEL<1:0>**: Transmission Interrupt Mode Selection bits
 11 = Reserved; do not use
 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 **UTXINV**: IrDA[®] Encoder Transmit Polarity Inversion bit⁽¹⁾
IREN = 0:
 1 = UxTX is Idle '0'
 0 = UxTX is Idle '1'
IREN = 1:
 1 = UxTX is Idle '1'
 0 = UxTX is Idle '0'
- bit 12 **Unimplemented**: Read as '0'
- bit 11 **UTXBRK**: Transmit Break bit
 1 = Send Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 0 = Sync Break transmission is disabled or completed
- bit 10 **UTXEN**: Transmit Enable bit⁽²⁾
 1 = Transmit is enabled, UxTX pin controlled by UARTx
 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by port.
- bit 9 **UTXBF**: Transmit Buffer Full Status bit (read-only)
 1 = Transmit buffer is full
 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT**: Transmit Shift Register Empty bit (read-only)
 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

- Note 1:** Value of bit only affects the transmit properties of the module when the IrDA[®] encoder is enabled (IREN = 1).
- Note 2:** If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPN/RPIN pin. See **Section 10.4 “Peripheral Pin Select (PPS)”** for more information.

18.0 UNIVERSAL SERIAL BUS WITH ON-THE-GO SUPPORT (USB OTG)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **Section 27. "USB On-The-Go (OTG)"** (DS39721). The information in this data sheet supersedes the information in the FRM.

PIC24FJ256DA210 family devices contain a full-speed and low-speed compatible, On-The-Go (OTG) USB Serial Interface Engine (SIE). The OTG capability allows the device to act either as a USB peripheral device or as a USB embedded host with limited host capabilities. The OTG capability allows the device to dynamically switch from device to host operation using OTG's Host Negotiation Protocol (HNP).

For more details on OTG operation, refer to the *"On-The-Go Supplement to the USB 2.0 Specification"*, published by the USB-IF. For more details on USB operation, refer to the *"Universal Serial Bus Specification"*, v2.0.

The USB OTG module offers these features:

- USB functionality in Device and Host modes, and OTG capabilities for application-controlled mode switching
- Software-selectable module speeds of full speed (12 Mbps) or low speed (1.5 Mbps, available in Host mode only)
- Support for all four USB transfer types: control, interrupt, bulk and isochronous
- 16 bidirectional endpoints for a total of 32 unique endpoints
- DMA interface for data RAM access
- Queues up to sixteen unique endpoint transfers without servicing
- Integrated, on-chip USB transceiver with support for off-chip transceivers via a digital interface
- Integrated VBUS generation with on-chip comparators and boost generation, and support of external VBUS comparators and regulators through a digital interface
- Configurations for on-chip bus pull-up and pull-down resistors

A simplified block diagram of the USB OTG module is shown in Figure 18-1.

The USB OTG module can function as a USB peripheral device or as a USB host, and may dynamically switch between Device and Host modes under software control. In either mode, the same data paths and Buffer Descriptors (BDs) are used for the transmission and reception of data.

In discussing USB operation, this section will use a controller-centric nomenclature for describing the direction of the data transfer between the microcontroller and the USB. RX (Receive) will be used to describe transfers that move data from the USB to the microcontroller and TX (Transmit) will be used to describe transfers that move data from the microcontroller to the USB. Table 18-1 shows the relationship between data direction in this nomenclature and the USB tokens exchanged.

TABLE 18-1: CONTROLLER-CENTRIC DATA DIRECTION FOR USB HOST OR TARGET

USB Mode	Direction	
	RX	TX
Device	OUT or SETUP	IN
Host	IN	OUT or SETUP

This chapter presents the most basic operations needed to implement USB OTG functionality in an application. A complete and detailed discussion of the USB protocol and its OTG supplement are beyond the scope of this data sheet. It is assumed that the user already has a basic understanding of USB architecture and the latest version of the protocol.

Not all steps for proper USB operation (such as device enumeration) are presented here. It is recommended that application developers use an appropriate device driver to implement all of the necessary features. Microchip provides a number of application-specific resources, such as USB firmware and driver support. Refer to www.microchip.com/usb for the latest firmware and driver support.

PIC24FJ256DA210 FAMILY

18.6.2 HOST NEGOTIATION PROTOCOL (HNP)

In USB OTG applications, a Dual Role Device (DRD) is a device that is capable of being either a host or a peripheral. Any OTG DRD must support Host Negotiation Protocol (HNP).

HNP allows an OTG B-device to temporarily become the USB host. The A-device must first enable the B-device to follow HNP. Refer to the “*On-The-Go Supplement to the USB 2.0 Specification*” for more information regarding HNP. HNP may only be initiated at full speed.

After being enabled for HNP by the A-device, the B-device requests being the host any time that the USB link is in suspend state, by simply indicating a disconnect. This can be done in software by clearing DPPULUP and DMPULUP. When the A-device detects the disconnect condition (via the URSTIF (U1IR<0>) interrupt), the A-device may allow the B-device to take over as host. The A-device does this by signaling connect as a full-speed function. Software may accomplish this by setting DPPULUP.

If the A-device responds instead with resume signaling, the A-device remains as host. When the B-device detects the connect condition (via ATTACHIF (U1IR<6>)), the B-device becomes host. The B-device drives Reset signaling prior to using the bus.

When the B-device has finished in its role as host, it stops all bus activity and turns on its D+ pull-up resistor by setting DPPULUP. When the A-device detects a suspend condition (Idle for 3 ms), the A-device turns off its D+ pull-up. The A-device may also power-down the VBUS supply to end the session. When the A-device detects the connect condition (via ATTACHIF), the A-device resumes host operation and drives Reset signaling.

18.6.3 EXTERNAL VBUS COMPARATORS

The external VBUS comparator option is enabled by setting the UVCMPDIS bit (U1CNFG2<1>). This disables the internal VBUS comparators, removing the need to attach VBUS to the microcontroller's VBUS pin.

The external comparator interface uses either the VCMPST1 and VCMPST2 pins, or the VBUSVLD, SESSVLD and SESSEND pins, based upon the setting of the UVCMPSEL bit (U1CNFG2<5>). These pins are digital inputs and should be set in the following patterns (see Table 18-3), based on the current level of the VBUS voltage.

TABLE 18-3: EXTERNAL VBUS COMPARATOR STATES

If UVCMPSEL = 0			
VCMPST1	VCMPST2	Bus Condition	
0	0	VBUS < VB_SESS_END	
1	0	VB_SESS_END < VBUS < VA_SESS_VLD	
0	1	VA_SESS_VLD < VBUS < VA_VBUS_VLD	
1	1	VBUS > VBUS_VLD	
If UVCMPSEL = 1			
VBUSVLD	SESSVLD	SESEND	Bus Condition
0	0	1	VBUS < VB_SESS_END
0	0	0	VB_SESS_END < VBUS < VA_SESS_VLD
0	1	0	VA_SESS_VLD < VBUS < VA_VBUS_VLD
1	1	0	VBUS > VBUS_VLD

PIC24FJ256DA210 FAMILY

REGISTER 22-26: G1CLUTWR: COLOR LOOK-UP TABLE (CLUT) MEMORY WRITE DATA REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLUTWR15	CLUTWR14	CLUTWR13	CLUTWR12	CLUTWR11	CLUTWR10	CLUTWR9	CLUTWR8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLUTWR7	CLUTWR6	CLUTWR5	CLUTWR4	CLUTWR3	CLUTWR2	CLUTWR1	CLUTWR0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0

CLUTWR<15:0>: Color Look-up Table Memory Write Data bits

A write to this register triggers a write to the CLUT memory at the address pointed to by the CLUTADR bits. A word write or a high byte write to this register triggers a write to the CLUT memory at the address pointed to by CLUTADR. Low byte write to this register will only update the G1CLUTWR<7:0> and no write to CLUT memory will be triggered. During power-up and power-down of the display, the most recent data written to this register will be used to control the timing of the GPWR signal. Refer to the "PIC24F Family Reference Manual", Section 43. "Graphics Controller Module (GFX)" for details on writing entries to the CLUT.

REGISTER 22-27: G1CLUTRD: COLOR LOOK-UP TABLE (CLUT) MEMORY READ DATA REGISTER

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
CLUTRD15	CLUTRD14	CLUTRD13	CLUTRD12	CLUTRD11	CLUTRD10	CLUTRD9	CLUTRD8
bit 15							bit 8

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
CLUTRD7	CLUTRD6	CLUTRD5	CLUTRD4	CLUTRD3	CLUTRD2	CLUTRD1	CLUTRD0
bit 7							bit 0

Legend:

HSC = Hardware Settable/Clearable bit

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0

CLUTRD<15:0>: Color Look-up Table Memory Read Data bits

This register contains the most recent read from the CLUT memory pointed to by the CLUTADR bits (G1CLUT<7:0>). Reading of the CLUT memory is triggered when the CLUTTRD bit (G1CLUT<9>) goes from '0' to '1'. Refer to the "PIC24F Family Reference Manual", Section 43. "Graphics Controller Module (GFX)" for details on reading entries from the CLUT.

PIC24FJ256DA210 FAMILY

REGISTER 23-5: ANCFG: A/D BAND GAP REFERENCE CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	VBG6EN	VBG2EN	VBGEN
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2 **VBG6EN:** A/D Input VBG/6 Enable bit

1 = Band gap voltage divided-by-six reference (VBG/6) is enabled

0 = Band gap divided-by-six reference (VBG/6) is disabled

bit 1 **VBG2EN:** A/D Input VBG/2 Enable bit

1 = Band gap voltage divided-by-two reference (VBG/2) is enabled

0 = Band gap divided-by-two reference (VBG/2) is disabled

bit 0 **VBGEN:** A/D Input VBG Enable bit

1 = Band gap voltage reference (VBG) is enabled

0 = Band gap reference (VBG) is disabled

REGISTER 23-6: AD1CSSL: A/D INPUT SCAN SELECT REGISTER (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **CSSL<15:0>:** A/D Input Pin Scan Selection bits

1 = Corresponding analog channel is selected for input scan

0 = Analog channel is omitted from input scan

PIC24FJ256DA210 FAMILY

REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN ⁽¹⁾	EDGEN	EDGSEQEN	IDISSEN	CTTRIG
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HSC	R/W-0, HSC
EDG2POL	EDG2SEL1	EDG2SEL0	EDG1POL	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **CTMUEN:** CTMU Enable bit
 1 = Module is enabled
 0 = Module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CTMUSIDL:** Stop in Idle Mode bit
 1 = Discontinue module operation when the device enters Idle mode
 0 = Continue module operation in Idle mode
- bit 12 **TGEN:** Time Generation Enable bit⁽¹⁾
 1 = Enables edge delay generation
 0 = Disables edge delay generation
- bit 10 **EDGEN:** Edge Enable bit
 1 = Edges are not blocked
 0 = Edges are blocked
- bit 10 **EDGSEQEN:** Edge Sequence Enable bit
 1 = Edge 1 event must occur before Edge 2 event can occur
 0 = No edge sequence is needed
- bit 9 **IDISSEN:** Analog Current Source Control bit
 1 = Analog current source output is grounded
 0 = Analog current source output is not grounded
- bit 8 **CTTRIG:** Trigger Control bit
 1 = Trigger output is enabled
 0 = Trigger output is disabled
- bit 7 **EDG2POL:** Edge 2 Polarity Select bit
 1 = Edge 2 is programmed for a positive edge response
 0 = Edge 2 is programmed for a negative edge response
- bit 6-5 **EDG2SEL<1:0>:** Edge 2 Source Select bits
 11 = CTEDG1 pin
 10 = CTEDG2 pin
 01 = OC1 module
 00 = Timer1 module
- bit 4 **EDG1POL:** Edge 1 Polarity Select bit
 1 = Edge 1 is programmed for a positive edge response
 0 = Edge 1 is programmed for a negative edge response

Note 1: If TGEN = 1, the peripheral inputs and outputs must be configured to an available RPn/RPIn pin. See **Section 10.4 "Peripheral Pin Select (PPS)"** for more information.

PIC24FJ256DA210 FAMILY

REGISTER 27-1: CW1: FLASH CONFIGURATION WORD 1 (CONTINUED)

bit 4	FWPSA: WDT Prescaler Ratio Select bit
	1 = Prescaler ratio of 1:128
	0 = Prescaler ratio of 1:32
bit 3-0	WDTPS<3:0>: Watchdog Timer Postscaler Select bits
	1111 = 1:32,768
	1110 = 1:16,384
	1101 = 1:8,192
	1100 = 1:4,096
	1011 = 1:2,048
	1010 = 1:1,024
	1001 = 1:512
	1000 = 1:256
	0111 = 1:128
	0110 = 1:64
	0101 = 1:32
	0100 = 1:16
	0011 = 1:8
	0010 = 1:4
	0001 = 1:2
	0000 = 1:1

Note 1: Unimplemented in 64-pin devices, maintain at '1' (VREF+ on RB0 and VREF- on RB1).

PIC24FJ256DA210 FAMILY

TABLE 29-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
TBLRDL	TBLRDL ws, wd	Read Prog<15:0> to Wd	1	2	None
TBLWTH	TBLWTH ws, wd	Write Ws<7:0> to Prog<23:16>	1	2	None
TBLWTL	TBLWTL ws, wd	Write Ws to Prog<15:0>	1	2	None
ULNK	ULNK	Unlink Frame Pointer	1	1	None
XOR	XOR f	f = f .XOR. WREG	1	1	N, Z
	XOR f, WREG	WREG = f .XOR. WREG	1	1	N, Z
	XOR #lit10, Wn	Wd = lit10 .XOR. Wd	1	1	N, Z
	XOR wb, ws, wd	Wd = Wb .XOR. Ws	1	1	N, Z
	XOR wb, #lit5, wd	Wd = Wb .XOR. lit5	1	1	N, Z
ZE	ZE ws, Wnd	Wnd = Zero-Extend Ws	1	1	C, Z, N

PIC24FJ256DA210 FAMILY

TABLE 30-13: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC mode)	DC 4	— —	32 48	MHz MHz	EC ECPLL
		Oscillator Frequency	3.5	—	10	MHz	XT
			4	—	8	MHz	XTPLL
			10	—	32	MHz	HS
			10 31	— —	32 33	MHz kHz	HSPLL SOSC
OS20	Tosc	Tosc = 1/Fosc	—	—	—	—	See parameter OS10 for Fosc value
OS25	Tcy	Instruction Cycle Time ⁽²⁾	62.5	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSCI) High or Low Time	0.45 x Tosc	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSCI) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ⁽³⁾	—	6	10	ns	
OS41	TckF	CLKO Fall Time ⁽³⁾	—	6	10	ns	

- Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** Instruction cycle period (Tcy) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Min." values with an external clock applied to the OSCI/CLKI pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.
- 3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin. CLKO is low for the Q1-Q2 period (1/2 Tcy) and high for the Q3-Q4 period (1/2 Tcy).

TABLE 30-14: PLL CLOCK TIMING SPECIFICATIONS (VDD = 2.2V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
OS50	FPLLI	PLL Input Frequency Range ⁽²⁾	4	—	48	MHz	ECPLL mode
			4		32	MHz	HSPLL mode
			4		8	MHz	XTPLL mode
OS51	FSYS	PLL Output Frequency Range	95.76	—	96.24	MHz	
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	200	μs	
OS53	DCLK	CLKO Stability (Jitter)	-0.25	—	0.25	%	

- Note 1:** These parameters are characterized but not tested in manufacturing.
- 2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

APPENDIX A: REVISION HISTORY

Revision A (February 2010)

Original data sheet for the PIC24FJ256DA210 family of devices.

Revision B (May 2010)

Minor changes throughout text and the values in **Section 30.0 “Electrical Characteristics”** were updated.

PIC24FJ256DA210 FAMILY

OSCTUN (FRC Oscillator Tune).....	146	Revision History.....	397
PADCFG1 (Pad Configuration Control).....	283, 288	RTCC	
PMCON1 (EPMP Control 1).....	275	Alarm Configuration.....	294
PMCON2 (EPMP Control 2).....	276	Calibration.....	294
PMCON3 (EPMP Control 3).....	277	Key Features.....	285
PMCON4 (EPMP Control 4).....	278	Register Mapping.....	286
PMCSxBS (Chip Select x Base Address).....	280	S	
PMCSxCF (Chip Select x Configuration).....	279	Selective Peripheral Power Control.....	156
PMCSxMD (Chip Select x Mode).....	281	Serial Peripheral Interface (SPI).....	211
PMSTAT (EPMP Status, Slave Mode).....	282	Serial Peripheral Interface. <i>See</i> SPI.	
RCFGCAL (RTCC Calibration and Configuration)....	287	SFR Space.....	49
RCON (Reset Control).....	88	Sleep Mode.....	155
REFOCON (Reference Oscillator Control).....	153	Software Simulator (MPLAB SIM).....	361
RPINRn (PPS Input).....	169–179	Software Stack.....	75
RPORn (PPS Output).....	180–187	Special Features.....	16
SPIxCON1 (SPIx Control 1).....	216	SPI.....	211
SPIxCON2 (SPIx Control 2).....	218	T	
SPIxSTAT (SPIx Status and Control).....	214	Timer1.....	189
SR (ALU STATUS).....	42, 97	Timer2/3 and Timer4/5.....	191
T1CON (Timer1 Control).....	190	Timing Diagrams	
TxCON (Timer2 and Timer4 Control).....	194	CLKO and I/O Timing.....	383
TyCON (Timer3 and Timer5 Control).....	195	External Clock.....	380
U1ADDR (USB Address).....	261	Triple Comparator.....	335
U1CNFG1 (USB Configuration 1).....	262	Triple Comparator Module.....	335
U1CNFG2 (USB Configuration 2).....	263	U	
U1CON (USB Control, Device Mode).....	259	UART.....	231
U1CON (USB Control, Host Mode).....	260	Baud Rate Generator (BRG).....	232
U1EIE (USB Error Interrupt Enable).....	270	IrDA Support.....	233
U1EIR (USB Error Interrupt Status).....	269	Operation of $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins.....	233
U1EPn (USB Endpoint n Control).....	271	Receiving in 8-Bit or 9-Bit Data Mode.....	233
U1IE (USB Interrupt Enable).....	268	Transmitting	
U1IR (USB Interrupt Status, Device Mode).....	266	Break and Sync Sequence.....	233
U1IR (USB Interrupt Status, Host Mode).....	267	in 8-Bit Data Mode.....	233
U1OTGCON (USB OTG Control).....	256	Transmitting in 9-Bit Data Mode.....	233
U1OTGIE (USB OTG Interrupt Enable,		Universal Asynchronous Receiver Transmitter. <i>See</i> UART.	
Host Mode).....	265	Universal Serial Bus	
U1OTGIR (USB OTG Interrupt Status,		Buffer Descriptors	
Host Mode).....	264	Assignment in Different Buffering Modes.....	245
U1OTGSTAT (USB OTG Status).....	255	Interrupts	
U1PWMCN USB (VBUS PWM Generator		and USB Transactions.....	249
Control).....	272	Universal Serial Bus. <i>See</i> USB OTG.	
U1PWRC (USB Power Control).....	257	USB On-The-Go (OTG).....	16
U1SOF (USB OTG Start-Of-Token		USB OTG.....	239
Threshold, Host Mode).....	262	Buffer Descriptors and BDT.....	244
U1STAT (USB Status).....	258	Device Mode Operation.....	249
U1TOK (USB Token, Host Mode).....	261	DMA Interface.....	245
UxMODE (UARTx Mode).....	234	Hardware	
UxSTA (UARTx Status and Control).....	236	Calculating	
WKDYHR (RTCC Weekday and Hours Value).....	291	Transceiver Power Requirements.....	243
YEAR (RTCC Year Value).....	290	Hardware Configuration.....	241
Resets		Device Mode.....	241
BOR (Brown-out Reset).....	87	External Interface.....	243
Clock Source Selection.....	90	Host and OTG Modes.....	242
CM (Configuration Mismatch Reset).....	87	VBUS Voltage Generation.....	243
Delay Times.....	91	Host Mode Operation.....	250
Device Times.....	90	Interrupts.....	248
IOPUWR (Illegal Opcode Reset).....	87	Operation.....	252
MCLR (Pin Reset).....	87	Registers.....	254
POR (Power-on Reset).....	87	VBUS Voltage Generation.....	243
RCON Flags Operation.....	89		
SFR States.....	90		
SWR (RESET Instruction).....	87		
TRAPR (Trap Conflict Reset).....	87		
UWR (Uninitialized W Register Reset).....	87		
WDT (Watchdog Timer Reset).....	87		