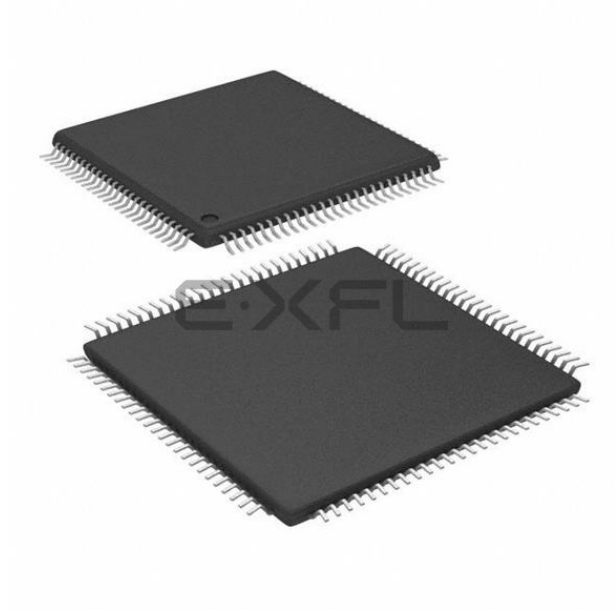
Microchip Technology - PIC24FJ256DA110T-I/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, GFX, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256da110t-i-pt

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 100-PIN DEVICES

Pin	Function	Pin	Function
1	GCLK/CN82/RG15	41	AN12/PMA11/CTEDG2/CN30/RB12
2	VDD	42	AN13/PMA10/CTEDG1/CN31/RB13
3	PMD5/CN63/RE5	43	AN14/CTPLS/**RP14**/PMA1/CN32/RB14
4	SCL3/PMD6/CN64/RE6	44	AN15/REFO/**RP29**/PMA0/CN12/RB15
5	SDA3/PMD7/CN65/RE7	45	VSS
6	**RPI38**/GD0/CN45/RC1	46	VDD
7	**RPI39**/GD8/CN46/RC2	47	**RPI43**/GD14/CN20/RD14
8	**RPI40**/GD1/CN47/RC3	48	**RP5**/GD15/CN21/RD15
9	AN16/**RPI41**/PMCS2/PMA22(2)/CN48/RC4	49	**RP10**/PMA9/CN17/RF4
10	AN17/C1IND/**RP21**/PMA5/PMA18(2)/CN8/RG6	50	**RP17**/PMA8/CN18/RF5
11	AN18/C1INC/**RP26**/PMA4/PMA20(2)/CN9/RG7	51	**RP16**/USBID/CN71/RF3
12	AN19/C2IND/**RP19**/PMA3/PMA21(2)/CN10/RG8	52	**RP30**/GD3/CN70/RF2
13	$\overline{\text{MCLR}}$	53	**RP15**/GD9/CN74/RF8
14	AN20/C2INC/**RP27**/PMA2/CN11/RG9	54	VBUS/CN73/RF7
15	VSS	55	VUSB
16	VDD	56	D-/CN84/RG3
17	TMS/CN33/RA0	57	D+/CN83/RG2
18	**RPI33**/PMCS1/CN66/RE8	58	SCL2/CN35/RA2
19	AN21/**RPI34**/PMA19/CN67/RE9	59	SDA2/PMA20/PMA4(2)/CN36/RA3
20	PGEC3/AN5/C1INA/VBUSON/**RP18**/CN7/RB5	60	TDI/PMA21/PMA3(2)/CN37/RA4
21	PGED3/AN4/C1INB/USBOEN/**RP28**/GD4/CN6/RB4	61	TDO/CN38/RA5
22	AN3/C2INA/GD5/VPIO/CN5/RB3	62	VDD
23	AN2/C2INB/VMIO/**RP13**/GD6/CN4/RB2	63	OSCI/CLKI/CN23/RC12
24	PGEC1/AN1/VREF-(1)/**RP1**/CN3/RB1	64	OSCO/CLKO/CN22/RC15
25	PGED1/AN0/VREF+(1)/**RP0**/CN2/RB0	65	VSS
26	PGEC2/AN6/**RP6**/CN24/RB6	66	SCL1/**RPI36**/PMA22/PMCS2(2)/CN43/RA14
27	PGED2/AN7/**RP7**/RCV/GPWR/CN25/RB7	67	SDA1/**RPI35**/PMBE1/CN44/RA15
28	VREF-/PMA7/CN41/RA9	68	DMLN/RTCC/**RP2**/CN53/RD8
29	VREF+/PMA6/CN42/RA10	69	DPLN/**RP4**/GD10/PMACK2/CN54/RD9
30	AVDD	70	**RP3**/PMA15/PMCS2(3)/CN55/RD10
31	AVSS	71	**RP12**/PMA14/PMCS1(3)/CN56/RD11
32	AN8/**RP8**/GD12/CN26/RB8	72	DMH/**RP11**/INT0/CN49/RD0
33	AN9/**RP9**/GD13/CN27/RB9	73	SOSCI/C3IND/CN1/RC13
34	AN10/CVREF/PMA13/CN28/RB10	74	SOSCO/SCLKI/T1CK/C3INC/**RPI37**/CN0/RC14
35	AN11/PMA12/CN29/RB11	75	VSS
36	VSS	76	VCPCON/**RP24**/GD7/VBUSCHG/CN50/RD1
37	VDD	77	DPH/**RP23**/GD11/PMACK1/CN51/RD2
38	TCK/CN34/RA1	78	**RP22**/PMBE0/CN52/RD3
39	**RP31**/GD2/CN76/RF13	79	**RPI42**/PMD12/CN57/RD12
40	**RPI32**/PMA18/PMA5(2)/CN75/RF12	80	PMD13/CN19/RD13

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note 1: Alternate pin assignments for VREF+ and VREF- when the $\overline{\text{ALTVREF}}$ Configuration bit is programmed.

2: Alternate pin assignments for EPMP when the $\overline{\text{ALTPMP}}$ Configuration bit is programmed.

3: Pin assignment for PMCSx when CSF<1:0> is not equal to '00'.

TABLE 1-3: PIC24FJ256DA210 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
PGEC1	15	24	K1	I/O	ST	In-Circuit Debugger/Emulator/ICSP™ Programming Clock 1.
PGED1	16	25	K2	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data 1.
PGEC2	17	26	L1	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock 2.
PGED2	18	27	J3	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data 2.
PGEC3	11	20	H1	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock 3.
PGED3	12	21	H2	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data 3.
PMA0	—	44	L8	I/O	ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	—	43	K7	I/O	ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2	—	14	F3	O	—	Parallel Master Port Address bits<22:2>.
PMA3	—	12, 60(1)	F2, G11(1)	O	—	
PMA4	—	11,59(1)	F4,G10(1)	O	—	
PMA5	—	10,40(1)	E3,K6(1)	O	—	
PMA6	—	29	K3	O	—	
PMA7	—	28	L2	O	—	
PMA8	—	50	L11	O	—	
PMA9	—	49	L10	O	—	
PMA10	—	42	L7	O	—	
PMA11	—	41	J7	O	—	
PMA12	—	35	J5	O	—	
PMA13	—	34	L5	O	—	
PMA14	—	71	C11	O	—	
PMA15	—	70	D11	O	—	
PMA16	—	95	C4	O	—	
PMA17	—	92	B5	O	—	
PMA18	—	40,10(1)	K6,E3(1)	O	—	
PMA19	—	19	G2	O	—	
PMA20	—	59, 11(1)	G10, F4(1)	O	—	
PMA21	—	60,12(1)	G11,F2(1)	O	—	
PMA22	—	66,9(1)	E11,E1(1)	O	—	
PMACK1	—	77	A10	I	ST/TTL	Parallel Master Port Acknowledge Input 1.
PMACK2	—	69	E10	I	ST/TTL	Parallel Master Port Acknowledge Input 2.
PMALL	—	44	L8	O	—	Parallel Master Port Lower Address Latch Strobe.
PMALH	—	43	K7	O	—	Parallel Master Port Higher Address Latch Strobe.
PMALU	—	14	F3	O	—	Parallel Master Port Upper Address Latch Strobe.
PMBE0	—	78	B9	O	—	Parallel Master Port Byte Enable Strobe 0.
PMBE1	—	67	E8	O	—	Parallel Master Port Byte Enable Strobe 1.
PMCS1	—	71(3),18	C11(3),G1	I/O	ST/TTL	Parallel Master Port Chip Select Strobe 1.
PMCS2	—	70(2),9, 66(1)	D11(2),E1, E11(1)	O	—	Parallel Master Port Chip Select Strobe 2.

Legend: TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; I^2C™ = I^2C/SMBus input buffer

Note 1: The alternate EPMP pins are selected when the $\overline{\text{ALTPMP}}$ (CW3<12>) bit is programmed to '0'.

2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.

3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.

4: The alternate VREF pins selected when the $\overline{\text{ALTVREF}}$ (CW1<5>) bit is programmed to '0'.

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during code execution. This arrangement also provides compatibility with data memory space addressing and makes it possible to access data in the program memory space.

4.1.2 HARD MEMORY VECTORS

All PIC24F devices reserve the addresses between 0x00000 and 0x000200 for hard coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user at 0x000000 with the actual address for the start of code at 0x000002.

PIC24F devices also have two interrupt vector tables, located from 0x000004 to 0x0000FF and 0x000100 to 0x0001FF. These vector tables allow each of the many device interrupt sources to be handled by separate ISRs. A more detailed discussion of the interrupt vector tables is provided in **Section 7.1 "Interrupt Vector Table"**.

4.1.3 FLASH CONFIGURATION WORDS

In PIC24FJ256DA210 family devices, the top four words of on-chip program memory are reserved for configuration information. On device Reset, the configuration information is copied into the appropriate Configuration register. The addresses of the Flash Configuration Word for devices in the PIC24FJ256DA210 family are shown in Table 4-1. Their location in the memory map is shown with the other memory vectors in Figure 4-1.

The Configuration Words in program memory are a compact format. The actual Configuration bits are mapped in several different registers in the configuration memory space. Their order in the Flash Configuration Words does not reflect a corresponding arrangement in the configuration space. Additional details on the device Configuration Words are provided in **Section 27.1 "Configuration Bits"**.

TABLE 4-1: FLASH CONFIGURATION WORDS FOR PIC24FJ256DA210 FAMILY DEVICES

Device	Program Memory (Words)	Configuration Word Addresses
PIC24FJ128DAXXX	44,032	0x0157F8:0x0157FE
PIC24FJ256DAXXX	87,552	0x02ABF8:0x02ABFE

FIGURE 4-2: PROGRAM MEMORY ORGANIZATION

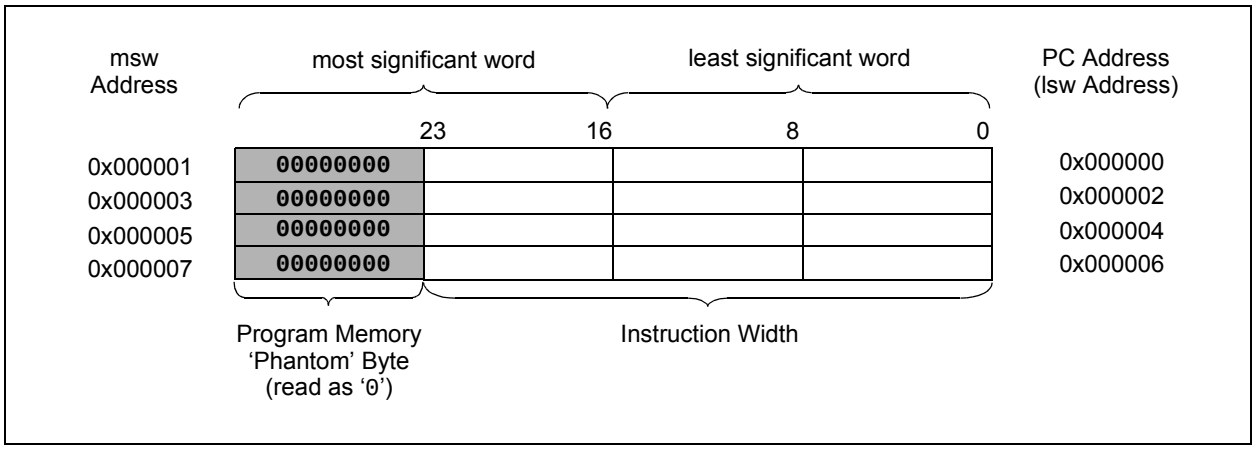


TABLE 4-31: GRAPHICS REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
G1CMDL	0700	Graphics Command Register<15:0>																0000
G1CMDH	0702	Graphics Command Register<31:16>																0000
G1CON1	0704	G1EN	—	G1SIDL	GCMDWMK4	GCMDWMK3	GCMDWMK2	GCMDWMK1	GCMDWMK0	PUBPP2	PUBPP1	PUBPP0	GCMDCNT4	GCMDCNT3	GCMDCNT2	GCMDCNT1	GCMDCNT0	0000
G1STAT	0706	PUBUSY	—	—	—	—	—	—	—	IPUBUSY	RCCBUSY	CHRBUSY	VMRGN	HMRGN	CMDLV	CMDFUL	CMDMPT	0000
G1IE	0708	PUIE	—	—	—	—	—	—	—	IPUIE	RCCIE	CHRIE	VMRGNIE	HMRGNIE	CMDLVIE	CMDFULIE	CMDMPTIE	0000
G1IR	070A	PUIF	—	—	—	—	—	—	—	IPUIF	RCCIF	CHRIF	VMRGNIF	HMRGNIF	CMDLVIF	CMDFULIF	CMDMPTIF	0000
G1W1ADRL	070C	GPU Work Area 1 Start Address Register<15:0>																0000
G1W1ADRH	070E	—	—	—	—	—	—	—	—	GPU Work Area 1 Start Address Register<23:16>								0000
G1W2ADRL	0710	GPU Work Area 2 Start Address Register<15:0>																0000
G1W2ADRH	0712	—	—	—	—	—	—	—	—	GPU Work Area 2 Start Address Register<23:16>								0000
G1PUW	0714	—	—	—	—	—	GPU Work Area Width Register											0000
G1PUH	0716	—	—	—	—	—	GPU Work Area Height Register											0000
G1DPADRL	0718	Display Buffer Start Address Register<15:0>																0000
G1DPADRH	071A	—	—	—	—	—	—	—	—	Display Buffer Start Address Register<23:16>								0000
G1DPW	071C	—	—	—	—	—	Display Frame Width Register											0000
G1DPH	071E	—	—	—	—	—	Display Frame Height Register											0000
G1DPWT	0720	—	—	—	—	—	Display Total Width Register											0000
G1DPHT	0722	—	—	—	—	—	Display Total Height Register											0000
G1CON2	0724	DPGWDTH1	DPGWDTH0	DPSTGER1	DPSTGER0	—	—	DPTEST1	DPTEST0	DPBPP2	DPBPP1	DPBPP0	—	—	DPMODE2	DPMODE1	DPMODE0	0000
G1CON3	0726	—	—	—	—	—	—	DPPINOE	DPPOWER	DPCLKPOL	DPENPOL	DPVSPOL	DPHSPOL	DPPWROE	DPENOE	DPVSOE	DPHSOE	0000
G1ACTDA	0728	Number of Lines Before the First Active Line Register								Number of Pixels Before the First Active PIxel Register								0000
G1HSYNC	072A	HSYNC Pulse-Width Configuration Register								HSYNC Start Delay Configuration Register								0000
G1VSYNC	072C	VSYNC Pulse-Width Configuration Register								VSYNC Start Delay Configuration Register								0000
G1DBLCON	072E	Vertical Blanking Start to First Displayed Line Configuration Regsiter								Horizontal Blanking Start to First Displayed Line Configuration Regsiter								0000
G1CLUT	0730	CLUTEN	CLUTBUSY	—	—	—	—	CLUTTRD	CLUTRWEN	Color Look-Up Table Memory Address Register								0000
G1CLUTWR	0732	Color Look-up Table Memory Write Data Register																0000
G1CLUTRD	0734	Color Look-up Table Memory Read Data Register																0000
G1MRGN	0736	Vertical Blanking Advance Register								Horizontal Blanking Advance Register								0000
G1CHRX	0738	—	—	—	—	—	Current Character X-Coordinate Position Register											0000
G1CHRY	073A	—	—	—	—	—	Current Character Y-Coordinate Position Register											0000
G1IPU	073C	—	—	—	—	—	—	—	—	—	—	HUFFERR	BLCKERR	LENERR	WRAPERR	IPUDONE	BFINAL	0000
G1DBEN	073E	GDBEN15	GDBEN14	GDBEN13	GDBEN12	GDBEN11	GDBEN10	GDBEN9	GDBEN8	GDBEN7	GDBEN6	GDBEN5	GDBEN4	GDBEN3	GDBEN2	GDBEN1	GDBEN0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.3.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).

   In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address (P<23:16>) to a data address. Note that D<15:8>, the 'phantom' byte, will always be '0'.

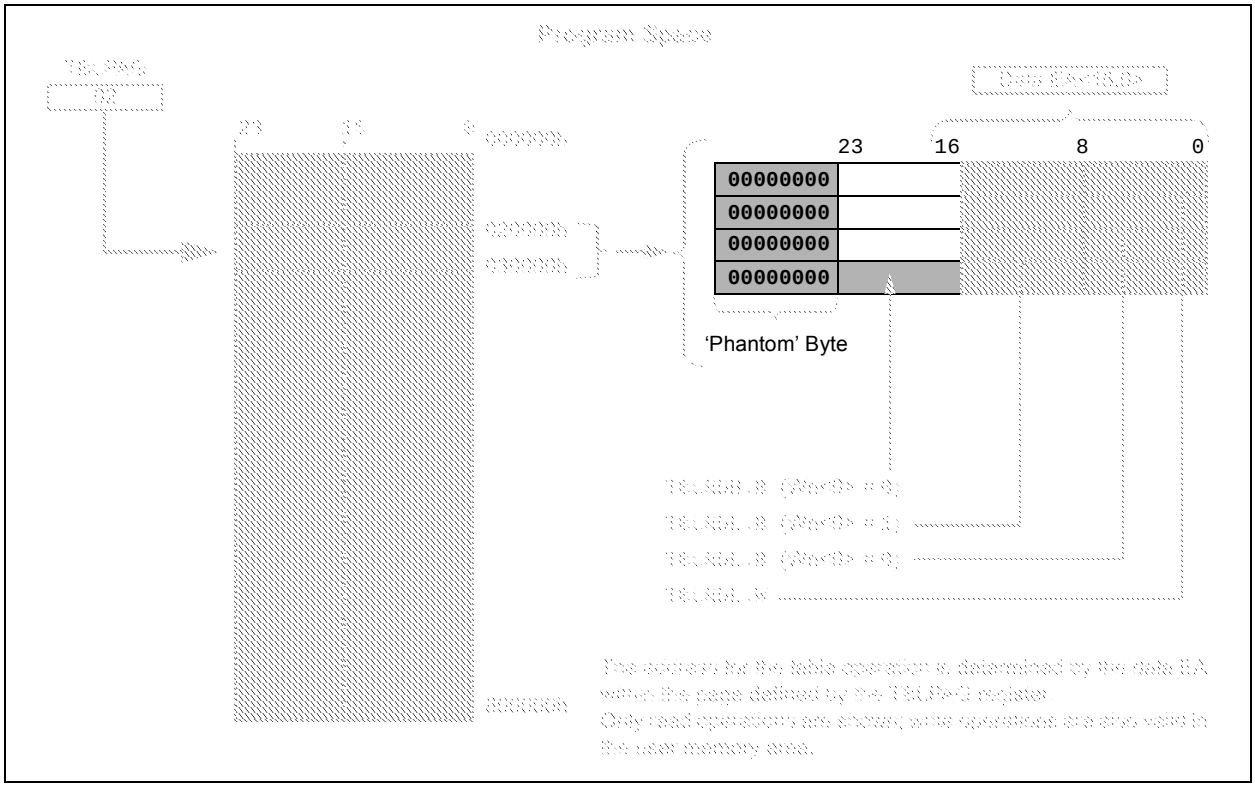
   In Byte mode, it maps the upper or lower byte of the program word to D<7:0> of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (byte select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are described in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

Note:	Only table read operations will execute in the configuration memory space, where Device IDs are located. Table write operations are not allowed.

FIGURE 4-9: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



5.6.2 PROGRAMMING A SINGLE WORD OF FLASH PROGRAM MEMORY

If a Flash location has been erased, it can be programmed using table write instructions to write an instruction word (24-bit) into the write latch. The TBLPAG register is loaded with the 8 Most Significant Bytes (MSB) of the Flash address. The TBLWTL and TBLWTH instructions write the desired data into the write latches and specify the lower 16 bits of the program memory address to write to. To configure the NVMCON register for a word write, set the NVMOP bits (NVMCON<3:0>) to '0011'. The write is performed by executing the unlock sequence and setting the WR bit (see Example 5-5). An equivalent procedure in 'C' compiler, using the MPLAB C30 compiler and built-in hardware functions is shown in Example 5-6.

EXAMPLE 5-5: PROGRAMMING A SINGLE WORD OF FLASH PROGRAM MEMORY

```
; Setup a pointer to data Program Memory
    MOV     #tblpage(PROG_ADDR), W0       ;
    MOV     W0, TBLPAG                    ;Initialize PM Page Boundary SFR
    MOV     #tbloffset(PROG_ADDR), W0     ;Initialize a register with program memory address

    MOV     #LOW_WORD_N, W2               ;
    MOV     #HIGH_BYTE_N, W3              ;
    TBLWTL  W2, [W0]                      ; Write PM low word into program latch
    TBLWTH  W3, [W0++]                    ; Write PM high byte into program latch

; Setup NVMCON for programming one word to data Program Memory
    MOV     #0x4003, W0                   ;
    MOV     W0, NVMCON                    ; Set NVMOP bits to 0011

    DISI    #5                            ; Disable interrupts while the KEY sequence is written
    MOV.B   #0x55, W0                     ; Write the key sequence
    MOV     W0, NVMKEY
    MOV.B   #0xAA, W0
    MOV     W0, NVMKEY
    BSET    NVMCON, #WR                   ; Start the write cycle
    NOP                                   ; Required delays
    NOP
```

EXAMPLE 5-6: PROGRAMMING A SINGLE WORD OF FLASH PROGRAM MEMORY ('C' LANGUAGE CODE)

```
// C example using MPLAB C30
unsigned int offset;
unsigned long progAddr = 0xXXXXXX;           // Address of word to program
unsigned int progDataL = 0xXXXX;             // Data to program lower word
unsigned char progDataH = 0xXX;              // Data to program upper byte

//Set up NVMCON for word programming
NVMCON = 0x4003;                             // Initialize NVMCON

//Set up pointer to the first memory location to be written
TBLPAG = progAddr>>16;                       // Initialize PM Page Boundary SFR
offset = progAddr & 0xFFFF;                  // Initialize lower word of address

//Perform TBLWT instructions to write latches
__builtin_tblwtl(offset, progDataL);         // Write to address low word
__builtin_tblwth(offset, progDataH);         // Write to upper byte
asm("DISI #5");                              // Block interrupts with priority <7
                                             // for next 5 instructions
__builtin_write_NVM();                       // C30 function to perform unlock
                                             // sequence and set WR
```

REGISTER 7-9: IFS4: INTERRUPT FLAG STATUS REGISTER 4

U-0	U-0	R/W-0, HS	U-0	U-0	U-0	U-0	R/W-0, HS
—	—	CTMUIF	—	—	—	—	LVDIF
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0
—	—	—	—	CRCIF	U2ERIF	U1ERIF	—
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CTMUIF:** CTMU Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **LVDIF:** Low-Voltage Detect Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **CRCIF:** CRC Generator Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **U2ERIF:** UART2 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **U1ERIF:** UART1 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **Unimplemented:** Read as '0'

REGISTER 7-32: IPC13: INTERRUPT PRIORITY CONTROL REGISTER 13

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT4IP2	INT4IP1	INT4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	INT3IP2	INT3IP1	INT3IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **INT4IP<2:0>:** External Interrupt 4 Priority bits
- 111 = Interrupt is priority 7 (highest priority interrupt)
- •
- •
- •
- 001 = Interrupt is priority 1
- 000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **INT3IP<2:0>:** External Interrupt 3 Priority bits
- 111 = Interrupt is priority 7 (highest priority interrupt)
- •
- •
- •
- 001 = Interrupt is priority 1
- 000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 12-2: TyCON: TIMER3 AND TIMER5 CONTROL REGISTER(3)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL(1)	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(1)	TCKPS1(1)	TCKPS0(1)	—	—	TCS(1,2)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit(1)
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,2)
1 = External clock from pin, TyCK (on the rising edge)
0 = Internal clock (FOSC/2)

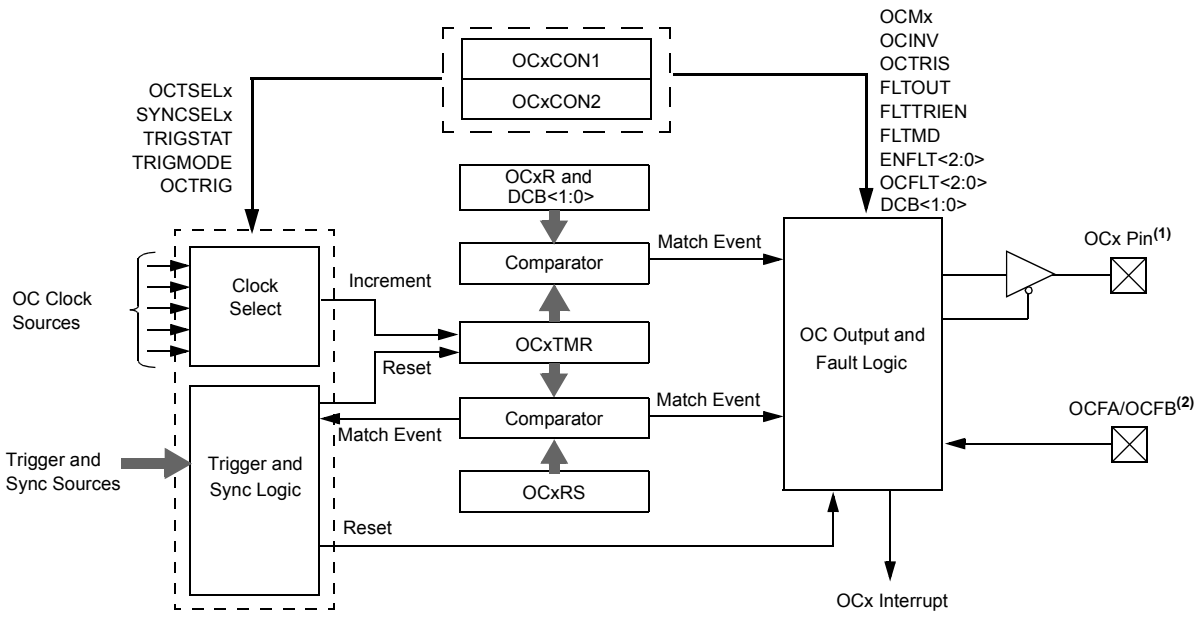
bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> or T4CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through T2CON and T4CON.

2: If TCS = 1, RPINRx (TxCK) must be configured to an available RPn/RPIn pin. See **Section 10.4 "Peripheral Pin Select (PPS)"** for more information.

3: Changing the value of TyCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

FIGURE 14-1: OUTPUT COMPARE BLOCK DIAGRAM (16-BIT MODE)



Note 1: The OCx outputs must be assigned to an available RPn pin before use. See **Section 10.4 "Peripheral Pin Select (PPS)"** for more information.

2: The OCFA/OCFB fault inputs must be assigned to an available RPn/RPIn pin before use. See **Section 10.4 "Peripheral Pin Select (PPS)"** for more information.

14.2 Compare Operations

In Compare mode (Figure 14-1), the output compare module can be configured for single-shot or continuous pulse generation. It can also repeatedly toggle an output pin on each timer event.

To set up the module for compare operations:

1. Configure the OCx output for one of the available Peripheral Pin Select pins.
2. Calculate the required values for the OCxR and (for Double Compare modes) OCxRS Duty Cycle registers:
   a) Determine the instruction clock cycle time. Take into account the frequency of the external clock to the timer source (if one is used) and the timer prescaler settings.
   b) Calculate time to the rising edge of the output pulse relative to the timer start value (0000h).
   c) Calculate the time to the falling edge of the pulse based on the desired pulse width and the time to the rising edge of the pulse.
3. Write the rising edge value to OCxR and the falling edge value to OCxRS.
4. Set the Timer Period register, PRy, to a value equal to or greater than the value in OCxRS.
5. Set the OCM<2:0> bits for the appropriate compare operation (= 0xx).
6. For Trigger mode operations, set OCTRIG to enable Trigger mode. Set or clear TRIGMODE to configure trigger operation and TRIGSTAT to select a hardware or software trigger. For Synchronous mode, clear OCTRIG.
7. Set the SYNCSEL<4:0> bits to configure the trigger or synchronization source. If free-running timer operation is required, set the SYNCSEL bits to '00000' (no sync/trigger source).
8. Select the time base source with the OCTSEL<2:0> bits. If necessary, set the TON bits for the selected timer, which enables the compare time base to count. Synchronous mode operation starts as soon as the time base is enabled; Trigger mode operation starts after a trigger source event occurs.

14.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the OCxRS and OCxR registers. The OCxRS and OCxR registers can be written to at any time, but the duty cycle value is not latched until a match between PRy and TMRy occurs (i.e., the period is complete). This provides a double buffer for the PWM duty cycle and is essential for glitchless PWM operation.

Some important boundary parameters of the PWM duty cycle include:

- If OCxR, OCxRS, and PRy are all loaded with 0000h, the OCx pin will remain low (0% duty cycle).
- If OCxRS is greater than PRy, the pin will remain high (100% duty cycle).

See Example 14-1 for PWM mode timing details. Table 14-1 and Table 14-2 show example PWM frequencies and resolutions for a device operating at 4 MIPS and 10 MIPS, respectively.

EQUATION 14-2: CALCULATION FOR MAXIMUM PWM RESOLUTION(1)

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}\left(\frac{FCY}{FPWM \bullet (\text{Timer Prescale Value})}\right)}{\log_{10}(2)} \text{ bits}$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

EXAMPLE 14-1: PWM PERIOD AND DUTY CYCLE CALCULATIONS(1)

1. Find the Timer Period register value for a desired PWM frequency of 52.08 kHz, where FOSC = 8 MHz with PLL (32 MHz device clock rate) and a Timer2 prescaler setting of 1:1.

   TCY = 2 * TOSC = 62.5 ns

   PWM Period = 1/PWM Frequency = 1/52.08 kHz = 19.2 ms

   PWM Period = (PR2 + 1) • TCY • (Timer2 Prescale Value)

   19.2 ms = PR2 + 1) • 62.5 ns • 1

   PR2 = 306

2. Find the maximum resolution of the duty cycle that can be used with a 52.08 kHz frequency and a 32 MHz device clock rate:

   PWM Resolution = $\log_{10}(FCY/FPWM)/\log_{10}2)$ bits

   = $(\log_{10}(16 \text{ MHz}/52.08 \text{ kHz})/\log_{10}2)$ bits

   = 8.3 bits

Note 1: Based on TCY = 2 * TOSC; Doze mode and PLL are disabled.

TABLE 14-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 4 MIPS (FCY = 4 MHz)(1)

PWM Frequency	7.6 Hz	61 Hz	122 Hz	977 Hz	3.9 kHz	31.3 kHz	125 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

TABLE 14-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 16 MIPS (FCY = 16 MHz)(1)

PWM Frequency	30.5 Hz	244 Hz	488 Hz	3.9 kHz	15.6 kHz	125 kHz	500 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

REGISTER 14-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits
11111 = This OC module(1)
11110 = Input Capture 9(2)
11101 = Input Capture 6(2)
11100 = CTMU(2)
11011 = A/D(2)
11010 = Comparator 3(2)
11001 = Comparator 2(2)
11000 = Comparator 1(2)
10111 = Input Capture 4(2)
10110 = Input Capture 3(2)
10101 = Input Capture 2(2)
10100 = Input Capture 1(2)
10011 = Input Capture 8(2)
10010 = Input Capture 7(2)
1000x = Reserved
01111 = Timer5
01110 = Timer4
01101 = Timer3
01100 = Timer2
01011 = Timer1
01010 = Input Capture 5(2)
01001 = Output Compare 9(1)
01000 = Output Compare 8(1)
00111 = Output Compare 7(1)
00110 = Output Compare 6(1)
00101 = Output Compare 5(1)
00100 = Output Compare 4(1)
00011 = Output Compare 3(1)
00010 = Output Compare 2(1)
00001 = Output Compare 1(1)
00000 = Not synchronized to any other module

Note 1: Never use an OC module as its own trigger source, either by selecting this mode or another equivalent SYNCSEL setting.
2: Use these inputs as trigger sources only and never as sync sources.
3: The DCB<1:0> bits are double-buffered in the PWM modes only (OCM<2:0> (OCxCON1<2:0>) = 111, 110).

18.0 UNIVERSAL SERIAL BUS WITH ON-THE-GO SUPPORT (USB OTG)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **Section 27. "USB On-The-Go (OTG)"** (DS39721). The information in this data sheet supersedes the information in the FRM.

PIC24FJ256DA210 family devices contain a full-speed and low-speed compatible, On-The-Go (OTG) USB Serial Interface Engine (SIE). The OTG capability allows the device to act either as a USB peripheral device or as a USB embedded host with limited host capabilities. The OTG capability allows the device to dynamically switch from device to host operation using OTG's Host Negotiation Protocol (HNP).

For more details on OTG operation, refer to the "*On-The-Go Supplement to the USB 2.0 Specification*", published by the USB-IF. For more details on USB operation, refer to the "*Universal Serial Bus Specification*", v2.0.

The USB OTG module offers these features:

- USB functionality in Device and Host modes, and OTG capabilities for application-controlled mode switching
- Software-selectable module speeds of full speed (12 Mbps) or low speed (1.5 Mbps, available in Host mode only)
- Support for all four USB transfer types: control, interrupt, bulk and isochronous
- 16 bidirectional endpoints for a total of 32 unique endpoints
- DMA interface for data RAM access
- Queues up to sixteen unique endpoint transfers without servicing
- Integrated, on-chip USB transceiver with support for off-chip transceivers via a digital interface
- Integrated VBUS generation with on-chip comparators and boost generation, and support of external VBUS comparators and regulators through a digital interface
- Configurations for on-chip bus pull-up and pull-down resistors

A simplified block diagram of the USB OTG module is shown in Figure 18-1.

The USB OTG module can function as a USB peripheral device or as a USB host, and may dynamically switch between Device and Host modes under software control. In either mode, the same data paths and Buffer Descriptors (BDs) are used for the transmission and reception of data.

In discussing USB operation, this section will use a controller-centric nomenclature for describing the direction of the data transfer between the microcontroller and the USB. RX (Receive) will be used to describe transfers that move data from the USB to the microcontroller and TX (Transmit) will be used to describe transfers that move data from the microcontroller to the USB. Table 18-1 shows the relationship between data direction in this nomenclature and the USB tokens exchanged.

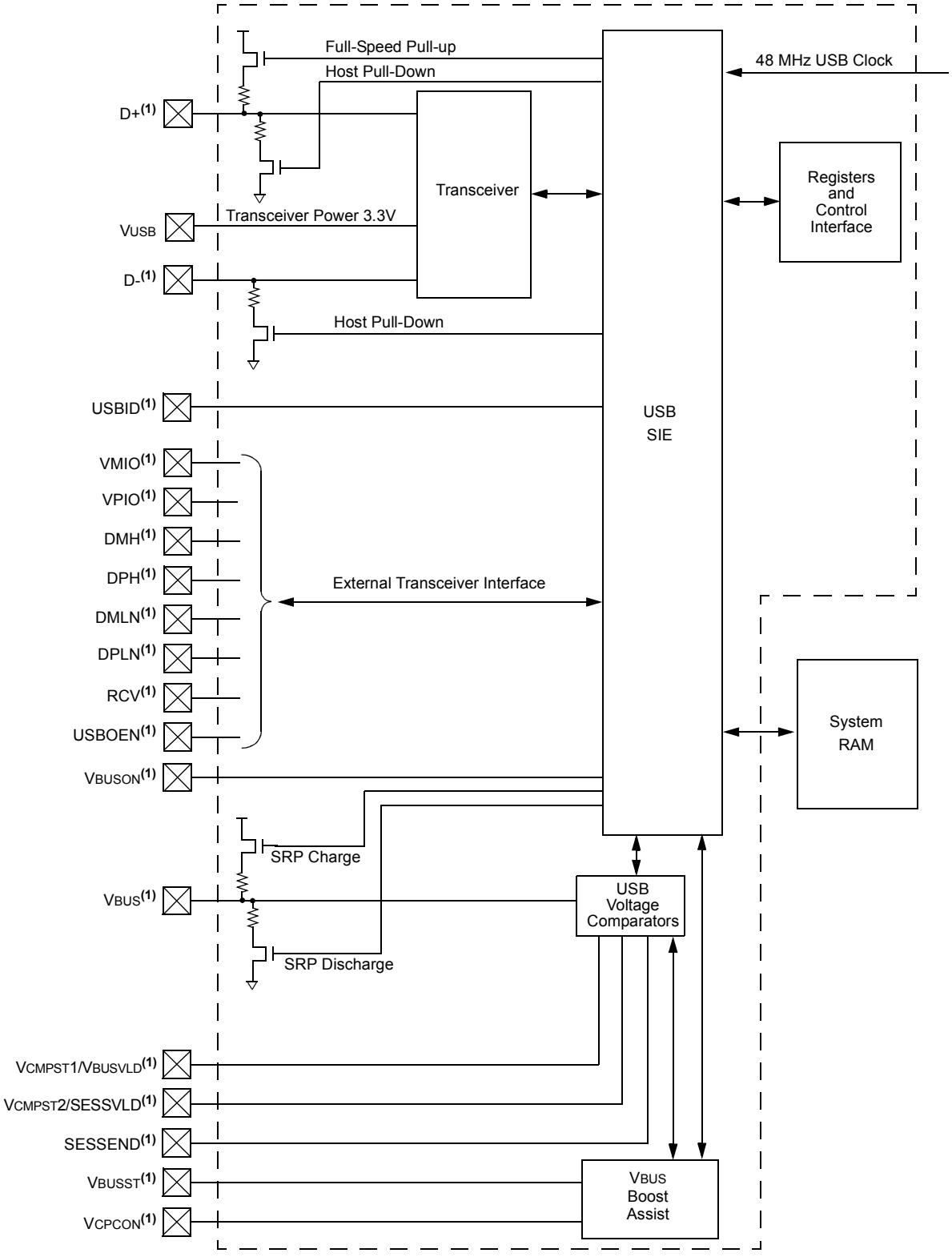
TABLE 18-1: CONTROLLER-CENTRIC DATA DIRECTION FOR USB HOST OR TARGET

USB Mode	Direction	
	RX	TX
Device	OUT or SETUP	IN
Host	IN	OUT or SETUP

This chapter presents the most basic operations needed to implement USB OTG functionality in an application. A complete and detailed discussion of the USB protocol and its OTG supplement are beyond the scope of this data sheet. It is assumed that the user already has a basic understanding of USB architecture and the latest version of the protocol.

Not all steps for proper USB operation (such as device enumeration) are presented here. It is recommended that application developers use an appropriate device driver to implement all of the necessary features. Microchip provides a number of application-specific resources, such as USB firmware and driver support. Refer to www.microchip.com/usb for the latest firmware and driver support.

FIGURE 18-1: USB OTG MODULE BLOCK DIAGRAM



Note 1: Pins are multiplexed with digital I/O and other device features.

REGISTER 18-15: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **LSTATEIE:** Line State Stable Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **SESENDIE:** B-Device Session End Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-Device VBUS Valid Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

20.1.5 ALRMVAL REGISTER MAPPINGS

REGISTER 20-8: ALMTHDY: ALARM MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 22-23: G1VSYNC: VERTICAL SYNCHRONIZATION CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VSLEN7	VSLEN6	VSLEN5	VSLEN4	VSLEN3	VSLEN2	VSLEN1	VSLEN0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VSST7	VSST6	VSST5	VSST4	VSST3	VSST2	VSST1	VSST0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **VSLEN<7:0>:** VSYNC Pulse-Width Configuration bits (in lines)
The DPVSOE bit (G1CON3<1>) must be set for the VSYNC signal to toggle; minimum value is 1.

bit 7-0 **VSST<7:0>:** VSYNC Start Delay Configuration bits (in lines)
This is the number of lines from the start of vertical blanking to the start of VSYNC active.

REGISTER 22-24: G1DBLCON: DISPLAY BLANKING CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VENST7	VENST6	VENST5	VENST4	VENST3	VENST2	VENST1	VENST0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HENST7	HENST6	HENST5	HENST4	HENST3	HENST2	HENST1	HENST0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **VENST<7:0>:** Vertical Blanking Start to First Displayed Line Configuration bits (in lines)
This is the number of lines from the start of vertical blanking to the first displayed line of a frame.

bit 7-0 **HENST<7:0>:** Horizontal Blanking Start to First Displayed Pixel Configuration bits (in DISPCLKs)
This is the number of GCLK cycles from the start of horizontal blanking to the first displayed pixel of each displayed line.

TABLE 30-4: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Operating Current (IDD)(2)						
DC20D	0.8	1.3	mA	-40°C	3.3V(3)	1 MIPS
DC20E	0.8	1.3	mA	+25°C		
DC20F	0.8	1.3	mA	+85°C		
DC23D	3.0	4.8	mA	-40°C	3.3V(3)	4 MIPS
DC23E	3.0	4.8	mA	+25°C		
DC23F	3.0	4.8	mA	+85°C		
DC24D	12.0	18	mA	-40°C	3.3V(3)	16 MIPS
DC24E	12.0	18	mA	+25°C		
DC24F	12.0	18	mA	+85°C		
DC31D	55	95	μA	-40°C	3.3V(3)	LPRC (31 kHz)
DC31E	55	95	μA	+25°C		
DC31F	135	225	μA	+85°C		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

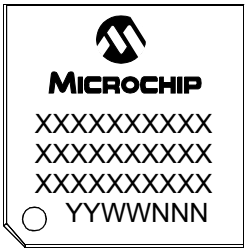
2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows: OSCI driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to VDD. MCLR = VDD; WDT and FSCM are disabled. CPU, SRAM, program memory and data memory are operational. No peripheral modules are operating and all of the Peripheral Module Disable (PMD) bits are set.

3: On-chip voltage regulator enabled (ENVREG tied to VDD). Brown-out Reset (BOR) is enabled.

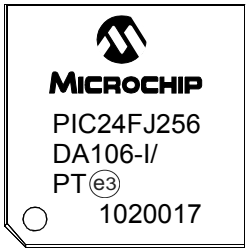
31.0 PACKAGING INFORMATION

31.1 Package Marking Information

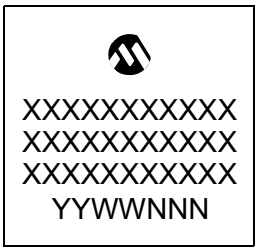
64-Lead TQFP (10x10x1 mm)



Example

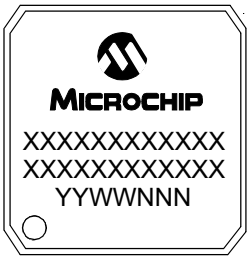


64-Lead QFN (9x9x0.9 mm)

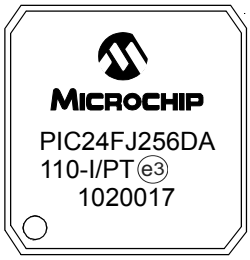


Example

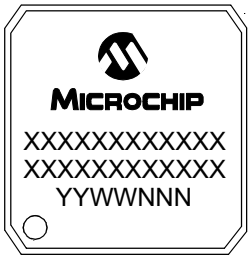
100-Lead TQFP (12x12x1 mm)



Example



121-BGA (10x10x1.1 mm)



Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

NOTES: