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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p34l1beabr

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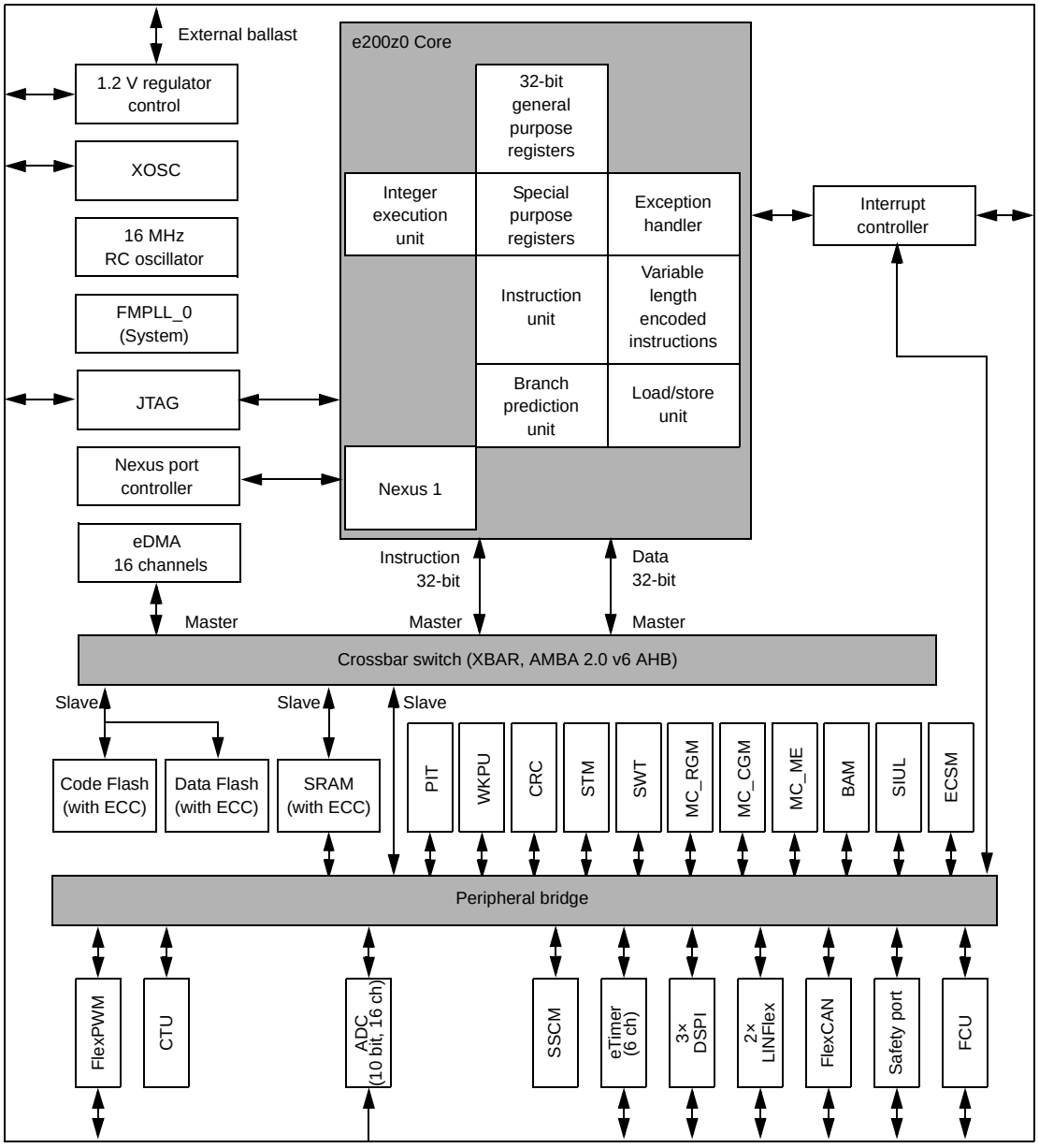
Figure 1. Block diagram (SPC560P40 full-featured configuration)



Legend:

ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System Integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

Table 4. SPC560P34/SPC560P40 series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Is the interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

Table 4. SPC560P34/SPC560P40 series block summary (continued)

Block	Function
Pulse width modulator (FlexPWM)	Contains four PWM submodules, each of which capable of controlling a single half-bridge power stage and two fault input channels
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR(1) and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events

1. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC560P34/SPC560P40:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module running at the same frequency as the e200z0h core
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency: 4–40 MHz
- Maximum output frequency: 64 MHz
- Voltage controlled oscillator (VCO)—frequency 256–512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the FMPLL to relock
- Frequency-modulated PLL
  - Modulation enabled/disabled through software
  - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency): programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.10 Main oscillator

The main oscillator provides these features:

- Input frequency range: 4–40 MHz
- Crystal input mode or oscillator input mode
- PLL reference

1.5.11 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

- 4 general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel usable as trigger for a DMA request

1.5.13 System timer module (STM)

The STM implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, a safety relay)
- Faults are latched into a register

The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers.

The NDI provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus Class 1 supports Static debug

1.5.29 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (*x*25 protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.30 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE test access port (TAP) interface 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS
  - IDCODE
  - EXTEST
  - SAMPLE
  - SAMPLE/PRELOAD
- 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
- 3 test data registers:
  - Bypass register
  - Boundary scan register (size parameterized to support a variety of boundary scan chain lengths)
  - Device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

1.5.31 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V/5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3	GPIO[49] — — EXT_TRG	SIUL — — CTU_0	I/O — — O	Slow	Medium	—	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3	GPIO[50] — — X[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	97
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] — — A[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	89
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] — — B[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	90
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] —	SIUL DSPI_0 FCU_0 —	I/O O O —	Slow	Medium	—	22
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 — — FAULT[1]	SIUL DSPI_0 — — FlexPWM_0	I/O O — — I	Slow	Medium	—	23
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3	GPIO[55] CS3 F[1] CS4	SIUL DSPI_1 FCU_0 DSPI_0	I/O O O O	Slow	Medium	17	26
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2 — CS5	SIUL DSPI_1 — DSPI_0	I/O O — O	Slow	Medium	14	21
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIUL FlexPWM_0 LIN_1 —	I/O O O —	Slow	Medium	8	15
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	53

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. LQFP thermal characteristics

Symbol	Parameter	Conditions	Typical value		Unit
			100-pin	64-pin	
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	63	57	°C/W
		Four layer board—2s2p	51	41	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board(2)	Four layer board—2s2p	33	22	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	15	13	°C/W
Ψ_{JB}	Junction-to-board, natural convection(4)	Operating conditions	33	22	°C/W
Ψ_{JC}	Junction-to-case, natural convection(5)	Operating conditions	1	1	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as RthJB or Theta-JB.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1: $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

3.6 Electromagnetic interference (EMI) characteristics

Table 13. EMI testing specifications

Symbol	Parameter	Conditions	Clocks	Frequency	Level (Typ)	Unit
V_{EME}	Radiated emissions	V_{DD} = 5.0 V; T_A = 25 °C Other device configuration, test conditions and EM testing per standard IEC61967-2	f_{OSC} = 8 MHz f_{CPU} = 64 MHz No PLL frequency modulation	150 kHz–150 MHz	11	dBµV
				150–1000 MHz	13	
				IEC level	M	—
			f_{OSC} = 8 MHz f_{CPU} = 64 MHz ±4% PLL frequency modulation	150 kHz–150 MHz	8	dBµV
				150–1000 MHz	12	
				IEC level	N	—
		V_{DD} = 3.3 V; T_A = 25 °C Other device configuration, test conditions and EM testing per standard IEC61967-2	f_{OSC} = 8 MHz f_{CPU} = 64 MHz No PLL frequency modulation	150 kHz–150 MHz	9	dBµV
				150–1000 MHz	12	
				IEC level	M	—
			f_{OSC} = 8 MHz f_{CPU} = 64 MHz ±4% PLL frequency modulation	150 kHz–150 MHz	7	dBµV
				150–1000 MHz	12	
				IEC level	N	—

3.7 Electrostatic discharge (ESD) characteristics

Table 14. ESD ratings(1),(2)

Symbol		Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	S R	Electrostatic discharge (Human Body Model)	—	2000	V
$V_{ESD(CDM)}$	S R	Electrostatic discharge (Charged Device Model)	—	750 (corners)	V
				500 (other)	

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The internal voltage regulator requires an external NPN ballast, approved ballast list availbale in *Table 15*, to be connected as shown in *Figure 10*. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins to less than L_{Reg}. (refer to *Table 16*).

Table 15. Approved NPN ballast components

Part	Manufacturer	Approved derivatives(1)
BC817	Infineon	BC817-16; BC817-25; BC817SU
	NXP	BC817-16; BC817-25
BCP56	ST	BCP56-16
	Infineon	BCP56-10; BCP56-16
	ON Semi	BCP56-10
	NXP	BCP56-10; BCP56-16

1. For automotive applications please check with the appropriate transistor vendor for automotive grade certification

Table 16. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	BJT from *Table 15*. Three capacitors (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	—	µF
				BJT BC817, one capacitance of 22 µF	14.3	22	—	µF
R_{REG}	SR	—	Resulting ESR of either one or all three C_{DEC1}	Absolute maximum value between 100 kHz and 10 MHz	—	—	45	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	Four capacitances (i.e. X7R or X8R capacitors) with nominal value of 440 nF	1200	1760	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on VDD_HV_REG	Three capacitors (i.e. X7R or X8R capacitors) with nominal value of 10 µF; C_{DEC3} has to be equal or greater than C_{DEC1}	19.5	30	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins	—	—	—	5	nH

3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 23*.

Table 23. I/O supply segment

Package	Supply segment				
	1	2	3	4	5
LQFP100	pin15–pin26	pin27–pin46	pin51–pin61	pin64–pin86	pin89–pin10
LQFP64	pin8–pin17	pin18–pin30	pin33–pin38	pin41–pin54	pin57–pin5

Table 24. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	

Table 26. Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{OSC}	SR	—	Oscillator frequency		4	40	MHz
g_m	—	P	Transconductance		4	20	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin		1	—	V
t_{OSCSU}	—	T	Start-up time(1),(2)		8	—	ms
C_L	CC	T	XTAL load capacitance(3)	4 MHz	5	30	pf
		T		8 MHz	5	26	
		T		12 MHz	5	23	
		T		16 MHz	5	19	
		T		20 MHz	5	16	
		T		40 MHz	5	8	

1. The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL
3. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

Table 27. Input clock characteristics

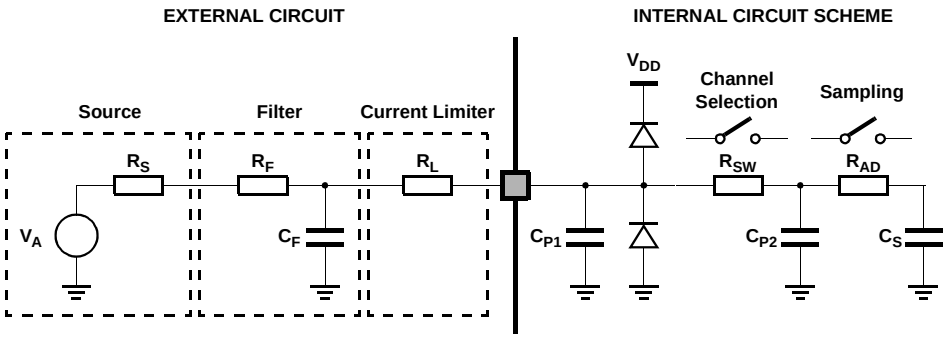
Symbol		Parameter	Value			Unit
			Min	Typ	Max	
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	64	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.12 FMPLL electrical characteristics

Table 28. FMPLL electrical characteristics

Symbol	C	Parameter	Conditions(1)	Value		Unit
				Min	Max	
$f_{ref\_crystal}$ f_{ref_ext}	D	PLL reference frequency range(2)	Crystal reference	4	40	MHz
f_{PLLIN}	D	Phase detector input frequency range (after pre-divider)	—	4	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	16	64	MHz

Figure 16. Input equivalent circuit



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW}: Channel selection switch impedance
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1} and C_{P2})
C_S: Sampling capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch closed).

Figure 17. Transient behavior during sampling phase

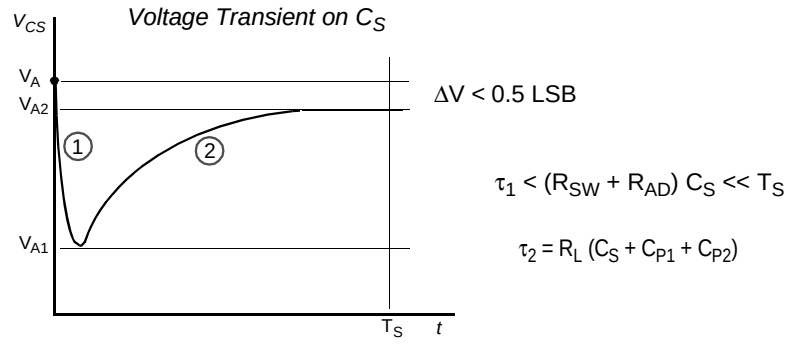


Figure 23. JTAG test access port timing

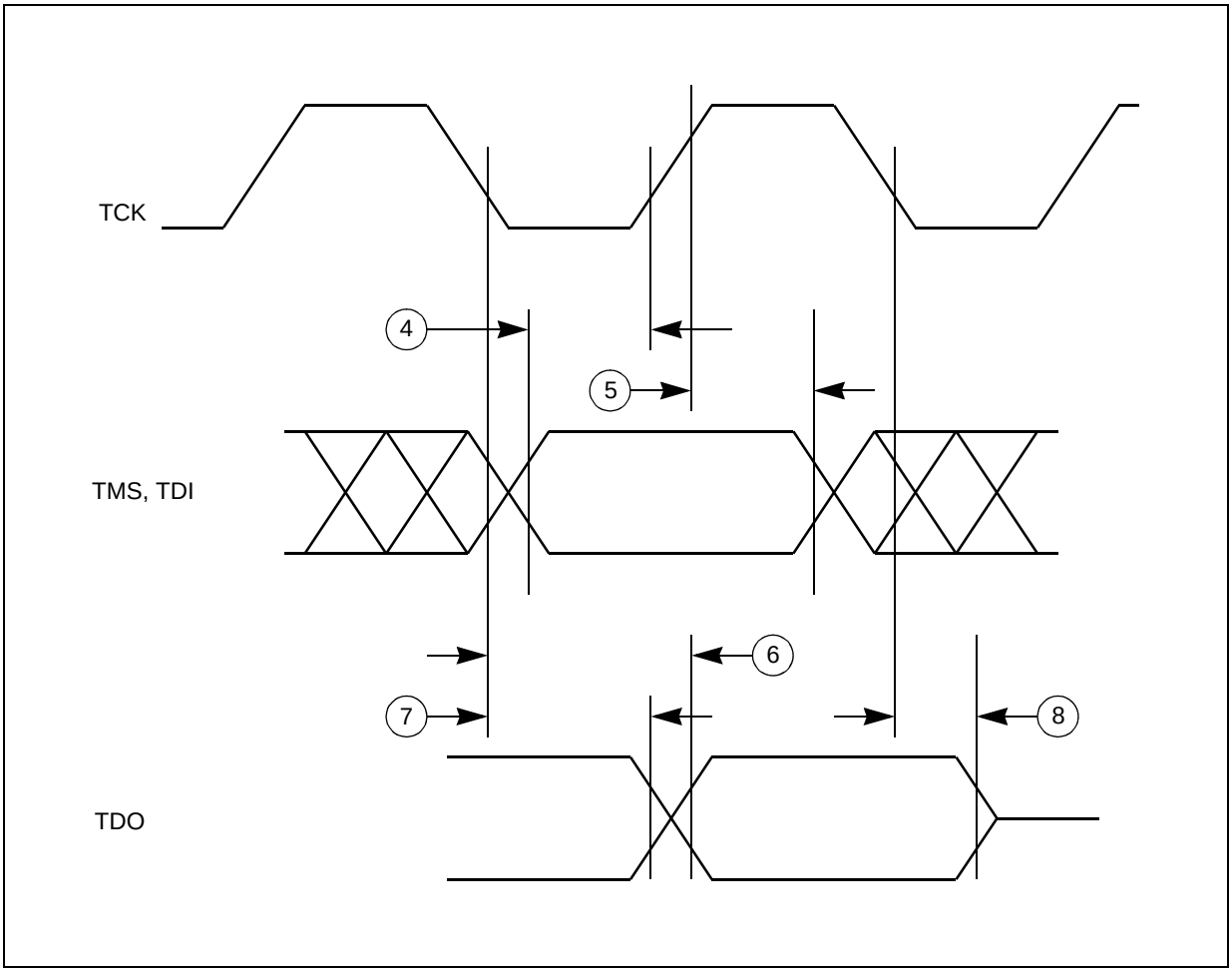
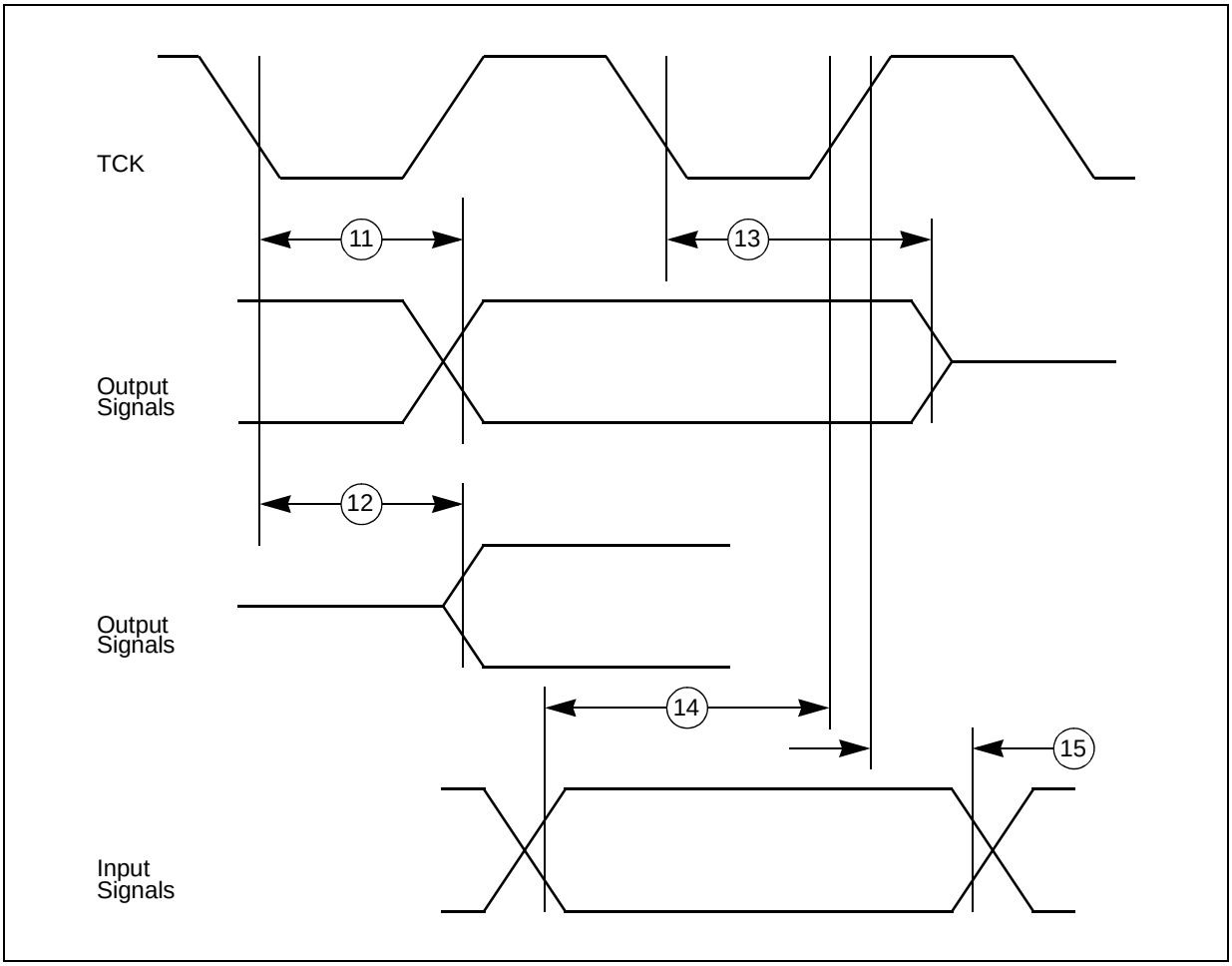


Figure 24. JTAG boundary scan timing



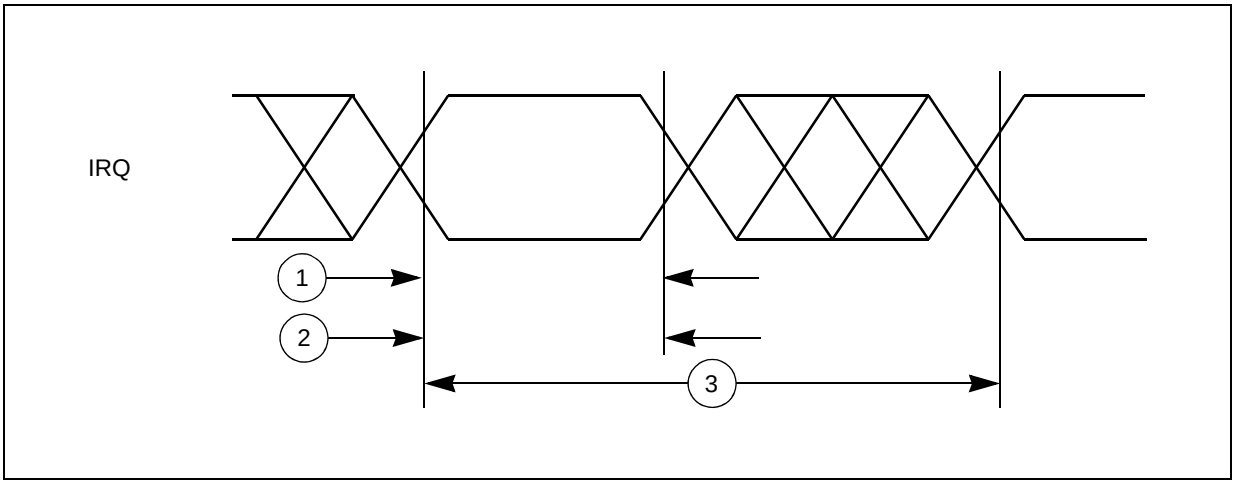
3.17.3 Nexus timing

Table 39. Nexus debug port timing(1)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	4(2)	—	—	t_{CYC}
2	t_{NTDIS}	CC	D	TDI data setup time	5	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	5	—	—	ns
3	t_{NTDIH}	CC	D	TDI data hold time	25	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	25	—	—	ns
4	t_{TDOV}	CC	D	TCK low to TDO data valid	10	—	20	ns
5	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	—	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. Lower frequency is required to be fully compliant to standard.

Figure 28. External interrupt timing



3.17.5 DSPI timing

Table 41. DSPI timing(1)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	60	—	ns
					Slave (MTFE = 0)	60	—	
2	t_{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	26	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	30	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT high impedance or invalid	—	16	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	35	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	35	—	
					Master (MTFE = 1, CPHA = 1)	35	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	–5	—	

Revision history

Table 45. Document revision history

Date	Revision	Changes
01-Sep-2009	1	Initial release.
21-May-2010	2	Editorial updates Updated the following items in the “SPC560P34/SPC560P40 device comparison” table: – The heading – The “SRAM” row – The “FlexCAN” row – The “CTU” row – The “FlexPWM” row – The “LINFlex” row – The “DSPI” row – The “Nexus” row Updated the “SPC560P34/SPC560P40 device configuration difference” table: – Editorial updates – Added the “CTU” row – Deleted the “temperature” row – Swapped the content of Airbag and Full Featured cells Added the “Wakeup unit” block in the SPC560P34/SPC560P40 block diagram Updated the “Absolute Maximum Ratings“ table Updated the “Recommended operating conditions (5.0 V)“ table Updated the “Recommended operating conditions (3.3 V)“ table Updated the “Thermal characteristics for 100-pin LQFP“ table: – Ψ_{JT}: changed the typical value Updated the “EMI testing specifications“ table: replaced all values in “Level (Max)“ column with TBD Updated the “Electrical characteristics“ section: – Added the “Introduction” section – Added the “Parameter classification“ section – Added the “NVUSRO register“ section – Added the “Power supplies constraints (–0.3 V ≤ $V_{DD\_HV\_IOx}$ ≤ 6.0 V)” figure – Added the “Independent ADC supply (–0.3 V ≤ $V_{DD\_HV\_REG}$ ≤ 6.0 V)“ figure – Added the “Power supplies constraints (3.0 V ≤ $V_{DD\_HV\_IOx}$ ≤ 5.5 V)“ figure – Added the “Independent ADC supply (3.0 V ≤ $V_{DD\_HV\_REG}$ ≤ 5.5 V)“ figure Updated the “Power management electrical characteristics” section Updated the “Power Up/Down sequencing” section Updated the “DC electrical characteristics“ section – Deleted the “NVUSRO register” section – Updated the “DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)“ section: – Deleted all rows concerning $\overline{\text{RESET}}$ – Deleted “I_{VPP}“ row – Added the max value for C_{IN}