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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p34l1cefby

Contents

Table 4. SPC560P34/SPC560P40 series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Is the interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

The flash memory module provides the following features:

- As much as 320 KB flash memory
  - 6 blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 128 KB) code flash memory
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash memory
  - Full Read-While-Write (RWW) capability between code flash memory and data flash memory
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: no wait-state for buffer hits, 2 wait-states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page sizes
  - Code flash memory: 128 bits (4 words)
  - Data flash memory: 32 bits (1 word)
- ECC with single-bit correction, double-bit detection for data integrity
  - Code flash memory: 64-bit ECC
  - Data flash memory: 32-bit ECC
- Embedded hardware program and erase algorithm
- Erase suspend and program abort
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 Static random access memory (SRAM)

The SPC560P34/SPC560P40 SRAM module provides up to 20 KB of general-purpose memory.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM from any master
- Up to 20 KB general purpose SRAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: no wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back-to-back with a read to same memory block

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

- 4 general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel usable as trigger for a DMA request

1.5.13 System timer module (STM)

The STM implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, a safety relay)
- Faults are latched into a register

platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC560P34/SPC560P40.

The sources of the ECC errors are:

- Flash memory
- SRAM

1.5.19 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.20 Controller area network (FlexCAN)

The SPC560P34/SPC560P40 MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures. For pin signal descriptions, please refer to *Table 7*.

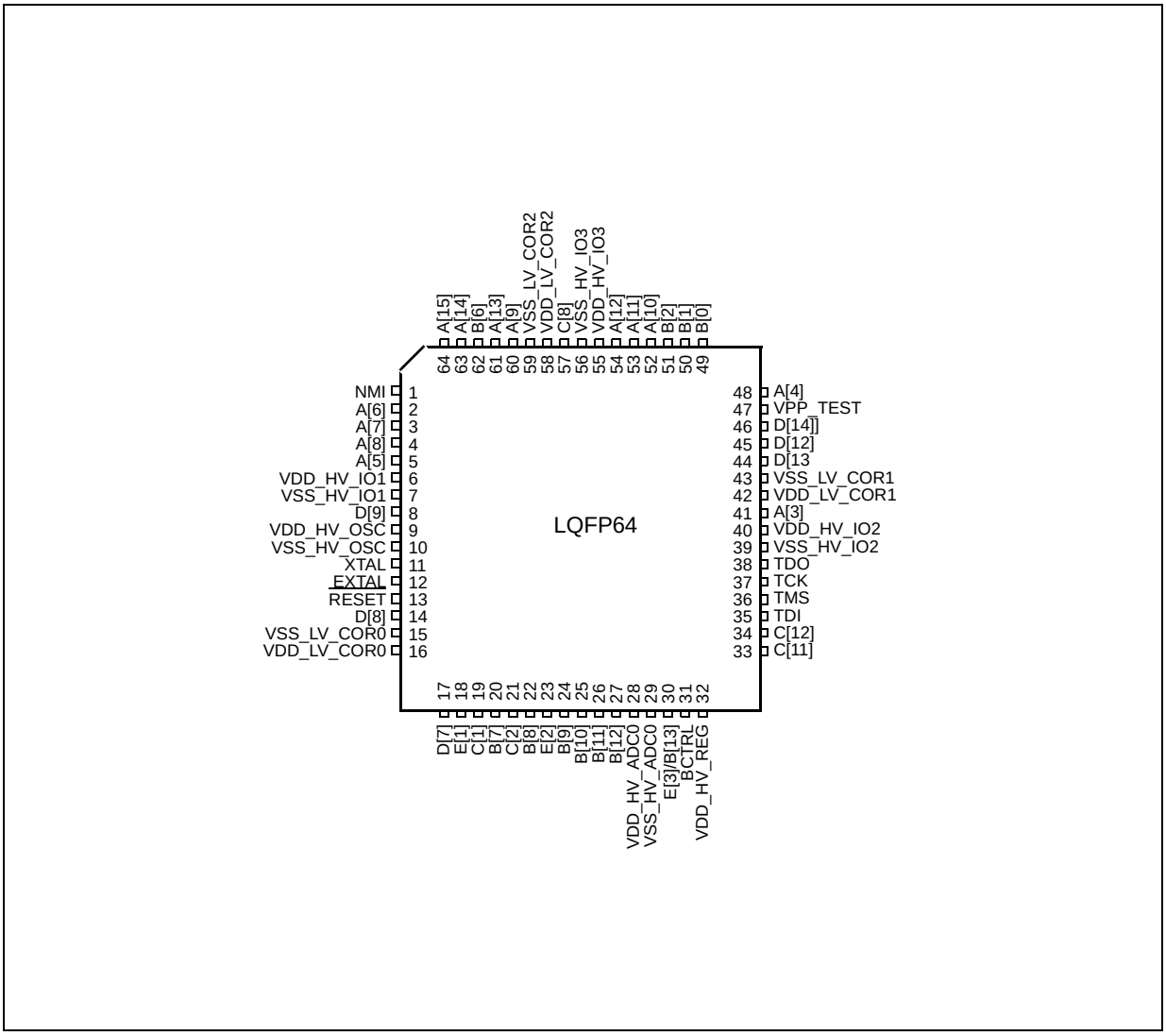


Figure 2. 64-pin LQFP pinout – Full featured configuration (top view)

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK A[0] A[2] EIRQ[10]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O O I	Slow	Medium	53	82
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT A[2] B[2] EIRQ[11]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O O O O I	Slow	Medium	54	83
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[13] — B[2] — SIN FAULT[0] EIRQ[12]	SIUL — FlexPWM_0 — DSPI_2 FlexPWM_0 SIUL	I/O — O — I I I	Slow	Medium	61	95
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD — — EIRQ[13]	SIUL Safety Port_0 — — SIUL	I/O O — — I	Slow	Medium	63	99
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — — — RXD EIRQ[14]	SIUL — — — Safety Port_0 SIUL	I/O — — — I I	Slow	Medium	64	100
Port B (16-bit)									
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD — DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	49	76
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] — — DEBUG[1] RXD EIRQ[16]	SIUL — — SSCM FlexCAN_0 SIUL	I/O — — — I I	Slow	Medium	50	77

3 Electrical characteristics

3.1 Introduction

This section contains device electrical characteristics as well as temperature and power considerations.

This microcontroller contains input protection against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down resistors, which are provided by the device for most general purpose pins.

The following tables provide the device characteristics and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution:

All of the following parameter values can vary depending on the application and must be confirmed during silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 10. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
$V_{DD\_HV\_ADC0}$	SR	5.0 V ADC_0 supply and high reference voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG}$ – 0.1	—	
$V_{SS\_HV\_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(3),(4)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(3),(4)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 60 MHz	–40	125	°C
			f_{CPU} = 64 MHz	–40	105	°C

1. Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 100$ mV.
3. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
4. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.
   – $V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.
   – $V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_RECORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Table 11. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V

Table 15. Approved NPN ballast components

Part	Manufacturer	Approved derivatives(1)
BC817	Infineon	BC817-16; BC817-25; BC817SU
	NXP	BC817-16; BC817-25
BCP56	ST	BCP56-16
	Infineon	BCP56-10; BCP56-16
	ON Semi	BCP56-10
	NXP	BCP56-10; BCP56-16

1. For automotive applications please check with the appropriate transistor vendor for automotive grade certification

Table 16. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	BJT from *Table 15*. Three capacitors (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	—	µF
				BJT BC817, one capacitance of 22 µF	14.3	22	—	µF
R_{REG}	SR	—	Resulting ESR of either one or all three C_{DEC1}	Absolute maximum value between 100 kHz and 10 MHz	—	—	45	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	Four capacitances (i.e. X7R or X8R capacitors) with nominal value of 440 nF	1200	1760	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on VDD_HV_REG	Three capacitors (i.e. X7R or X8R capacitors) with nominal value of 10 µF; C_{DEC3} has to be equal or greater than C_{DEC1}	19.5	30	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins	—	—	—	5	nH

3.10.2 DC electrical characteristics (5 V)

Table 19 gives the DC electrical characteristics at 5 V (4.5 V < $V_{DD\_HV\_IOx}$ < 5.5 V, NVUSRO[PAD3V5V] = 0).

Table 19. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.4(1)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.4 (1)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 14 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –14 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 24. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.11 Main oscillator electrical characteristics

The SPC560P34/SPC560P40 provides an oscillator/resonator driver.

Table 25. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{OSC}	SR	—	Oscillator frequency		4	40	MHz
g_m	—	P	Transconductance		6.5	25	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin		1	—	V
t_{OSCSU}	—	T	Start-up time[1],[2]		8	—	ms
C_L	CC	T	XTAL load capacitance[3]	4 MHz	5	30	pf
		T		8 MHz	5	26	
		T		12 MHz	5	23	
		T		16 MHz	5	19	
		T		20 MHz	5	16	
		T		40 MHz	5	8	

1. The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL
3. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

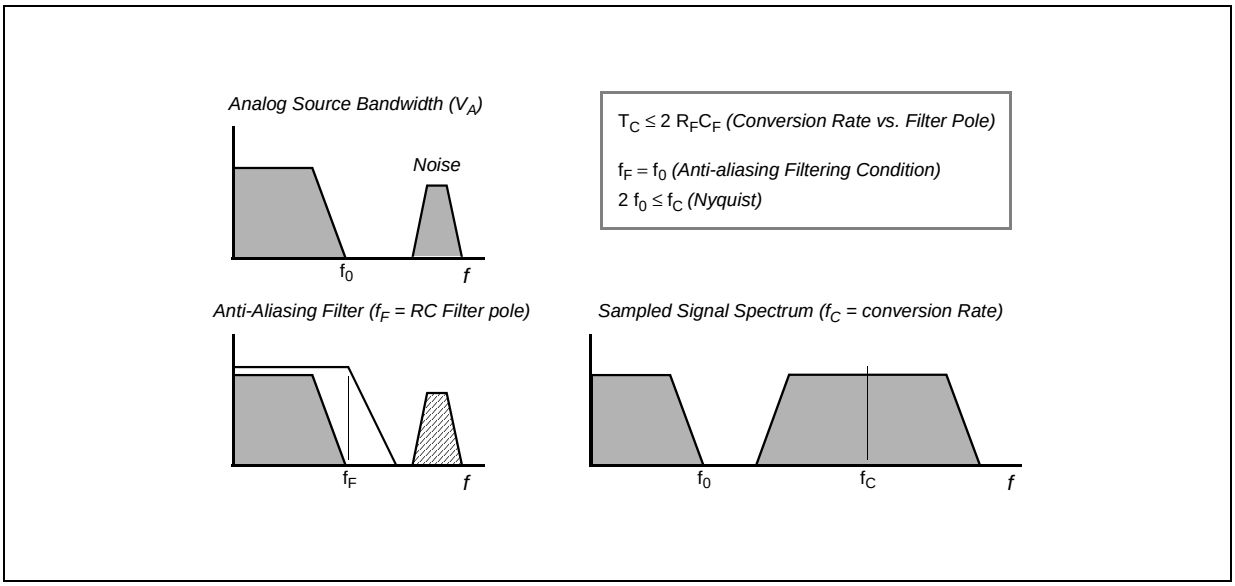
Table 28. FMPLL electrical characteristics (continued)

Symbol	C	Parameter		Conditions[1]	Value		Unit
					Min	Max	
f_{FREE}	P	Free-running frequency		Measured using clock division—typically /16	20	150	MHz
t_{CYC}	D	System clock period		—	—	1 / f_{SYS}	ns
f_{LORL}	D	Loss of reference frequency window[3]		Lower limit	1.6	3.7	MHz
f_{LORH}	D			Upper limit	24	56	
f_{SCM}	D	Self-clocked mode frequency[4],[5]		—	20	150	MHz
C_{JITTER}	T	CLKOUT period jitter[6],[7],[8],[9]	Short-term jitter[10]	f_{SYS} maximum	–4	4	% f_{CLKOUT}
			Long-term jitter (average over 2 ms interval)	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 64 MHz, 4000 cycles	—	10	ns
t_{lpll}	D	PLL lock time[11], [12]		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	–6	6	% f_{SYS}
f_{UL}	D	Frequency un-LOCK range		—	–18	18	% f_{SYS}
f_{CS}	D	Modulation depth		Center spread	±0.25	±4.0 (13)	% f_{SYS}
f_{DS}	D			Down spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency[14]		—	—	70	kHz

1. $V_{DD\_LV\_CORx}$ = 1.2 V ±10%; V_{SS} = 0 V; T_A = –40 to 125 °C, unless otherwise specified
2. Considering operation with PLL not bypassed.
3. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
4. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
5. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
6. This value is determined by the crystal manufacturer and board design.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DD\_LV\_COR0}$ and $V_{SS\_LV\_COR0}$ and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
8. Proper PC board layout procedures must be followed to achieve specifications.
9. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
10. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
12. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
13. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
14. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

Figure 18. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 2048 \bullet C_S$$

4. C_L includes device and package capacitance (C_{PKG} < 5 pF).
5. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}$/2)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing

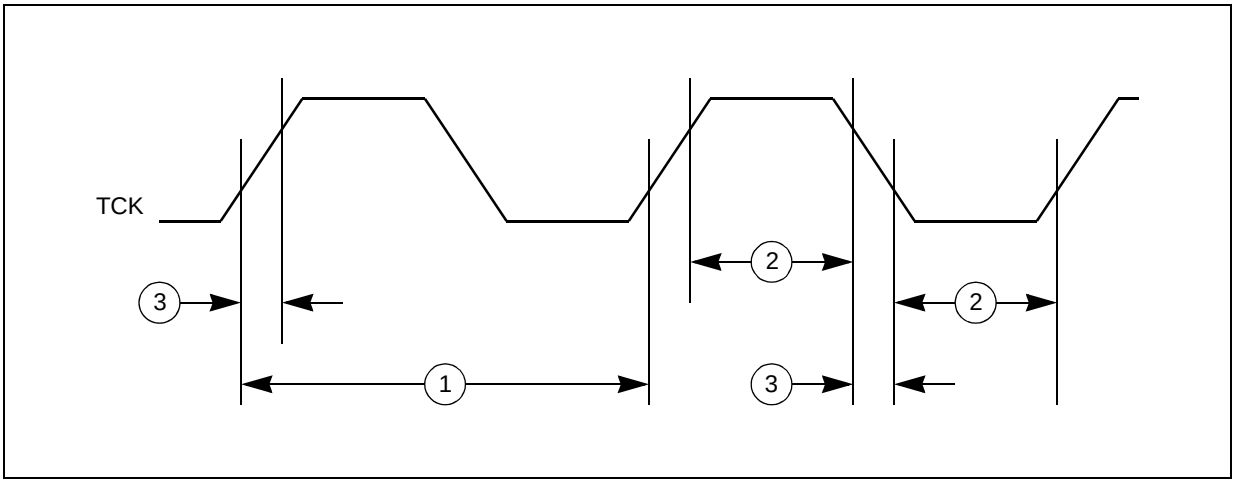
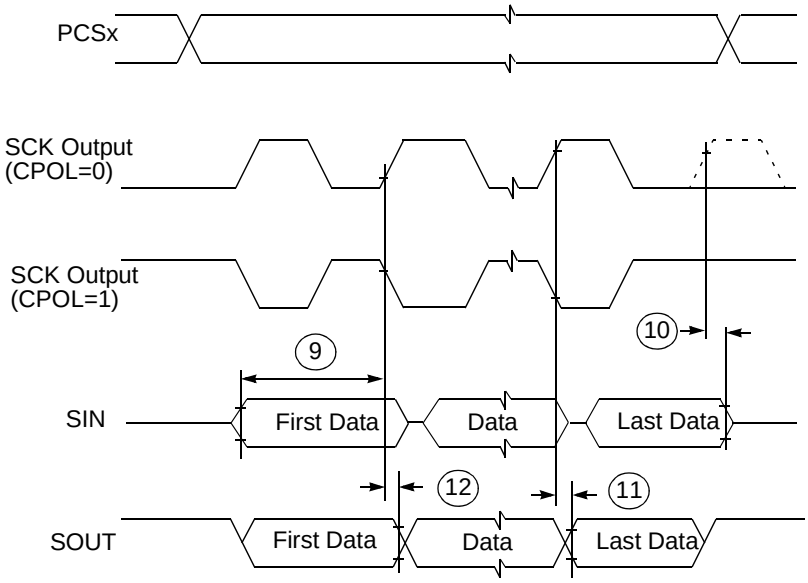
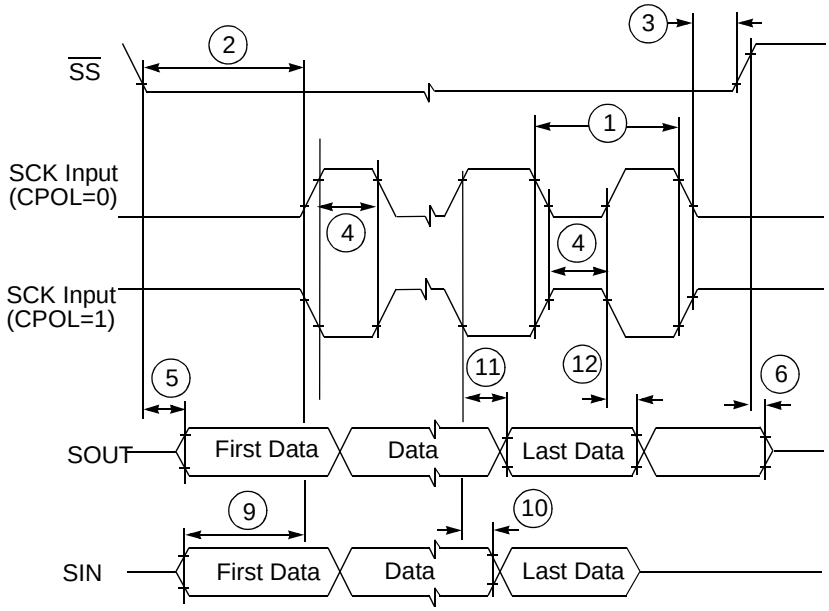


Figure 34. DSPI modified transfer format timing – Master, CPHA = 1



Note: Numbers shown reference *Table 41*.

Figure 35. DSPI modified transfer format timing – Slave, CPHA = 0



Note: Numbers shown reference *Table 41*.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2.2 LQFP64 mechanical outline drawing

Figure 39. LQFP64 package mechanical drawing

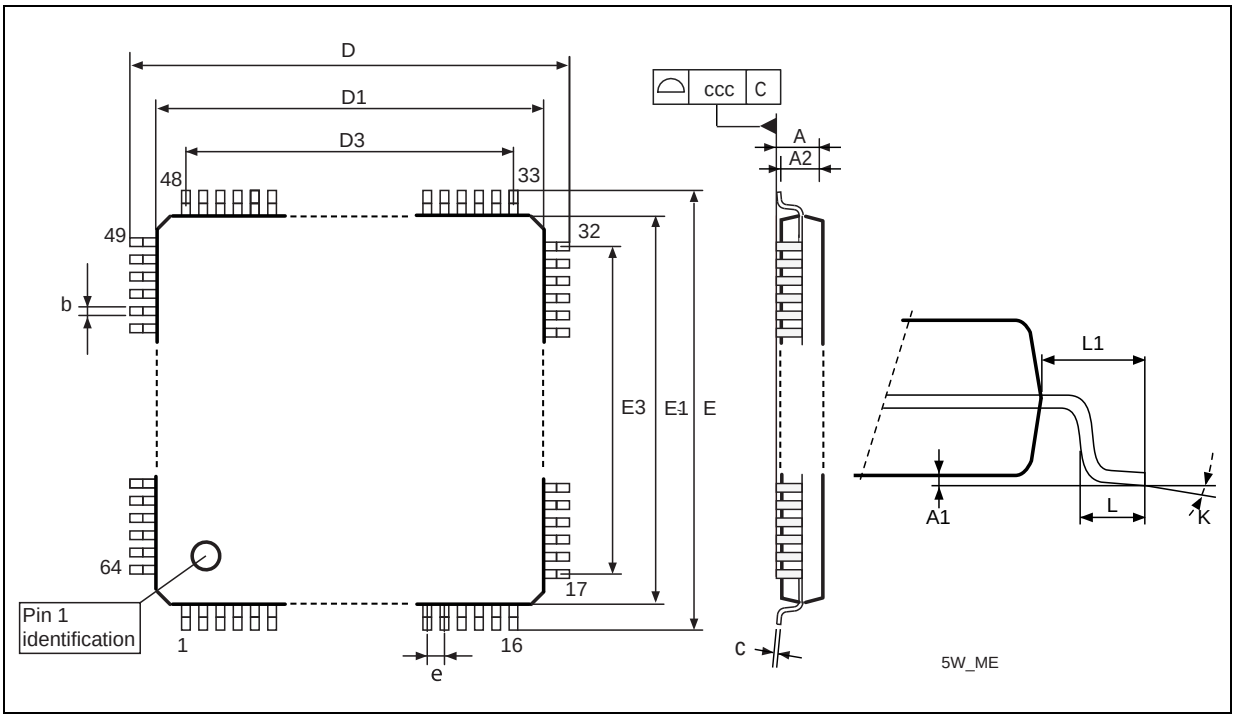
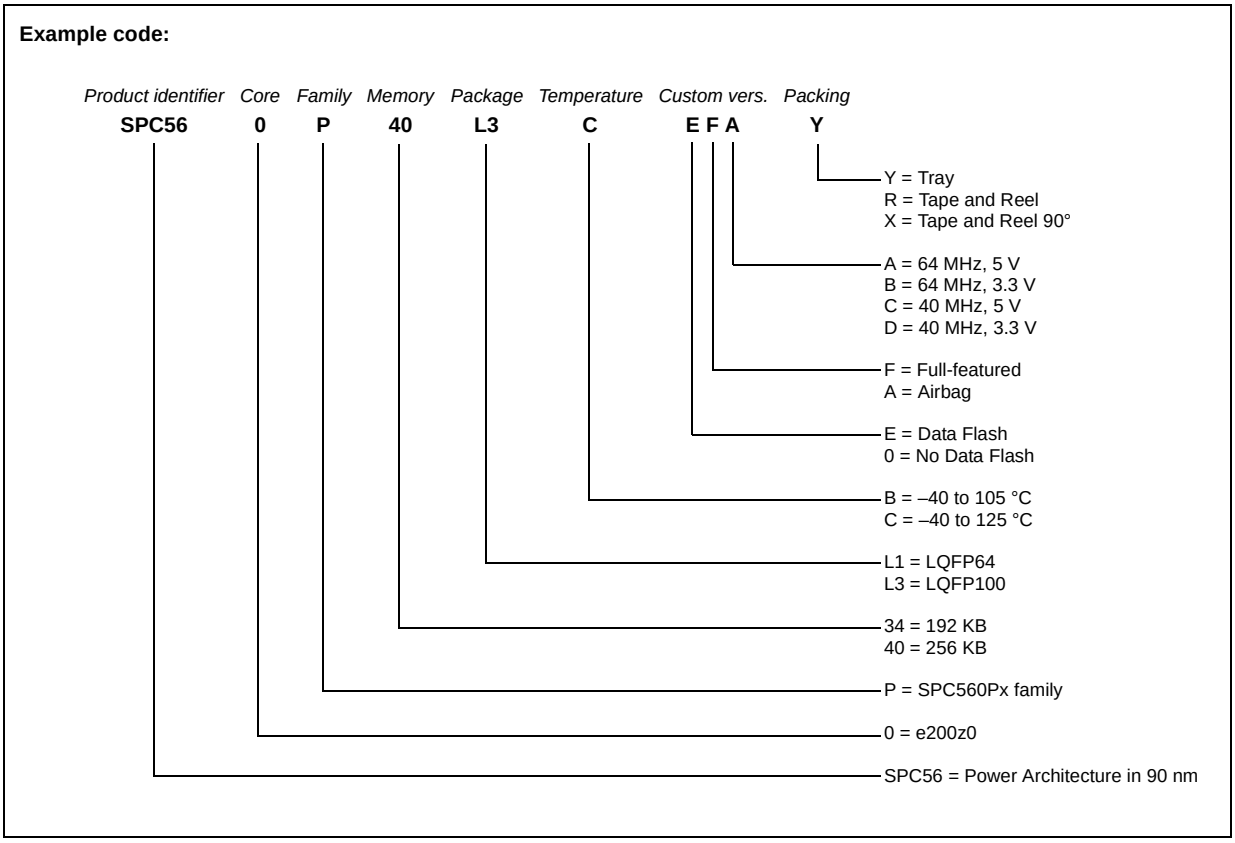


Table 43. LQFP64 package mechanical data

Symbol	Dimensions					
	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.6	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.0059
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	—	0.2	0.0035	—	0.0079
D	11.8	12	12.2	0.4646	0.4724	0.4803
D1	9.8	10	10.2	0.3858	0.3937	0.4016
D3	—	7.5	—	—	0.2953	—
E	11.8	12	12.2	0.4646	0.4724	0.4803
E1	9.8	10	10.2	0.3858	0.3937	0.4016
E3	—	7.5	—	—	0.2953	—
e	—	0.5	—	—	0.0197	—
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1	—	1	—	—	0.0394	—

5 Ordering information

Figure 40. Commercial product code structure



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