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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	64
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p34l3cefay

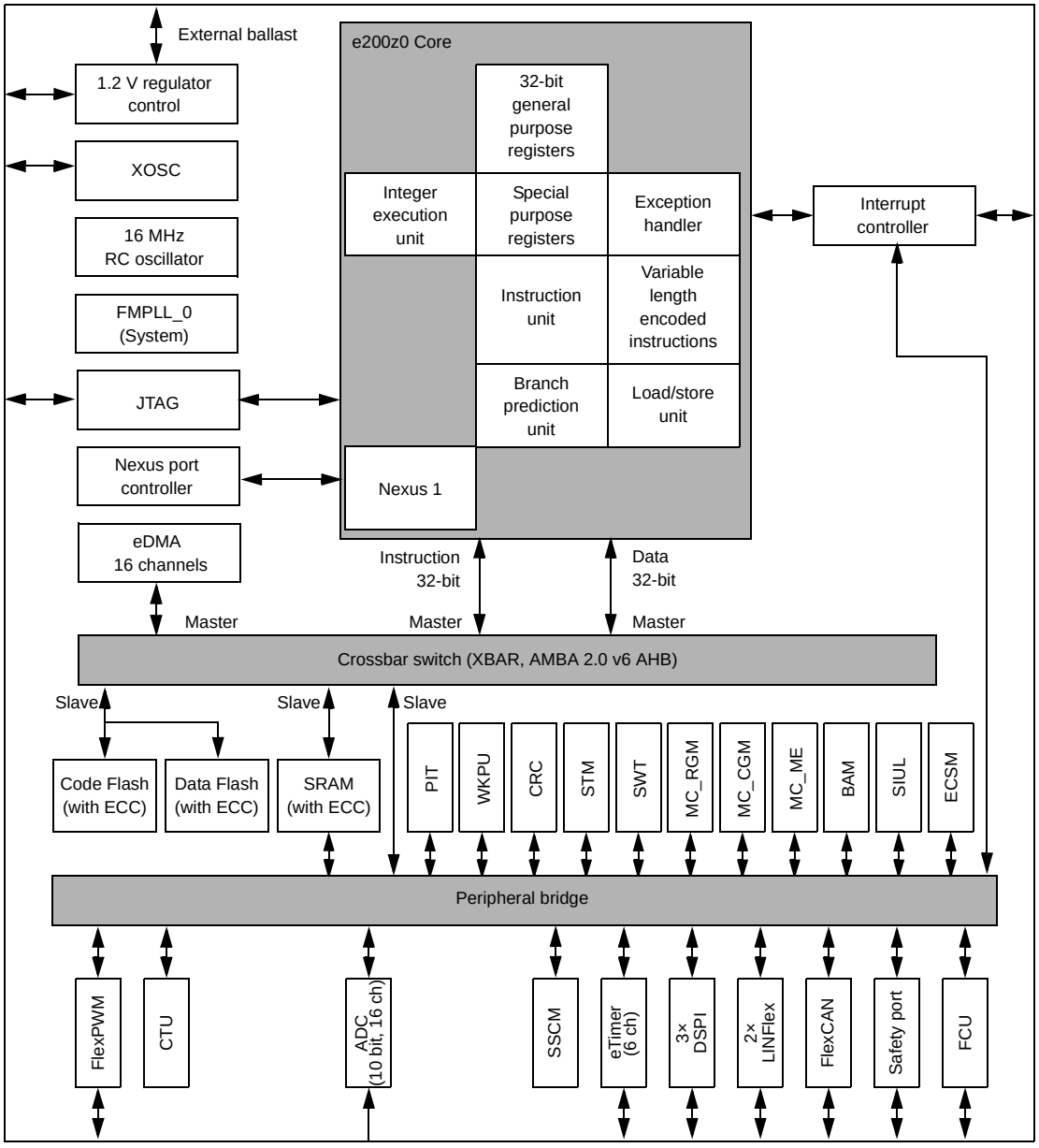
Table 2. SPC560P34/SPC560P40 device comparison (continued)

Feature		SPC560P34 Full-featured	SPC560P40 Full-featured
eDMA (enhanced direct memory access) channels		16	
FlexCAN (controller area network)		1(1)	2(1),(2)
Safety port		No	Yes (via second FlexCAN module)
FCU (fault collection unit)		Yes	
CTU (cross triggering unit)		Yes	Yes
eTimer		1 (16-bit, 6 channels)	
FlexPWM (pulse-width modulation) channels		8 (capture capabity not supported)	8 (capture capability not supported)
Analog-to-digital converter (ADC)		1 (10-bit, 16 channels)	
LINFlex		2 (1 × Master/Slave, 1 × Master only)	2 (1 × Master/Slave, 1 × Master only)
DSPI (deserial serial peripheral interface)		2	3
CRC (cyclic redundancy check) unit		Yes	
Junction temperature sensor		No	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Nexus Class 1)	
Supply	Digital power supply(3)	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		LQFP64 LQFP100	
Temperature	Standard ambient temperature	–40 to 125 °C	

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a safety port with a bit rate as high as 8 Mbit/s at 64 MHz.
3. The different supply voltages vary according to the part number ordered.

SPC560P34/SPC560P40 is available in two configurations having different features: Full-featured and airbag. *Table 3* shows the main differences between the two versions of the SPC560P40 MCU.

Figure 1. Block diagram (SPC560P40 full-featured configuration)



Legend:

ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System Integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

The crossbar provides the following features:

- 3 master ports:
  - e200z0 core complex instruction port
  - e200z0 core complex Load/Store Data port
  - eDMA
- 3 slave ports:
  - Flash memory (Code and Data)
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels.

The eDMA module provides the following features:

- 16 channels support independent 8-, 16- or 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to either post-increment or to remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, FlexPWM, eTimer and CTU
- Programmable DMA channel multiplexer allows assignment of any DMA source to any available DMA channel with as many as 30 request sources
- eDMA abort operation through software

1.5.4 Flash memory

The SPC560P34/SPC560P40 provides 320 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module is interfaced to the system bus by a dedicated flash memory controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit wide prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring two wait-states.

1.5.31 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V/5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures. For pin signal descriptions, please refer to *Table 7*.

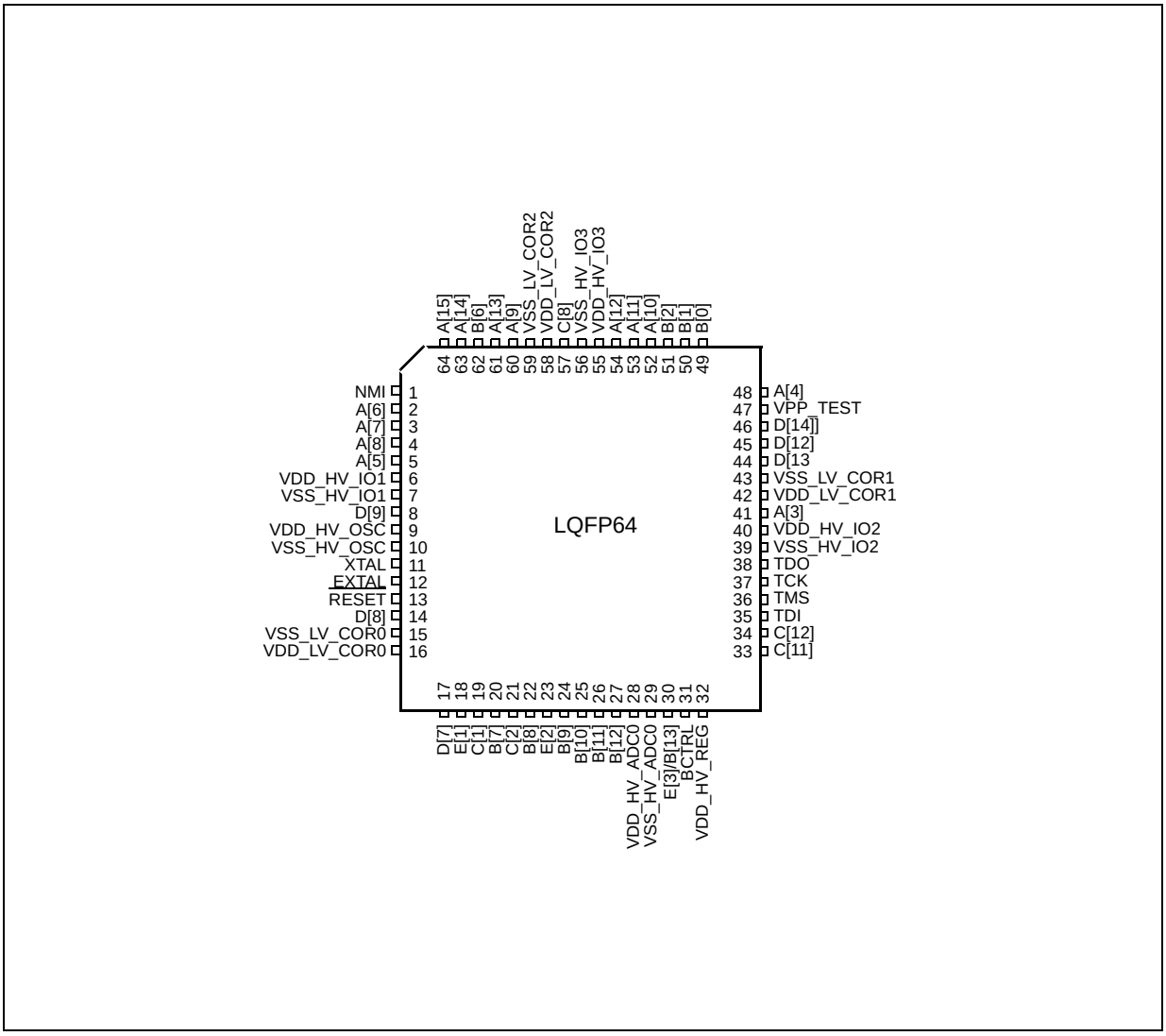


Figure 2. 64-pin LQFP pinout – Full featured configuration (top view)

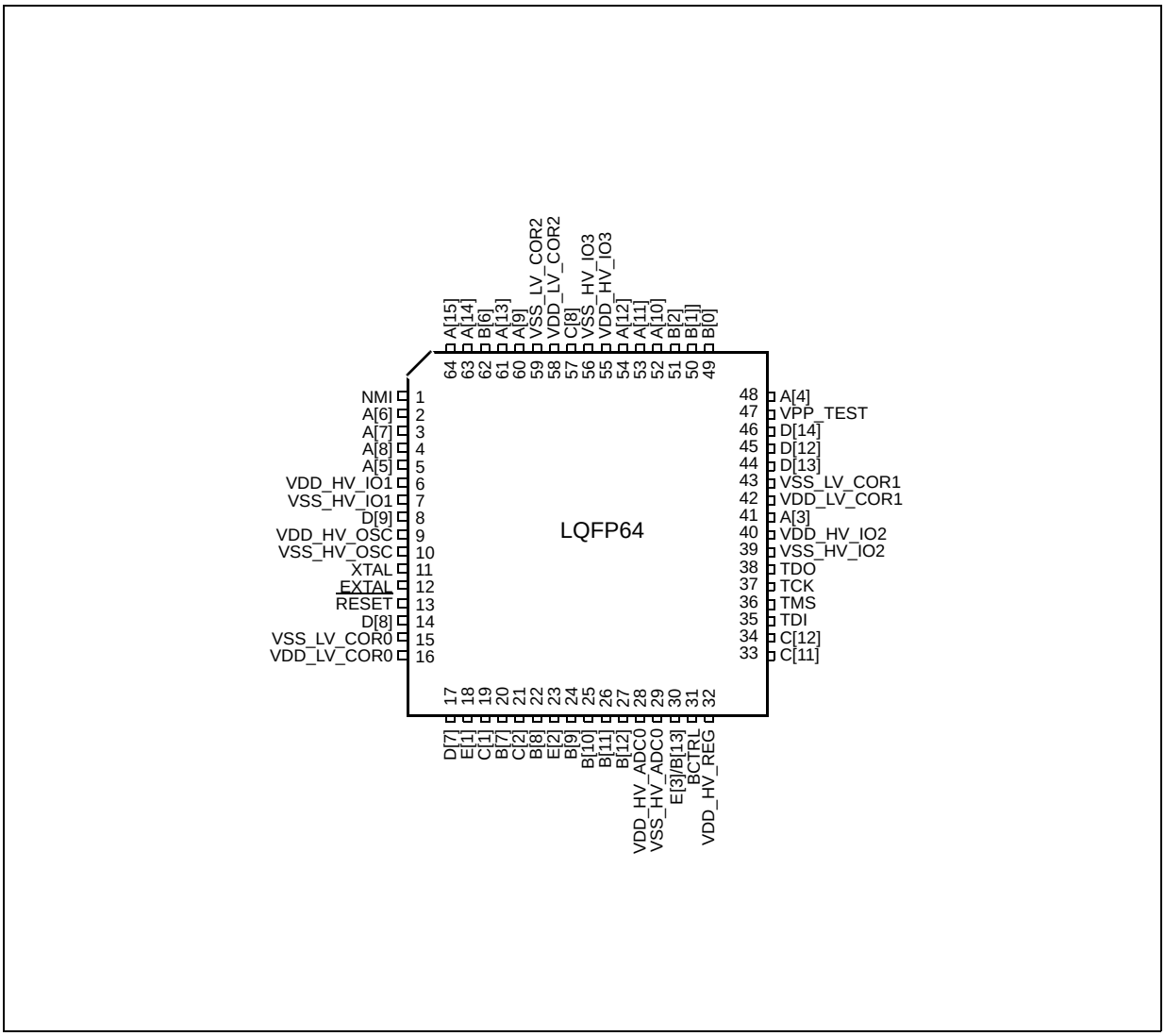


Figure 3. 64-pin LQFP pinout – Airbag configuration (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC560P34/SPC560P40 devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC560P34/SPC560P40 devices.

Table 5. Supply pins

Supply		Pin	
Symbol	**Description**	**64-pin**	**100-pin**
VREG control and power supply pins. Pins available on 64-pin and 100-pin packages			
BCTRL	Voltage regulator external NPN ballast base control pin	31	47
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	32	50
ADC_0 reference and supply voltage. Pins available on 64-pin and 100-pin packages			
$V_{DD\_HV\_ADC0}$(1)	ADC_0 supply and high reference voltage	28	39
$V_{SS\_HV\_ADC0}$	ADC_0 ground and low reference voltage	29	40
Power supply pins (3.3 V or 5.0 V). Pins available on 64-pin and 100-pin packages			
$V_{DD\_HV\_IO1}$	Input/output supply voltage	6	13
$V_{SS\_HV\_IO1}$	Input/output ground	7	14
$V_{DD\_HV\_IO2}$	Input/output supply voltage and data Flash memory supply voltage	40	63
$V_{SS\_HV\_IO2}$	Input/output ground and Flash memory HV ground	39	62
$V_{DD\_HV\_IO3}$	Input/output supply voltage and code Flash memory supply voltage	55	87
$V_{SS\_HV\_IO3}$	Input/output ground and code Flash memory HV ground	56	88
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	9	16
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	10	17
Power supply pins (1.2 V). Pins available on 64-pin and 100-pin packages			
$V_{DD\_LV\_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	16	25
$V_{SS\_LV\_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	15	24
$V_{DD\_LV\_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	42	65
$V_{SS\_LV\_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	43	66

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD — DEBUG[2] EIRQ[17]	SIUL LIN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	51	79
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — — DEBUG[3] RXD	SIUL — — SSCM LIN_0	I/O — — — I	Slow	Medium	—	80
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] CLKOUT CS2 — EIRQ[18]	SIUL Control DSPI_2 — SIUL	I/O O O — I	Slow	Medium	62	96
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LIN_0	Input only	—	—	20	29
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input only	—	—	22	31
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIUL — — — ADC_0	Input only	—	—	24	35
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIUL — — — ADC_0	Input only	—	—	25	36

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	54
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O O — — I	Slow	Medium	45	70
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	44	67
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3	GPIO[62] B[1] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	46	73
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[63] — — — AN[10] emu. AN[4]	SIUL — — — ADC_0 emu. ADC_1[6]	Input only	—	—	—	41
Port E (16-bit)									
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input only	—	—	18	27
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input only	—	—	23	32
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input only	—	—	30	42

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	44
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input only	—	—	—	43
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input only	—	—	—	45
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input only	—	—	—	41

1. ALT0 is the primary (default) function for each port after reset.
2. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 → ALT0; PCR.PA = 01 → ALT1; PCR.PA = 10 → ALT2; PCR.PA = 11 → ALT3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
3. Module included on the MCU.
4. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
5. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
6. ADC0.AN emulates ADC1.AN. This feature is used to provide software compatibility between SPC560P34/SPC560P40 and SPC560P50. Refer to ADC chapter of reference manual for more details.

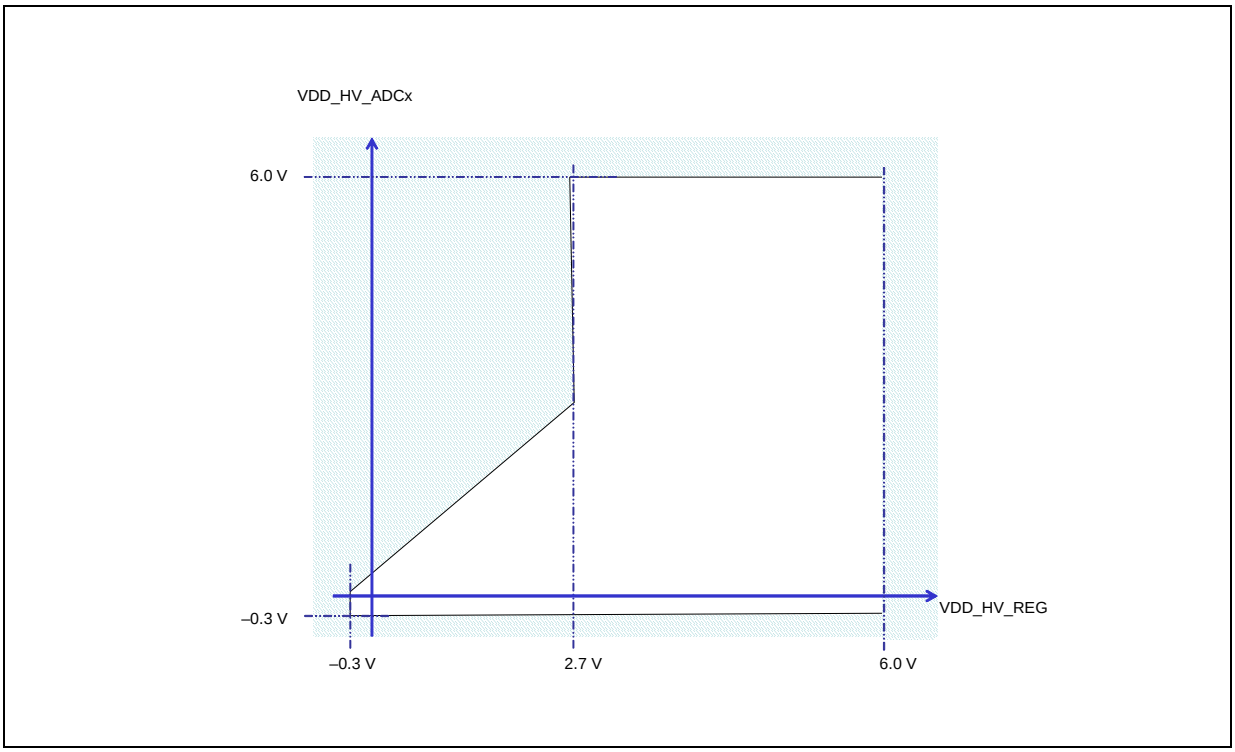


Figure 7. Independent ADC supply (–0.3 V ≤ $V_{DD\_HV\_REG}$ ≤ 6.0 V)

3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	

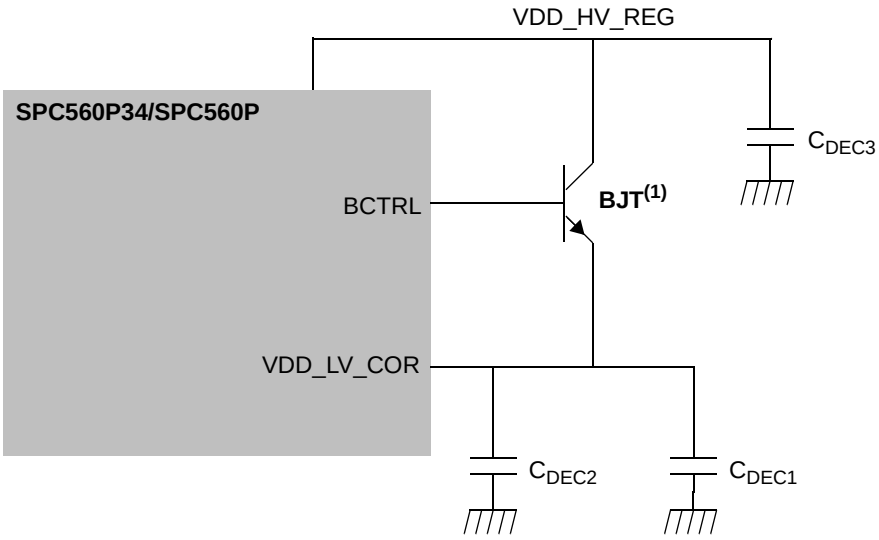
Note: The voltage regulator output cannot be used to drive external circuits. Output pins are to be used only for decoupling capacitance.

$V_{DD\_LV\_COR}$ must be generated using internal regulator and external NPN transistor. It is not possible to provide $V_{DD\_LV\_COR}$ through external regulator.

For the SPC560P34/SPC560P40 microcontroller, capacitor(s), with total values not below C_{DEC1}, should be placed between $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ close to external ballast transistor emitter. 4 capacitors, with total values not below C_{DEC2}, should be placed close to microcontroller pins between each $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ supply pairs and the $V_{DD\_LV\_REGCOR}/V_{SS\_LV\_REGCOR}$ pair . Additionally, capacitor(s) with total values not below C_{DEC3}, should be placed between the $V_{DD\_HV\_REG}/V_{SS\_HV\_REG}$ pins close to ballast collector. Capacitors values have to take into account capacitor accuracy, aging and variation versus temperature.

All reported information are valid for voltage and temperature ranges described in recommended operating condition, *Table 10* and *Table 11*.

Figure 10. Voltage regulator configuration



1. Refer to *Table 15*.

Table 15. Approved NPN ballast components

Part	Manufacturer	Approved derivatives(1)
BCP68	ON Semi	BCP68
	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10; BCX68-16; BCX-25
BC868	NXP	BC868

3.8.2 Voltage monitor electrical characteristics

The device implements a power on reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors low voltage digital power domain

Table 17. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25 °C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5 V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5 V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC560P34/SPC560P40 implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5 V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash

3.10.2 DC electrical characteristics (5 V)

Table 19 gives the DC electrical characteristics at 5 V (4.5 V < $V_{DD\_HV\_IOx}$ < 5.5 V, NVUSRO[PAD3V5V] = 0).

Table 19. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.4(1)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.4 (1)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 14 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –14 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Figure 20. Start-up reset requirements

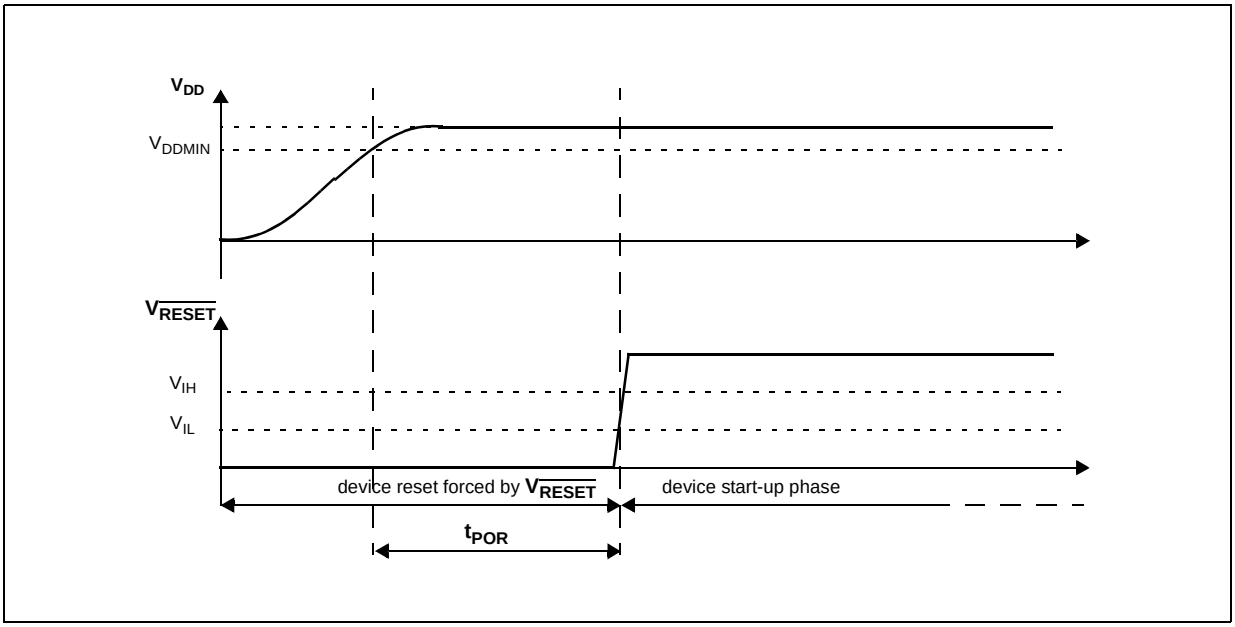


Figure 21. Noise filtering on reset signal

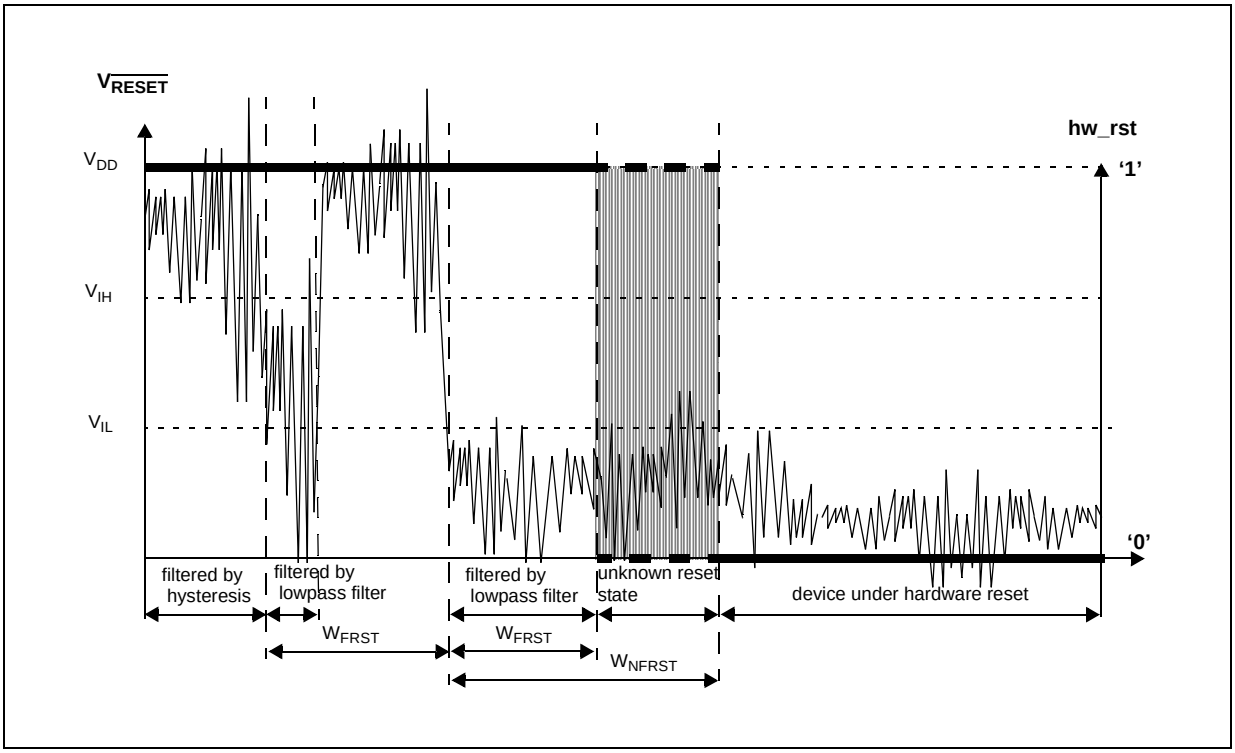
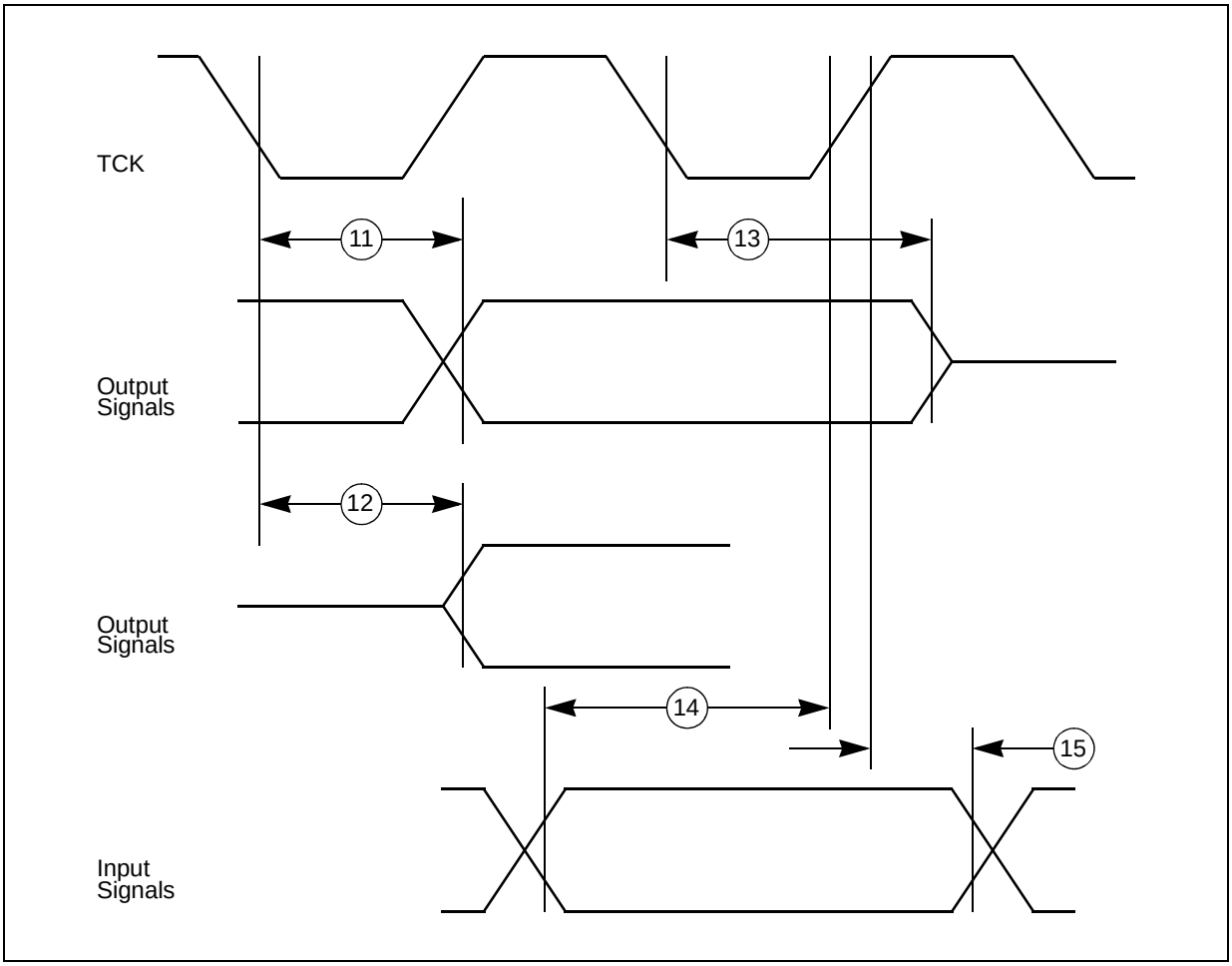


Table 37. $\overline{\text{RESET}}$ electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
t_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
t_{POR}	CC	D	Maximum delay before internal reset is released after all V_{DD_HV} reach nominal supply	Monotonic V_{DD_HV} supply ramp	—	—	1	ms
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[5]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. All values need to be confirmed during device validation.
3. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).

Figure 24. JTAG boundary scan timing



3.17.3 Nexus timing

Table 39. Nexus debug port timing(1)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	4(2)	—	—	t_{CYC}
2	t_{NTDIS}	CC	D	TDI data setup time	5	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	5	—	—	ns
3	t_{NTDIH}	CC	D	TDI data hold time	25	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	25	—	—	ns
4	t_{TDOV}	CC	D	TCK low to TDO data valid	10	—	20	ns
5	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	—	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. Lower frequency is required to be fully compliant to standard.

Table 43. LQFP64 package mechanical data (continued)

Symbol	Dimensions					
	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc[2]	0.08			0.0031		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. Tolerance

Revision history

Table 45. Document revision history

Date	Revision	Changes
01-Sep-2009	1	Initial release.
21-May-2010	2	Editorial updates Updated the following items in the “SPC560P34/SPC560P40 device comparison” table: – The heading – The “SRAM” row – The “FlexCAN” row – The “CTU” row – The “FlexPWM” row – The “LINFlex” row – The “DSPI” row – The “Nexus” row Updated the “SPC560P34/SPC560P40 device configuration difference” table: – Editorial updates – Added the “CTU” row – Deleted the “temperature” row – Swapped the content of Airbag and Full Featured cells Added the “Wakeup unit” block in the SPC560P34/SPC560P40 block diagram Updated the “Absolute Maximum Ratings“ table Updated the “Recommended operating conditions (5.0 V)“ table Updated the “Recommended operating conditions (3.3 V)“ table Updated the “Thermal characteristics for 100-pin LQFP“ table: – Ψ_{JT}: changed the typical value Updated the “EMI testing specifications“ table: replaced all values in “Level (Max)“ column with TBD Updated the “Electrical characteristics“ section: – Added the “Introduction” section – Added the “Parameter classification“ section – Added the “NVUSRO register“ section – Added the “Power supplies constraints (–0.3 V ≤ $V_{DD\_HV\_IOx}$ ≤ 6.0 V)” figure – Added the “Independent ADC supply (–0.3 V ≤ $V_{DD\_HV\_REG}$ ≤ 6.0 V)“ figure – Added the “Power supplies constraints (3.0 V ≤ $V_{DD\_HV\_IOx}$ ≤ 5.5 V)“ figure – Added the “Independent ADC supply (3.0 V ≤ $V_{DD\_HV\_REG}$ ≤ 5.5 V)“ figure Updated the “Power management electrical characteristics” section Updated the “Power Up/Down sequencing” section Updated the “DC electrical characteristics“ section – Deleted the “NVUSRO register” section – Updated the “DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)“ section: – Deleted all rows concerning $\overline{\text{RESET}}$ – Deleted “I_{VPP}“ row – Added the max value for C_{IN}

Table 45. Document revision history (continued)

Date	Revision	Changes
21-May-2010	2 (continued)	– Updated the “DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 0)“ section: – Deleted all rows concerning $\overline{\text{RESET}}$ – Deleted “I_{VPP}“ row – Added the max value for C_{IN} Added the “I/O pad current specification“ section Updated the Order codes table. Added “Appendix A”
23-Dec-2010	3	“Introduction” section: – Changed title (was “Overview“) – Updated contents “SPC560P34/SPC560P40 device comparison” table: – Added sentence above table – Removed “FlexRay” row – “FlexCAN” row: removed link to footnote 2 for SPC560P34 – Updated “Safety port” row for SPC560P34 – Updated “DSPI” row for SPC560P34 “SPC560P34/SPC560P40 block diagram”: added the following blocks: MC_CGM, MC_ME, MC_PCU, MC_RGM, CRC, and SSCM Added “SPC560P34/SPC560P40 series block summary” table “Pin muxing” section: removed information on “Symmetric pads” “Electrical characteristics” section: – Updated “Caution” note – Demoted “NVUSRO register” section to subsection of “DC electrical characteristics” section – “NVUSRO register” section: deleted “NVUSRO[WATCHDOG_EN] field description“ section Updated “EMI testing specifications” table “Low voltage monitor electrical characteristics” table: updated $V_{MLVDDOK\_H}$ max value “DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)” table: removed $_{VOL\_SYM}$, and V_{OH_SYM} rows “Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)” table: – $I_{DD\_LV\_CORE}$, RUN—Maximum mode, 40/64 MHz: updated typ/max values – $I_{DD\_LV\_CORE}$, RUN—Airbag mode, 40/64 MHz: updated typ/max values – $I_{DD\_LV\_CORE}$, RUN—Maximum mode, “P” parameter classification: removed – I_{DD_FLASH}: removed rows – I_{DD_ADC}, Maximum mode: updated typ/max values – I_{DD_OSC}: updated max value Updated “DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)” table “Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)” table: – $I_{DD\_LV\_CORE}$, RUN—Maximum mode, 40/64 MHz: updated typ/max values – $I_{DD\_LV\_CORE}$, RUN—Airbag mode, 40/64 MHz: updated typ/max values – I_{DD_FLASH}: removed rows – I_{DD_ADC}, Maximum mode: updated typ/max values – I_{DD_OSC}: updated max value Added “I/O consumption” table Removed “I/O weight” table