Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p40l1beaar

Contents

List of figures

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC560P34/40 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 2 provides a summary of different members of the SPC560P34/SPC560P40 family and their features—relative to full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC560P34/SPC560P40 device comparison

Feature	SPC560P34 Full-featured	SPC560P40 Full-featured
Code flash memory (with ECC)	192 KB	256 KB
Data flash memory / EE option (with ECC)	64 KB	
SRAM (with ECC)	12 KB	20 KB
Processor core	32-bit e200z0h	
Instruction set	VLE (variable length encoding)	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) module	1	
INTC (interrupt controller) channels	120	
PIT (periodic interrupt timer)	1 (with four 32-bit timers)	

Table 2. SPC560P34/SPC560P40 device comparison (continued)

Feature		SPC560P34 Full-featured	SPC560P40 Full-featured
eDMA (enhanced direct memory access) channels		16	
FlexCAN (controller area network)		1(1)	2(1),(2)
Safety port		No	Yes (via second FlexCAN module)
FCU (fault collection unit)		Yes	
CTU (cross triggering unit)		Yes	Yes
eTimer		1 (16-bit, 6 channels)	
FlexPWM (pulse-width modulation) channels		8 (capture capabity not supported)	8 (capture capability not supported)
Analog-to-digital converter (ADC)		1 (10-bit, 16 channels)	
LINFlex		2 (1 × Master/Slave, 1 × Master only)	2 (1 × Master/Slave, 1 × Master only)
DSPI (deserial serial peripheral interface)		2	3
CRC (cyclic redundancy check) unit		Yes	
Junction temperature sensor		No	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Nexus Class 1)	
Supply	Digital power supply(3)	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		LQFP64 LQFP100	
Temperature	Standard ambient temperature	–40 to 125 °C	

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a safety port with a bit rate as high as 8 Mbit/s at 64 MHz.
3. The different supply voltages vary according to the part number ordered.

SPC560P34/SPC560P40 is available in two configurations having different features: Full-featured and airbag. *Table 3* shows the main differences between the two versions of the SPC560P40 MCU.

1.5 Feature details

1.5.1 High performance e200z0 core processor

The e200z0 Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16- and 32-bit instructions
  - Results in smaller code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non-maskable interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 3 master ports:
  - e200z0 core complex instruction port
  - e200z0 core complex Load/Store Data port
  - eDMA
- 3 slave ports:
  - Flash memory (Code and Data)
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels.

The eDMA module provides the following features:

- 16 channels support independent 8-, 16- or 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to either post-increment or to remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, FlexPWM, eTimer and CTU
- Programmable DMA channel multiplexer allows assignment of any DMA source to any available DMA channel with as many as 30 request sources
- eDMA abort operation through software

1.5.4 Flash memory

The SPC560P34/SPC560P40 provides 320 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module is interfaced to the system bus by a dedicated flash memory controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit wide prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring two wait-states.

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 128 selectable-priority interrupt sources.

For high-priority interrupt requests, the time from the assertion of the interrupt request by the peripheral to the execution of the interrupt service routine (ISR) by the processor has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources.
- 1 external high priority interrupt (NMI) directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
  - Memory sizes/status
  - Device mode and security status
  - Determine boot vector
  - Search code flash for bootable sector
  - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

The FlexPWM block implements the following features:

- 16-bit resolution for center, edge-aligned, and asymmetrical PWMs
- Clock frequency same as that used for e200z0h core
- PWM outputs can operate as complementary pairs or independent channels
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Write protection for critical registers
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a “Force Out” event
- PWMX pin can optionally output a third PWM signal from each submodule
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual-edge capture functionality
- eDMA support with automatic reload
- 2 fault inputs
- Capture capability for PWMA, PWMB, and PWMX channels not supported

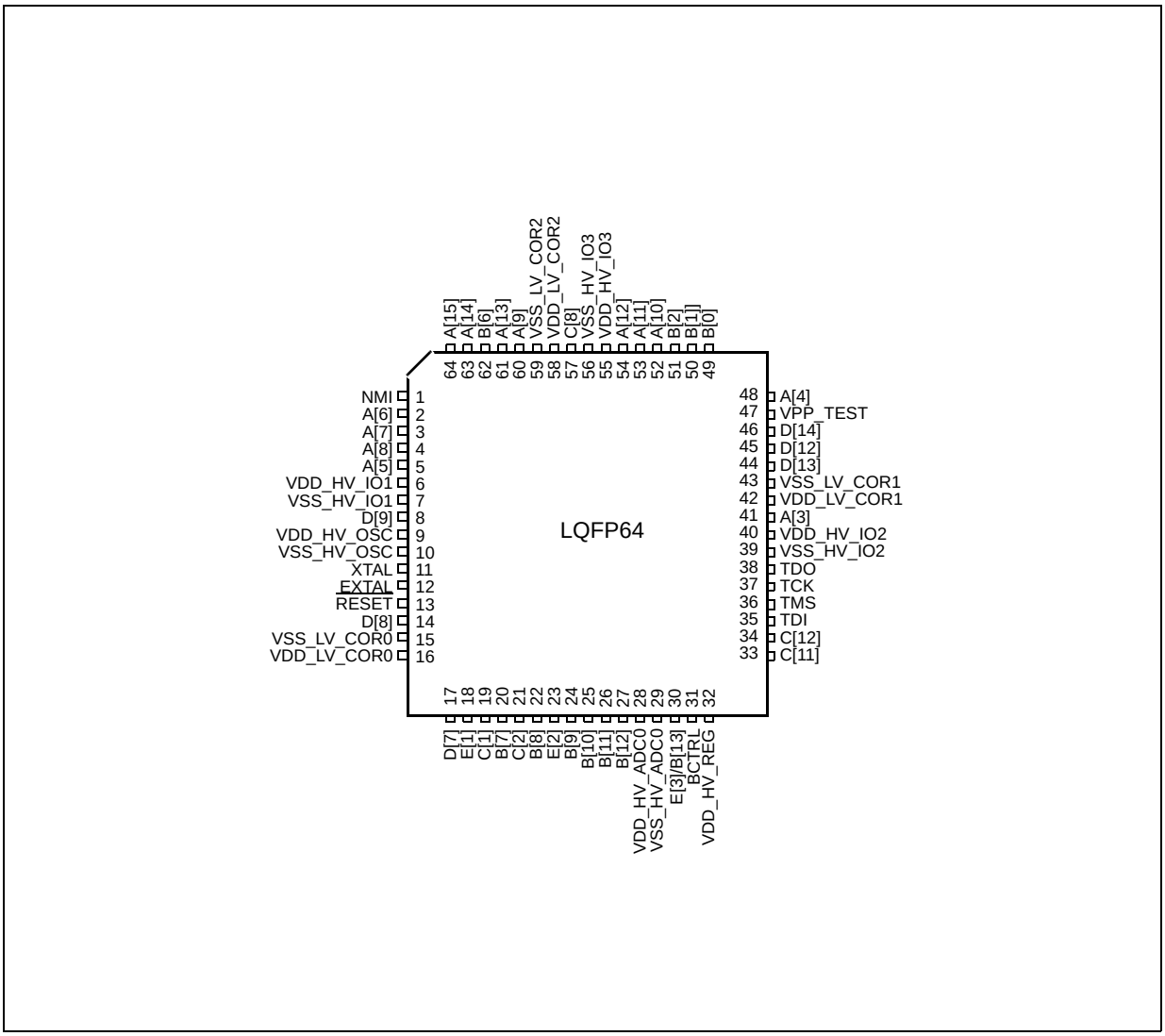


Figure 3. 64-pin LQFP pinout – Airbag configuration (top view)

2.2.3 Pin multiplexing

Table 7 defines the pin list and muxing for the SPC560P34/SPC560P40 devices.

Each row of *Table 7* shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

SPC560P34/SPC560P40 devices provide three main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see “Pad AC Specifications” in the device datasheet.

Table 7. Pin muxing

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O I/O O I	Slow	Medium	—	51
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	—	52
A[2]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O — O I I I	Slow	Medium	—	57
A[3]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	41	64

3 Electrical characteristics

3.1 Introduction

This section contains device electrical characteristics as well as temperature and power considerations.

This microcontroller contains input protection against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down resistors, which are provided by the device for most general purpose pins.

The following tables provide the device characteristics and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution:

All of the following parameter values can vary depending on the application and must be confirmed during silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 9. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(2)	
I_{INJSUM}	S R	Absolute sum of all input currents during overload condition	—	–50	50	mA
T_{STG}	S R	Storage temperature	—	–55	150	°C
T_J	S R	Junction temperature under bias	—	–40	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages.
3. The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 300$ mV.
4. Guaranteed by device validation.
5. Minimum value of TV_{DD} must be guaranteed until $V_{DD\_HV\_REG}$ reaches 2.6 V (maximum value of V_{PORH})
6. Only when $V_{DD\_HV\_IOx} < 5.2$ V

Figure 6 shows the constraints of the different power supplies.

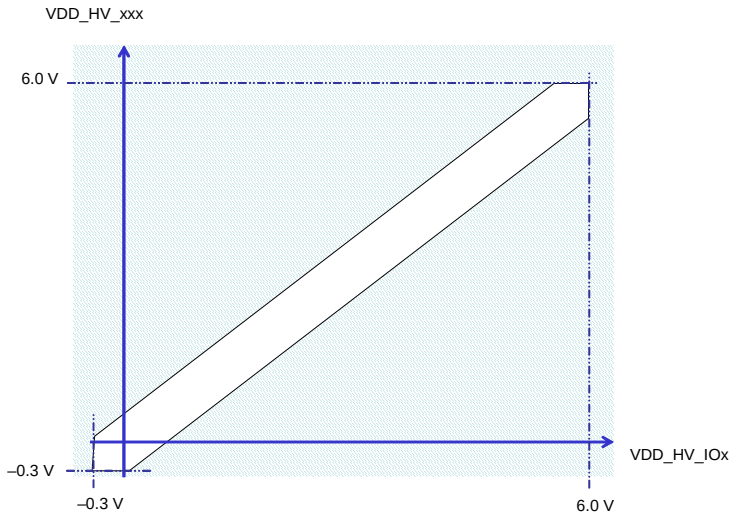


Figure 6. Power supplies constraints (–0.3 V ≤ $V_{DD\_HV\_IOx}$ ≤ 6.0 V)

The SPC560P34/SPC560P40 supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. *Figure 7* shows the constraints of the ADC power supply.

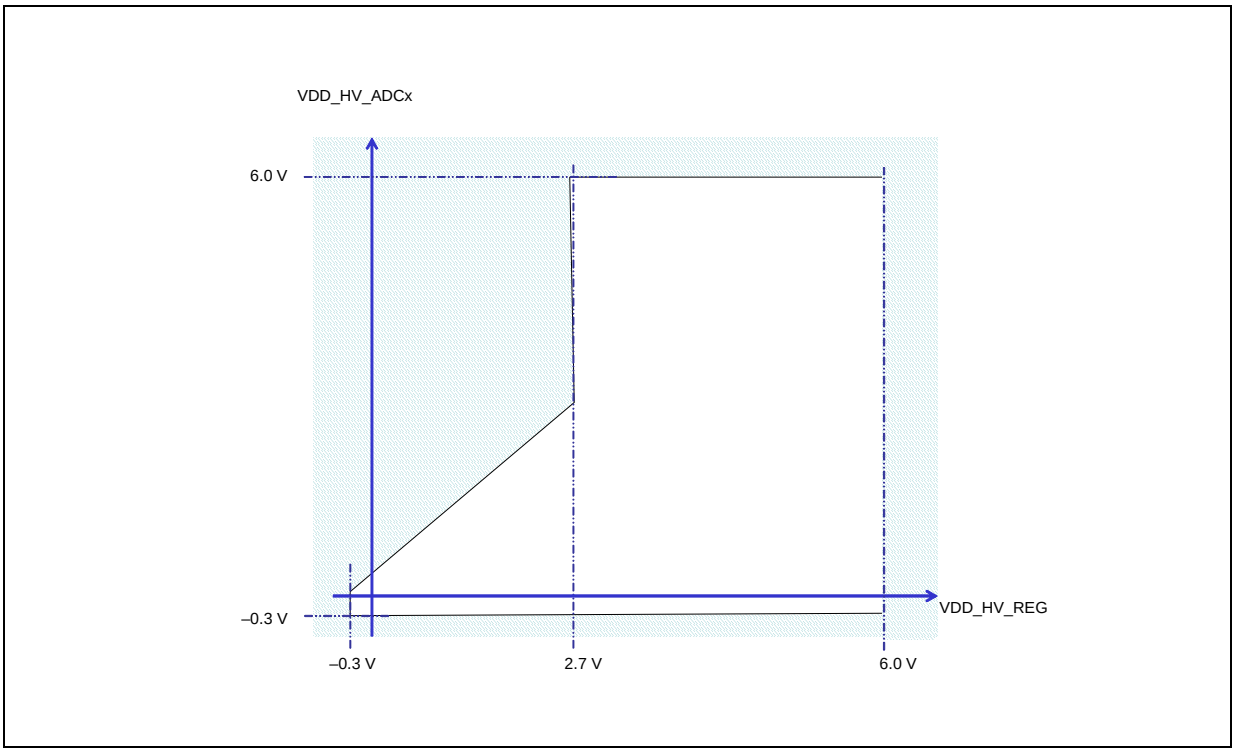


Figure 7. Independent ADC supply (–0.3 V ≤ $V_{DD\_HV\_REG}$ ≤ 6.0 V)

3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	

Table 11. Recommended operating conditions (3.3 V) (continued)

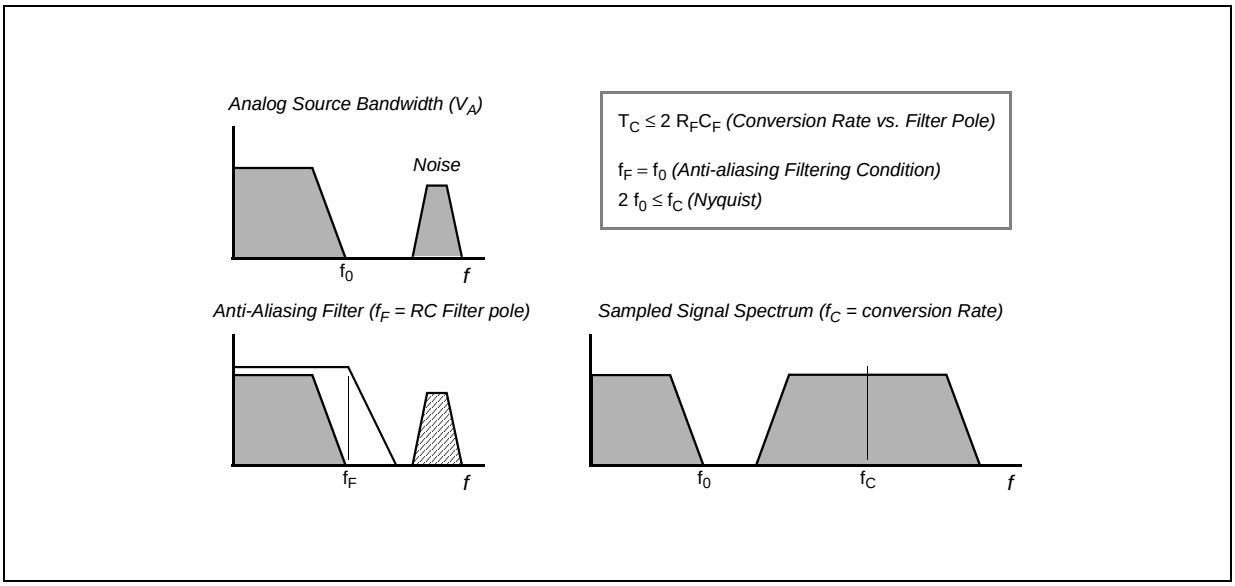
Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{DD\_HV\_ADC0}$	SR	3.3 V ADC_0 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG}$ – 0.1	5.5	
$V_{SS\_HV\_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(3),(4)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(3),(4)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 60 MHz	–40	125	°C
			f_{CPU} = 64 MHz	–40	105	°C

1. Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 100$ mV.
3. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
4. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.
   – $V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.
   – $V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_RECORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Figure 8 shows the constraints of the different power supplies.

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

Figure 18. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 2048 \bullet C_S$$

Table 32. Flash memory module life

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	years
			Blocks with 10000 P/E cycles	10	—	years
			Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 33. Flash memory read access timing

Symbol	C	Parameter	Conditions(1)	Max value	Unit
f_{max}	C	Maximum working frequency for code flash memory at given number of wait states in worst conditions	2 wait states	66	MHz
			0 wait states	18	
f_{max}	C	Maximum working frequency for data flash memory at given number of wait states in worst conditions	8 wait states	66	MHz

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.15.2 Flash memory power supply DC characteristics

Table 34 shows the power supply DC characteristics on external supply.

Table 34. Flash memory power supply DC electrical characteristics

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
I_{FLPW}	CC	D	Sum of the current consumption on $V_{DD\_HV\_IOx}$ and $V_{DD\_LV\_CORx}$ during low-power mode	Code flash memory	—	—	900	µA
I_{FPWD}	CC	D	Sum of the current consumption on $V_{DD\_HV\_IOx}$ and $V_{DD\_LV\_CORx}$ during power-down mode	Code flash memory	—	—	150	µA
				Data flash memory	—	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

3.15.3 Start-up/Switch-off timings

Table 35. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	Code flash memory	—	—	125	µs
		T		Data flash memory	—	—	125	
$T_{FLALPEXIT}$	CC	D	Delay for Flash module to exit low-power mode	Code flash memory	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	Code flash memory	—	—	30	
		T		Data flash memory	—	—	30	
$T_{FLALPENTRY}$	CC	D	Delay for Flash module to enter low-power mode	Code flash memory	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

3.16 AC specifications

3.16.1 Pad AC specifications

Table 36. Output pin transition times

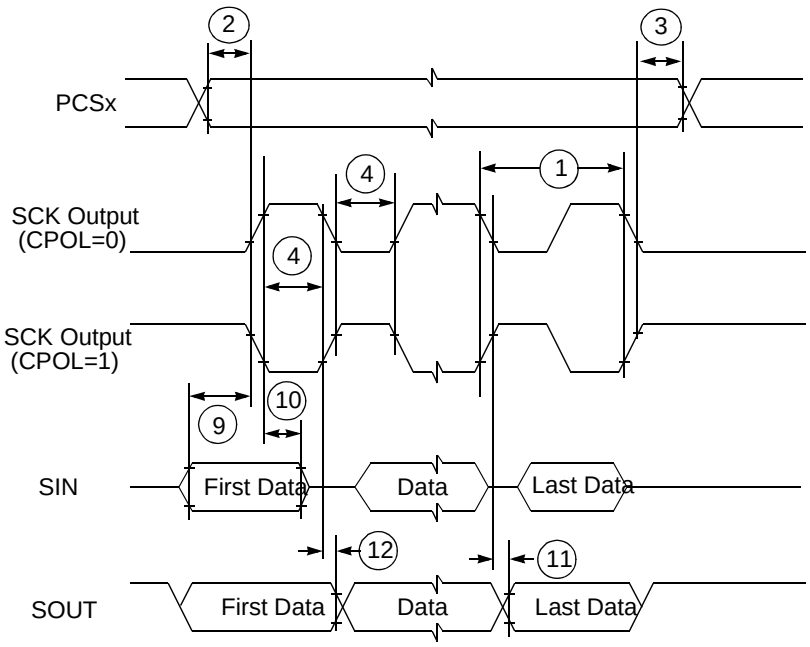
Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
t_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

Table 41. DSPI timing(1) (continued)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

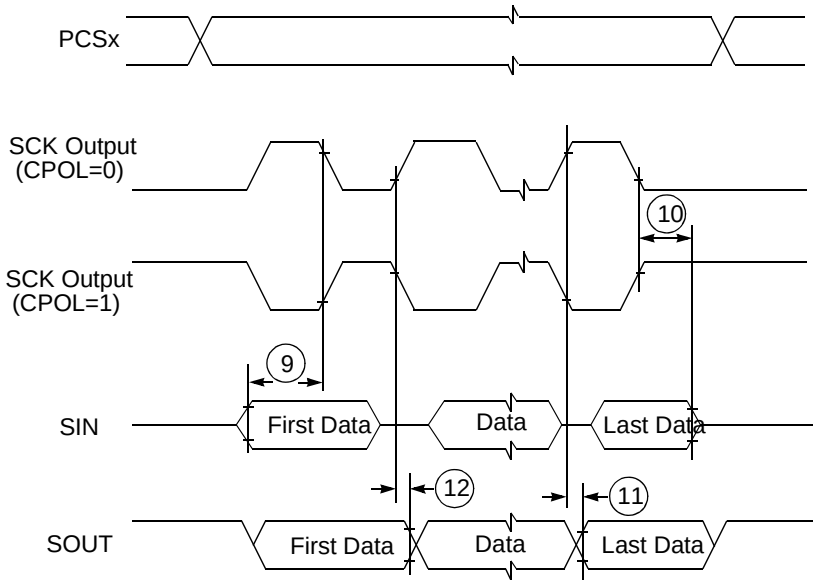
1. All timing are provided with 50 pF capacitance on output, 1 ns transition time on input signal

Figure 29. DSPI classic SPI timing – Master, CPHA = 0



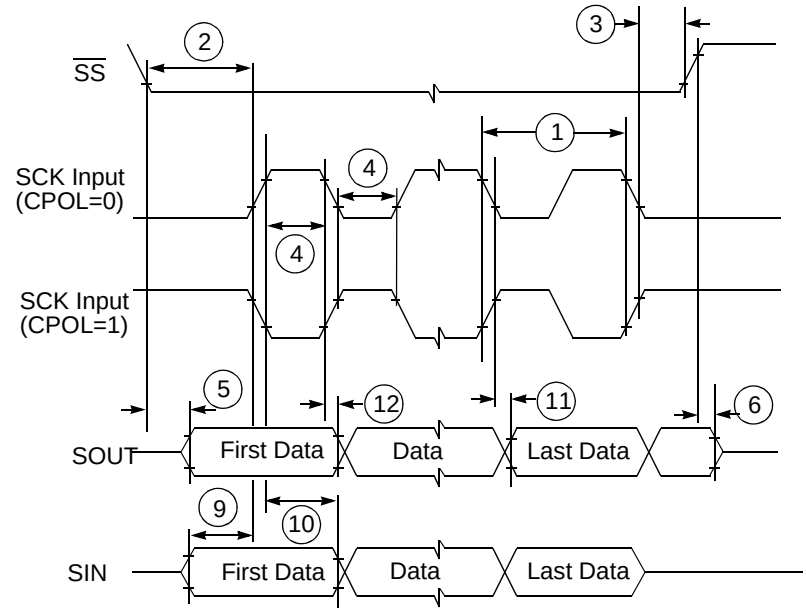
Note: Numbers shown reference *Table 41*.

Figure 30. DSPI classic SPI timing – Master, CPHA = 1



Note: Numbers shown reference *Table 41*.

Figure 31. DSPI classic SPI timing – Slave, CPHA = 0



Note: Numbers shown reference *Table 41*.

Table 45. Document revision history (continued)

Date	Revision	Changes
23-Dec-2010	3 (continued)	Updated “Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)” table Updated “Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)” table “Input clock characteristics” table: updated f_{CLK} max value “PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)” table: – Updated supply voltage range for V_{DDPLL} in the table title – Updated f_{SCM} max value – Updated C_{JITTER} row – Updated f_{MOD} max value Updated “16 MHz RC oscillator electrical characteristics” table Updated “ADC conversion characteristics” table “Program and erase specifications” table: – $T_{wprogram}$: updated initial max and max values – T_{BKPRG}, 64 KB: updated initial max and max values – added information about “erase time” for Data Flash “Flash module life” table: – P/E, 32 KB: added typ value – P/E, 128 KB: added typ value Replaced “Pad AC specifications (5.0 V, NVUSRO[PAD3V5V] = 0)” and “Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)” tables with “Output pin transition times” table “JTAG pin AC electrical characteristics” table: – t_{TDOV}: updated max value – t_{TDOHZ}: added min value and removed max value “Nexus debug port timing” table: removed the rows “t_{MCYC}”, “t_{MDOV}”, “t_{MSEOV}”, and “t_{EVTOV}” Updated “External interrupt timing (IRQ pin)” table Updated “FlexCAN timing” table Updated “DSPI timing” table Updated “Ordering information” section