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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p40l1beaby

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Table 3. SPC560P40 device configuration differences

Feature	Configuration	
	Airbag	Full-featured
SRAM (with ECC)	16 KB	20 KB
FlexCAN (controller area network)	1	2
Safety port	No	Yes (via second FlexCAN module)
FlexPWM (pulse-width modulation) channels	No	8 (capture capability not supported)
CTU (cross triggering unit)	No	Yes

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC560P34/SPC560P40 MCU. *Table 2* summarizes the functions of the blocks.

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 128 selectable-priority interrupt sources.

For high-priority interrupt requests, the time from the assertion of the interrupt request by the peripheral to the execution of the interrupt service routine (ISR) by the processor has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources.
- 1 external high priority interrupt (NMI) directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
  - Memory sizes/status
  - Device mode and security status
  - Determine boot vector
  - Search code flash for bootable sector
  - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.22 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the SPC560P34/SPC560P40 features the following:

- Supports LIN Master mode (both instances), LIN Slave mode (only one instance) and UART mode
- LIN state machine compliant to LIN1.3, 2.0 and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to 8 data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features:
  - Autonomous LIN header handling
  - Autonomous LIN response handling
  - Optional discarding of irrelevant LIN responses using ID filter
- UART mode:
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function(1),(2)	Functions	Peripheral(3)	I/O direction(4)	Pad speed(5)		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	44
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input only	—	—	—	43
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input only	—	—	—	45
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input only	—	—	—	41

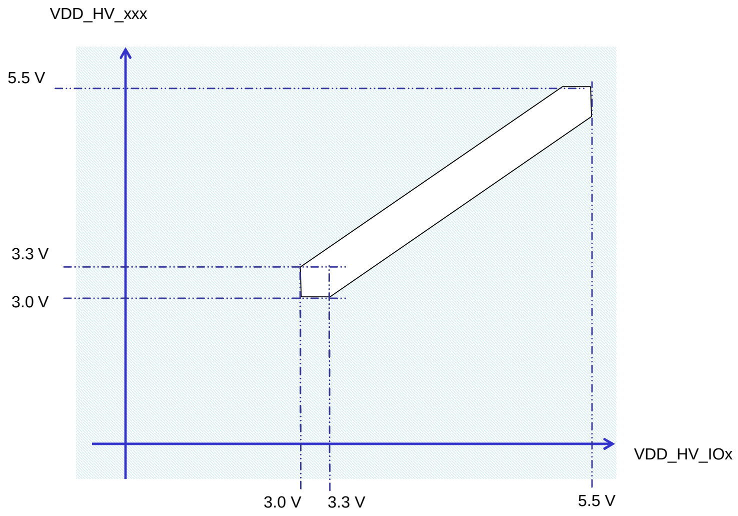
1. ALT0 is the primary (default) function for each port after reset.
2. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 → ALT0; PCR.PA = 01 → ALT1; PCR.PA = 10 → ALT2; PCR.PA = 11 → ALT3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to ‘1’, regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as “—”.
3. Module included on the MCU.
4. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
5. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
6. ADC0.AN emulates ADC1.AN. This feature is used to provide software compatibility between SPC560P34/SPC560P40 and SPC560P50. Refer to ADC chapter of reference manual for more details.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(2)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(3)	SR	3.3 V/5.0 V input/output supply voltage (supply). Code flash memory supply with $V_{DD\_HV\_IO3}$ and data flash memory with $V_{DD\_HV\_IO2}$	—	–0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	3.3 V/5.0 V input/output supply voltage (ground). Code flash memory ground with $V_{SS\_HV\_IO3}$ and data flash memory with $V_{SS\_HV\_IO2}$	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V/5.0 V crystal oscillator amplifier supply voltage (supply)	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_OSC}$	SR	3.3 V/5.0 V crystal oscillator amplifier supply voltage (ground)	—	–0.1	0.1	V
$V_{DD\_HV\_ADC0}$	SR	3.3 V/5.0 V ADC_0 supply and high-reference voltage	$V_{DD\_HV\_REG}$ < 2.7 V	–0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	–0.3	6.0	
$V_{SS\_HV\_ADC0}$	SR	3.3 V/5.0 V ADC_0 ground and low-reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V/5.0 V voltage-regulator supply voltage	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up(4) with respect to ground (V_{SS})	—	3.0(5)	500 x 10^3 (0.5 [V/µs])	V/s
$V_{DD\_LV\_CORx}$	CC	1.2 V supply pins for core logic (supply)	—	–0.1	1.5	V
$V_{SS\_LV\_CORx}$	SR	1.2 V supply pins for core logic (ground)	—	–0.1	0.1	V
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$)	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3(6)	
I_{INJPAD}	SR	Input current on any pin during overload condition	—	–10	10	mA

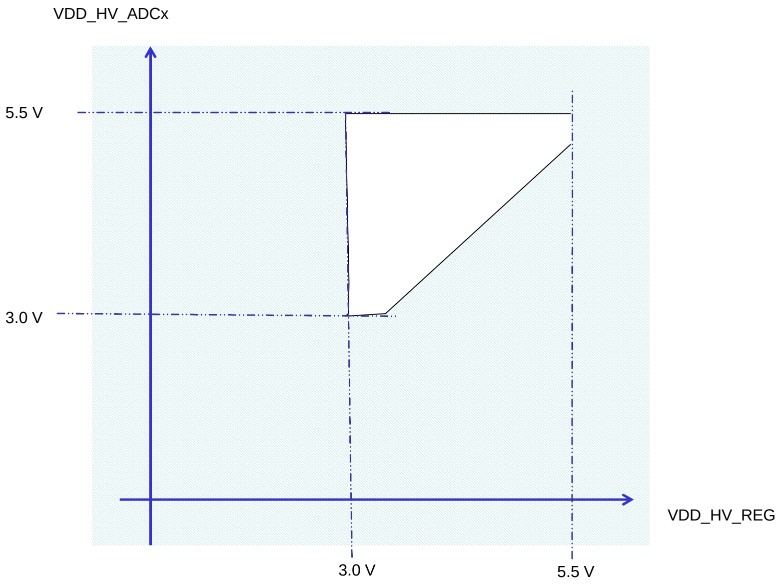
Figure 8. Power supplies constraints (3.0 V $\leq V_{DD\_HV\_IOx} \leq$ 5.5 V)



Note: IO AC and DC characteristics are guaranteed only in the range of 3.0–3.6 V when PAD3V5V is low, and in the range of 4.5–5.5 V when PAD3V5V is high.

The SPC560P34/SPC560P40 supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. *Figure 9* shows the constraints of the ADC power supply.

Figure 9. Independent ADC supply (3.0 V $\leq V_{DD\_HV\_REG} \leq$ 5.5 V)



Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3: $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

- Semiconductor Equipment and Materials International
  3081 Zanker Road
  San Jose, CA 95134U.S.A.
  (408) 943-6900
- MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at (800) 854-7179 or (303) 397-7956.
- JEDEC specifications are available on the WEB at http://www.jedec.org.
- C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
- G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53–58, March 1998.
- B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.8.2 Voltage monitor electrical characteristics

The device implements a power on reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors low voltage digital power domain

Table 17. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25 °C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5 V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5 V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC560P34/SPC560P40 implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5 V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash

3.10.3 DC electrical characteristics (3.3 V)

Table 21 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IOx}$ < 3.6 V, NVUSRO[PAD3V5V] = 1); see *Figure 14*.

Table 21. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)(1)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.4(2)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.4(2)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 11 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF

1. These specifications are design targets and subject to change per device characterization.
2. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 24. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.11 Main oscillator electrical characteristics

The SPC560P34/SPC560P40 provides an oscillator/resonator driver.

Table 25. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{OSC}	SR	—	Oscillator frequency		4	40	MHz
g_m	—	P	Transconductance		6.5	25	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin		1	—	V
t_{OSCSU}	—	T	Start-up time(1),(2)		8	—	ms
C_L	CC	T	XTAL load capacitance(3)	4 MHz	5	30	pf
		T		8 MHz	5	26	
		T		12 MHz	5	23	
		T		16 MHz	5	19	
		T		20 MHz	5	16	
		T		40 MHz	5	8	

1. The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL
3. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

Table 28. FMPLL electrical characteristics (continued)

Symbol	C	Parameter		Conditions(1)	Value		Unit
					Min	Max	
f_{FREE}	P	Free-running frequency		Measured using clock division—typically /16	20	150	MHz
t_{CYC}	D	System clock period		—	—	1 / f_{SYS}	ns
f_{LORL}	D	Loss of reference frequency window(3)		Lower limit	1.6	3.7	MHz
f_{LORH}	D			Upper limit	24	56	
f_{SCM}	D	Self-clocked mode frequency(4),(5)		—	20	150	MHz
C_{JITTER}	T	CLKOUT period jitter(6),(7),(8),(9)	Short-term jitter(10)	f_{SYS} maximum	–4	4	% f_{CLKOUT}
			Long-term jitter (average over 2 ms interval)	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 64 MHz, 4000 cycles	—	10	ns
t_{lpll}	D	PLL lock time(11), (12)		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	–6	6	% f_{SYS}
f_{UL}	D	Frequency un-LOCK range		—	–18	18	% f_{SYS}
f_{CS}	D	Modulation depth		Center spread	±0.25	±4.0(13)	% f_{SYS}
f_{DS}	D			Down spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency(14)		—	—	70	kHz

1. $V_{DD\_LV\_CORx}$ = 1.2 V ±10%; V_{SS} = 0 V; T_A = –40 to 125 °C, unless otherwise specified
2. Considering operation with PLL not bypassed.
3. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
4. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
5. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
6. This value is determined by the crystal manufacturer and board design.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DD\_LV\_COR0}$ and $V_{SS\_LV\_COR0}$ and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
8. Proper PC board layout procedures must be followed to achieve specifications.
9. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
10. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
12. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
13. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
14. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

4. C_L includes device and package capacitance (C_{PKG} < 5 pF).
5. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}/2$)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing

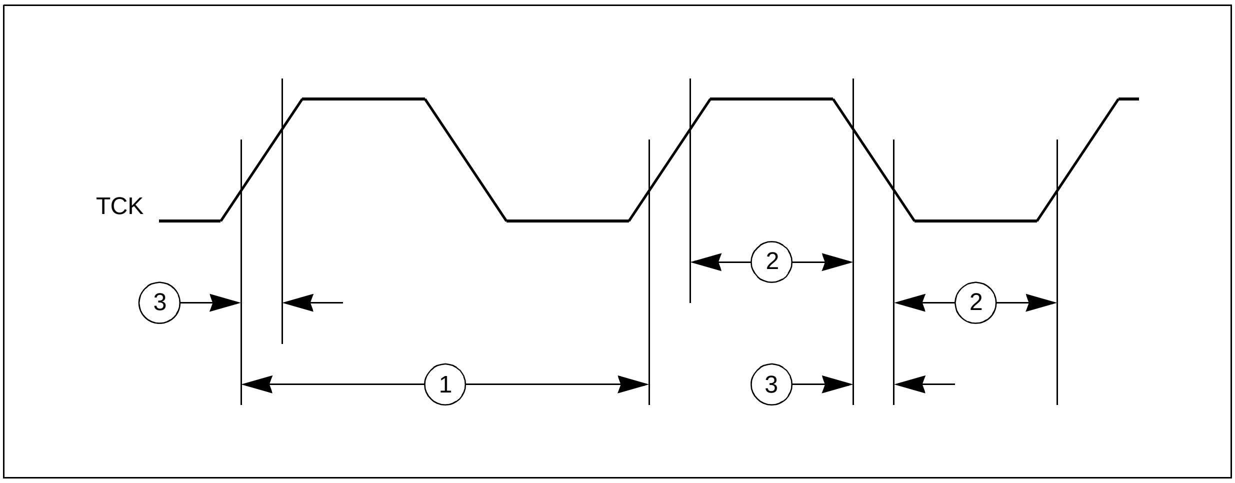


Figure 25. Nexus output timing

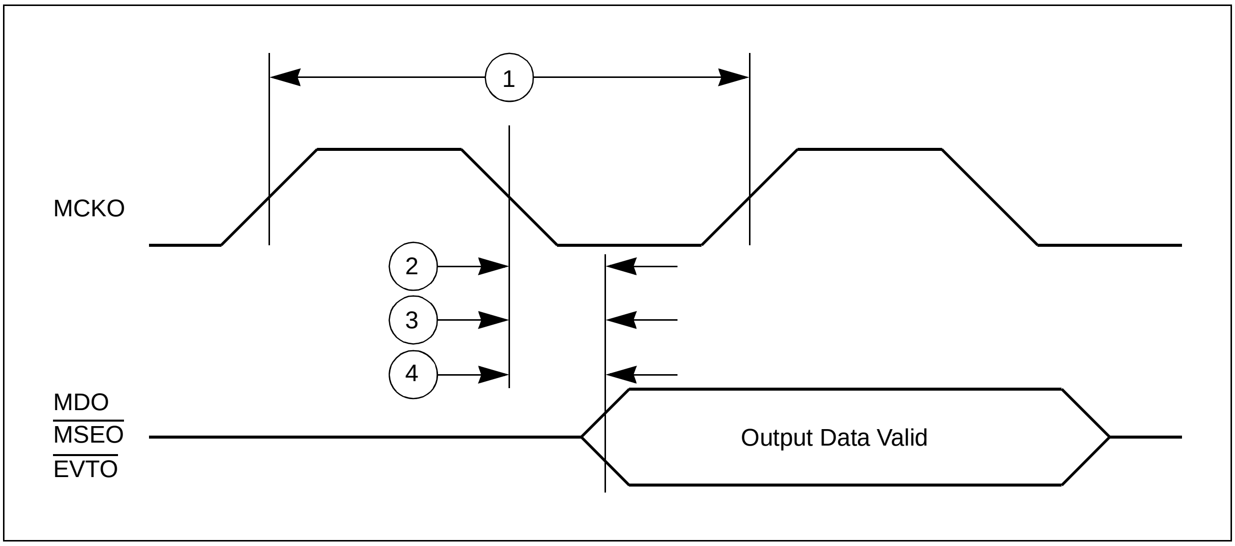


Figure 26. Nexus event trigger and test clock timing

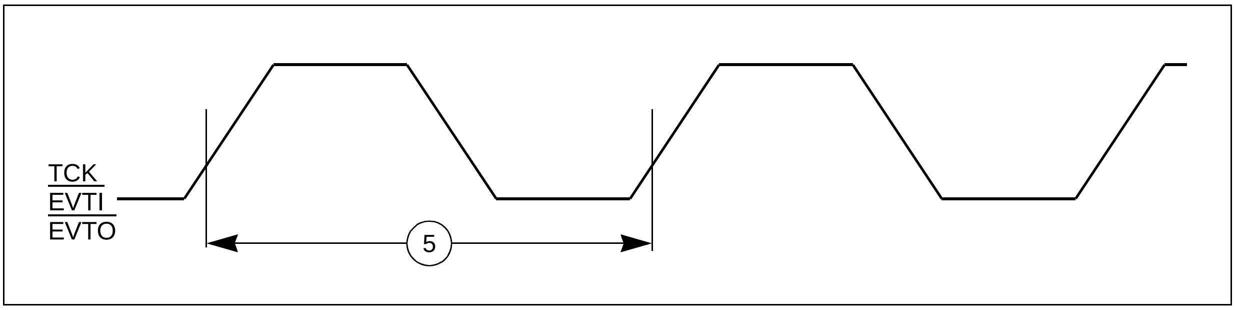
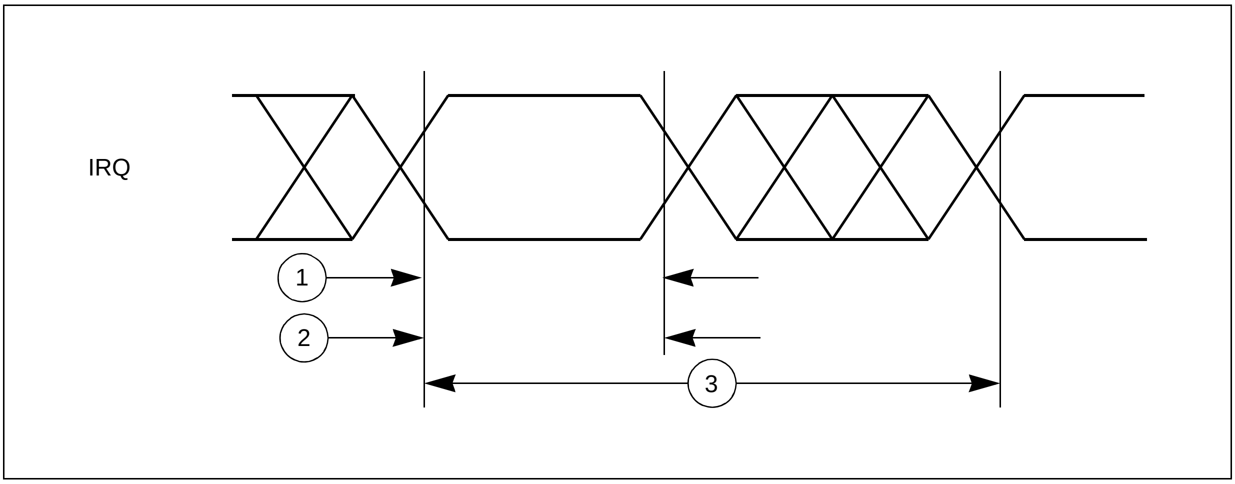


Figure 28. External interrupt timing

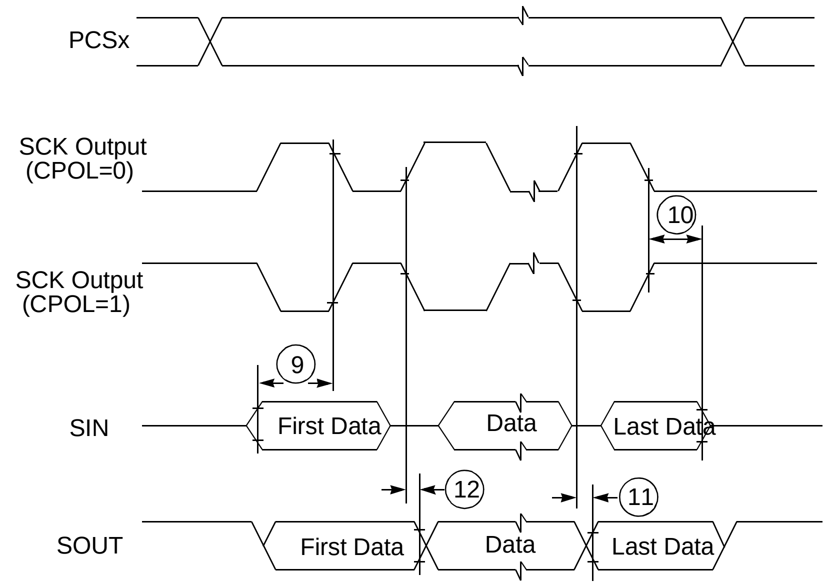


3.17.5 DSPI timing

Table 41. DSPI timing(1)

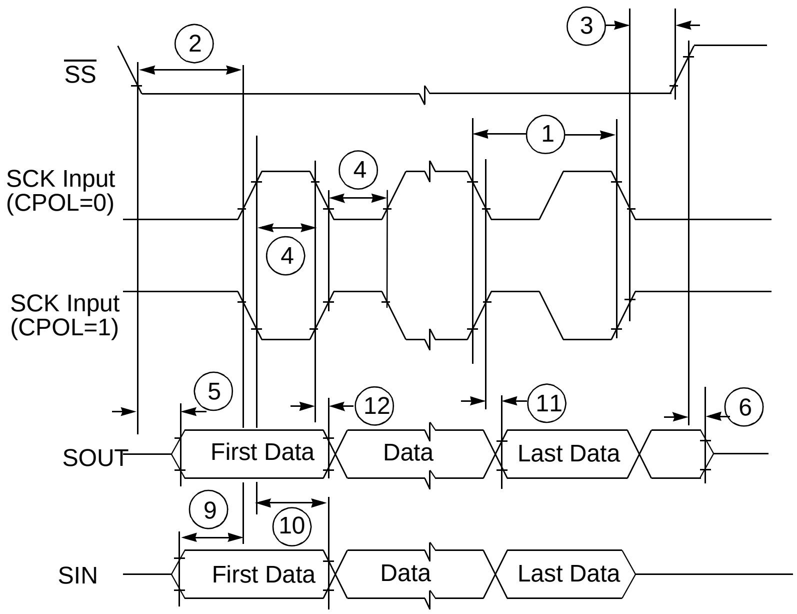
No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	60	—	ns
					Slave (MTFE = 0)	60	—	
2	t_{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	26	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{\text{SS}}$ active to SOUT valid	—	30	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{\text{SS}}$ inactive to SOUT high impedance or invalid	—	16	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{\text{PCSS}}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{\text{PCSS}}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	35	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	35	—	
					Master (MTFE = 1, CPHA = 1)	35	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	–5	—	

Figure 30. DSPI classic SPI timing – Master, CPHA = 1



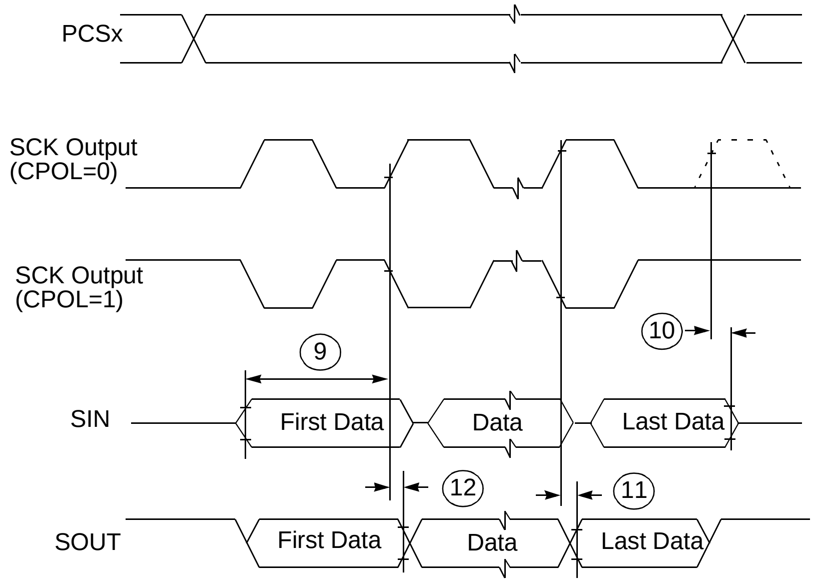
Note: Numbers shown reference *Table 41*.

Figure 31. DSPI classic SPI timing – Slave, CPHA = 0



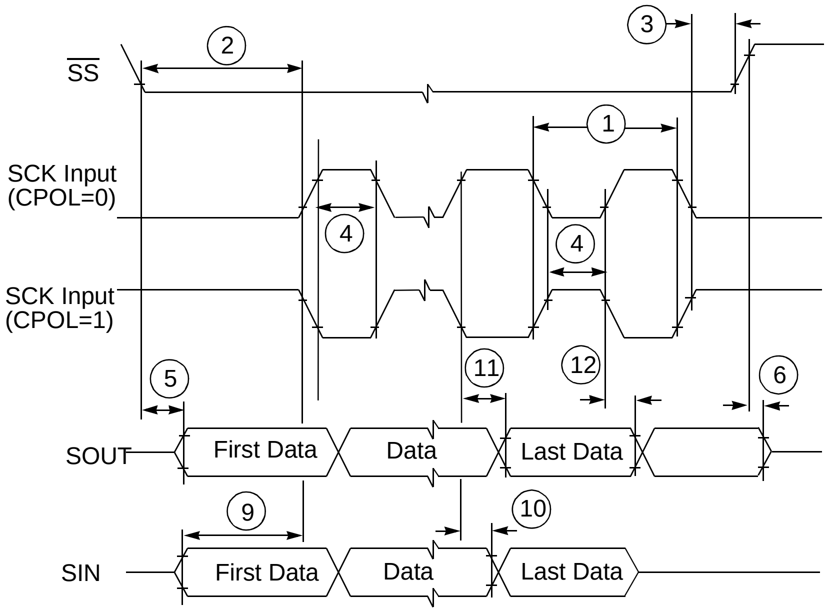
Note: Numbers shown reference *Table 41*.

Figure 34. DSPI modified transfer format timing – Master, CPHA = 1



Note: Numbers shown reference *Table 41*.

Figure 35. DSPI modified transfer format timing – Slave, CPHA = 0



Note: Numbers shown reference *Table 41*.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
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