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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p40l1cefay

Table 3. SPC560P40 device configuration differences

Feature	Configuration	
	Airbag	Full-featured
SRAM (with ECC)	16 KB	20 KB
FlexCAN (controller area network)	1	2
Safety port	No	Yes (via second FlexCAN module)
FlexPWM (pulse-width modulation) channels	No	8 (capture capability not supported)
CTU (cross triggering unit)	No	Yes

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC560P34/SPC560P40 MCU. *Table 2* summarizes the functions of the blocks.

Table 4. SPC560P34/SPC560P40 series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Is the interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

1.5 Feature details

1.5.1 High performance e200z0 core processor

The e200z0 Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16- and 32-bit instructions
  - Results in smaller code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non-maskable interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

1.5.23 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC560P34/SPC560P40 MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 8 chip select lines available:
  - 8 on DSPI_0
  - 4 each on DSPI_1 and DSPI_2
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- Queueing operation possible through use of the I/O processor or eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.24 Pulse width modulator (FlexPWM)

The pulse width modulator module (PWM) contains four PWM submodules each of which is set up to control a single half-bridge power stage. There are also three fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

Table 5. Supply pins (continued)

Supply		Pin	
Symbol	**Description**	**64-pin**	**100-pin**
$V_{DD\_LV\_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	58	92
$V_{SS\_LV\_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD\_LV\_COR}$ pin.	59	93

1. Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on $V_{DD\_HV\_ADCx}$/$V_{SS\_HV\_ADCx}$ pins.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC560P34/SPC560P40 devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective pad configuration register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad speed(1)		Pin	
			SRC = 0	SRC = 1	64-pin	100-pin
Dedicated pins						
NMI	Non-maskable Interrupt	Input only	Slow	—	1	1
XTAL	Analog output of the oscillator amplifier circuit—needs to be grounded if oscillator is used in bypass mode	—	—	—	11	18
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode Analog input for the clock generator when the oscillator is in bypass mode	—	—	—	12	19
TDI	JTAG test data input	Input only	Slow	—	35	58
TMS	JTAG state machine control	Input only	Slow	—	36	59
TCK	JTAG clock	Input only	Slow	—	37	60
TDO	JTAG test data output	Output only	Slow	Fast	38	61
Reset pin						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	13	20
Test pin						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	47	74

1. SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

Table 7. Pin muxing (continued)

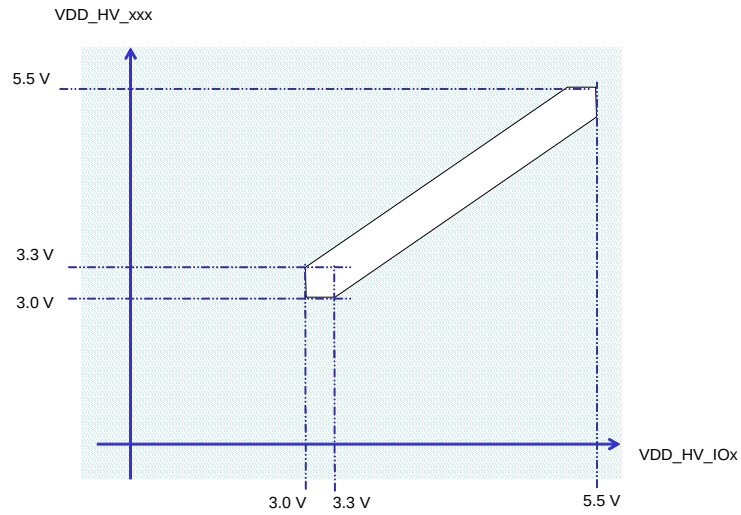
Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	54
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O O — — I	Slow	Medium	45	70
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	44	67
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3	GPIO[62] B[1] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	46	73
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[63] — — — AN[10] emu. AN[4]	SIUL — — — ADC_0 emu. ADC_1[6]	Input only	—	—	—	41
Port E (16-bit)									
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input only	—	—	18	27
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input only	—	—	23	32
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input only	—	—	30	42

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max[2]	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$[3]	SR	3.3 V/5.0 V input/output supply voltage (supply). Code flash memory supply with $V_{DD\_HV\_IO3}$ and data flash memory with $V_{DD\_HV\_IO2}$	—	–0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	3.3 V/5.0 V input/output supply voltage (ground). Code flash memory ground with $V_{SS\_HV\_IO3}$ and data flash memory with $V_{SS\_HV\_IO2}$	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V/5.0 V crystal oscillator amplifier supply voltage (supply)	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_OSC}$	SR	3.3 V/5.0 V crystal oscillator amplifier supply voltage (ground)	—	–0.1	0.1	V
$V_{DD\_HV\_ADC0}$	SR	3.3 V/5.0 V ADC_0 supply and high-reference voltage	$V_{DD\_HV\_REG}$ < 2.7 V	–0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	–0.3	6.0	
$V_{SS\_HV\_ADC0}$	SR	3.3 V/5.0 V ADC_0 ground and low-reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V/5.0 V voltage-regulator supply voltage	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up[4] with respect to ground (V_{SS})	—	3.0[5]	500 x 10^3 (0.5 [V/µs])	V/s
$V_{DD\_LV\_CORx}$	CC	1.2 V supply pins for core logic (supply)	—	–0.1	1.5	V
$V_{SS\_LV\_CORx}$	SR	1.2 V supply pins for core logic (ground)	—	–0.1	0.1	V
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$)	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3[6]	
I_{INJPAD}	SR	Input current on any pin during overload condition	—	–10	10	mA

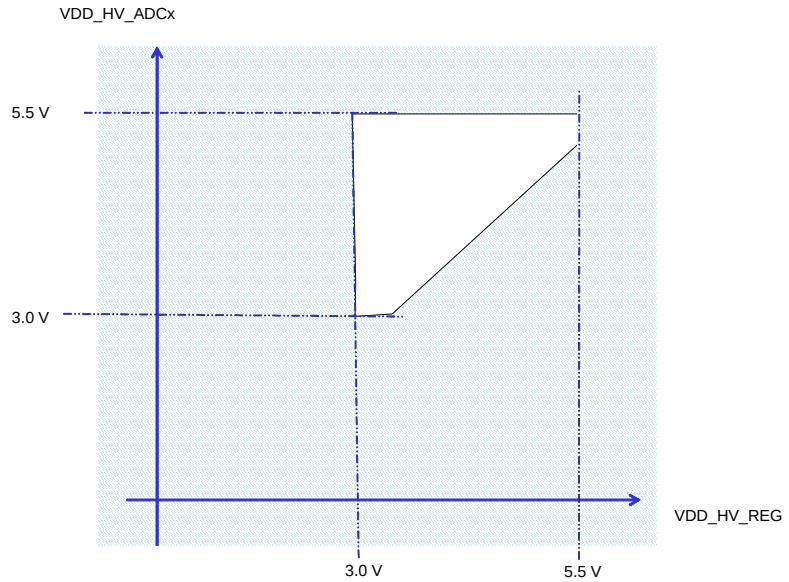
Figure 8. Power supplies constraints (3.0 V ≤ $V_{DD\_HV\_IOx}$ ≤ 5.5 V)



Note: IO AC and DC characteristics are guaranteed only in the range of 3.0–3.6 V when PAD3V5V is low, and in the range of 4.5–5.5 V when PAD3V5V is high.

The SPC560P34/SPC560P40 supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. *Figure 9* shows the constraints of the ADC power supply.

Figure 9. Independent ADC supply (3.0 V ≤ $V_{DD\_HV\_REG}$ ≤ 5.5 V)



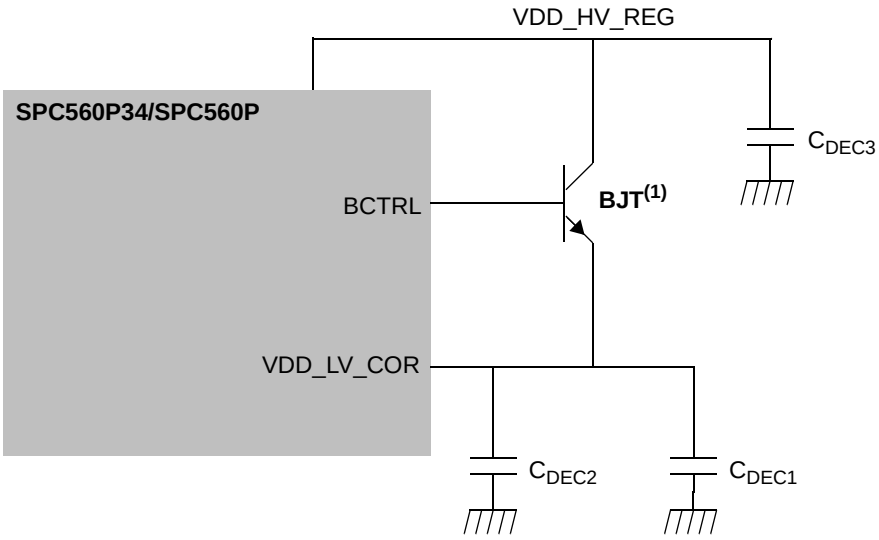
Note: The voltage regulator output cannot be used to drive external circuits. Output pins are to be used only for decoupling capacitance.

$V_{DD\_LV\_COR}$ must be generated using internal regulator and external NPN transistor. It is not possible to provide $V_{DD\_LV\_COR}$ through external regulator.

For the SPC560P34/SPC560P40 microcontroller, capacitor(s), with total values not below C_{DEC1}, should be placed between $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ close to external ballast transistor emitter. 4 capacitors, with total values not below C_{DEC2}, should be placed close to microcontroller pins between each $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ supply pairs and the $V_{DD\_LV\_REGCOR}/V_{SS\_LV\_REGCOR}$ pair . Additionally, capacitor(s) with total values not below C_{DEC3}, should be placed between the $V_{DD\_HV\_REG}/V_{SS\_HV\_REG}$ pins close to ballast collector. Capacitors values have to take into account capacitor accuracy, aging and variation versus temperature.

All reported information are valid for voltage and temperature ranges described in recommended operating condition, *Table 10* and *Table 11*.

Figure 10. Voltage regulator configuration



1. Refer to *Table 15*.

Table 15. Approved NPN ballast components

Part	Manufacturer	Approved derivatives(1)
BCP68	ON Semi	BCP68
	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10; BCX68-16; BCX-25
BC868	NXP	BC868

memory and 16 MHz RC oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated modules are set into a safe state.

Figure 11. Power-up typical sequence

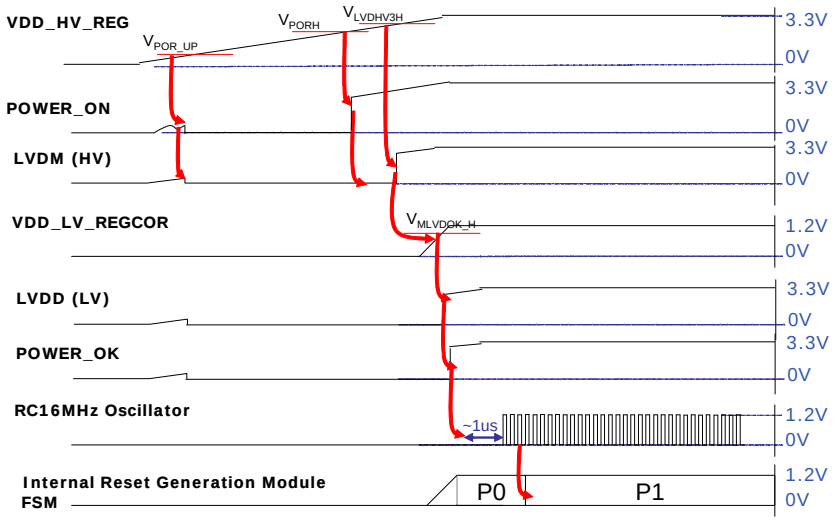


Figure 12. Power-down typical sequence

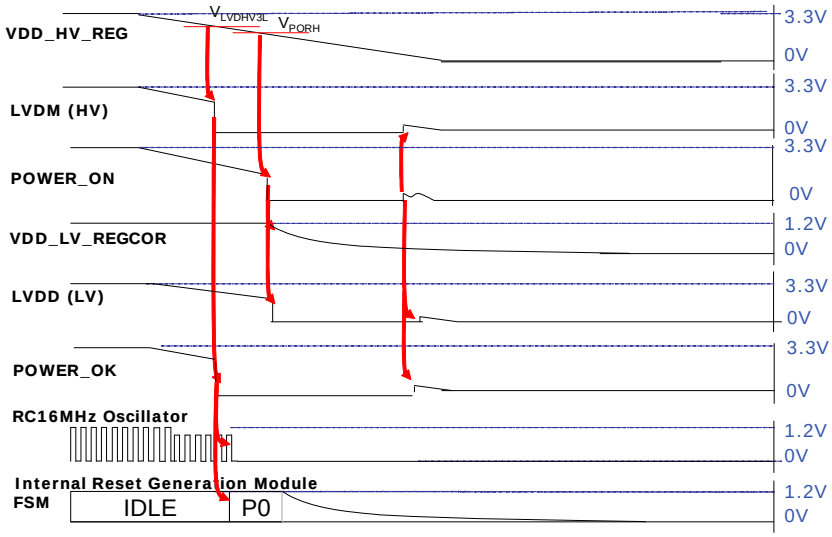
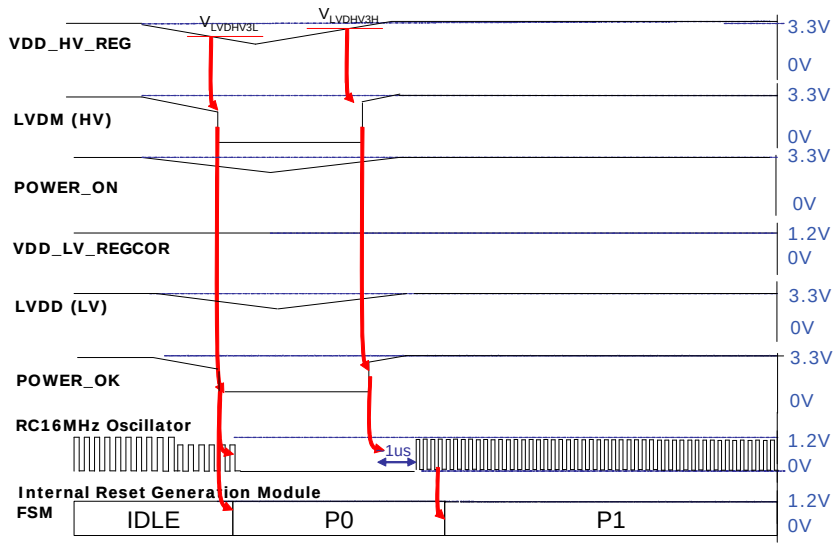


Figure 13. Brown-out typical sequence



3.10 DC electrical characteristics

3.10.1 NVUSRO register

Portions of the device configuration, such as high voltage supply and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. *Table 18* shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 18. PAD3V5V field description

Value(1)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

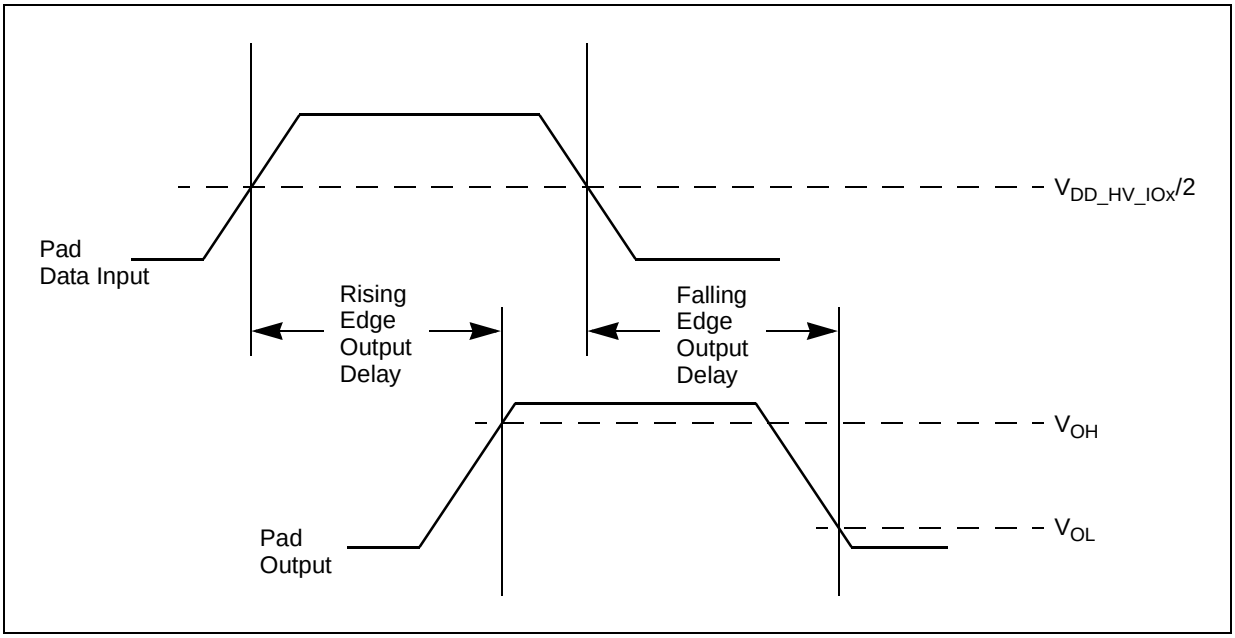
1. Default manufacturing value before flash initialization is ‘1’ (3.3 V).

Table 36. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	
t_{SYM}[3]	CC	T	Symmetric transition time, same drive strength between N and P transistor	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	4	ns
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified.
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).
3. Transition timing of both positive and negative slopes will differ maximum 50%.

Figure 19. Pad output delay



3.17 AC timing characteristics

3.17.1 $\overline{\text{RESET}}$ pin characteristics

The SPC560P34/SPC560P40 implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 20. Start-up reset requirements

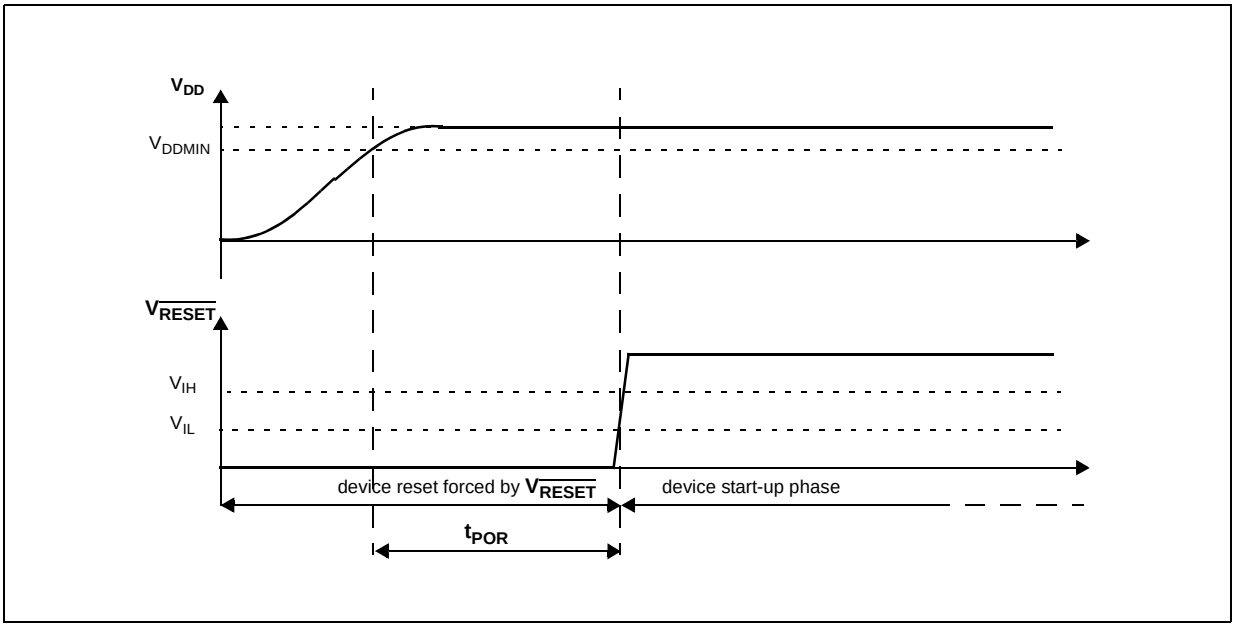
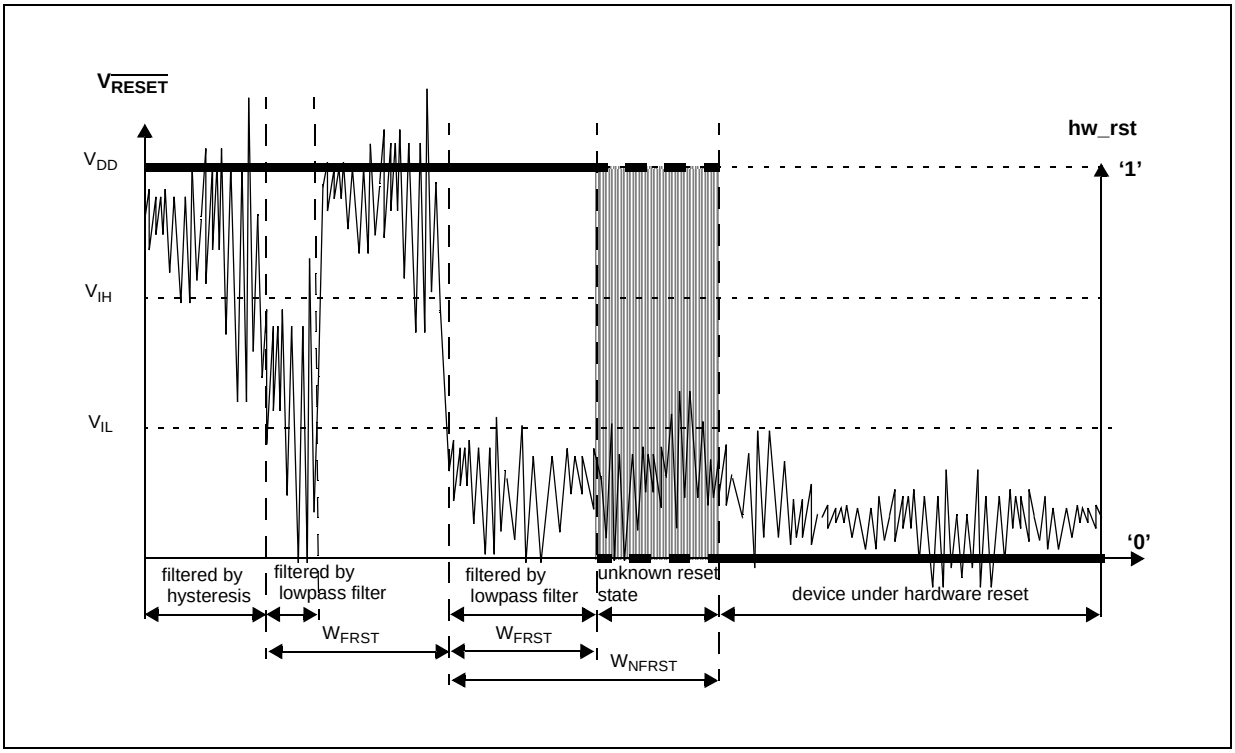


Figure 21. Noise filtering on reset signal



4. C_L includes device and package capacitance (C_{PKG} < 5 pF).
5. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}$/2)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing

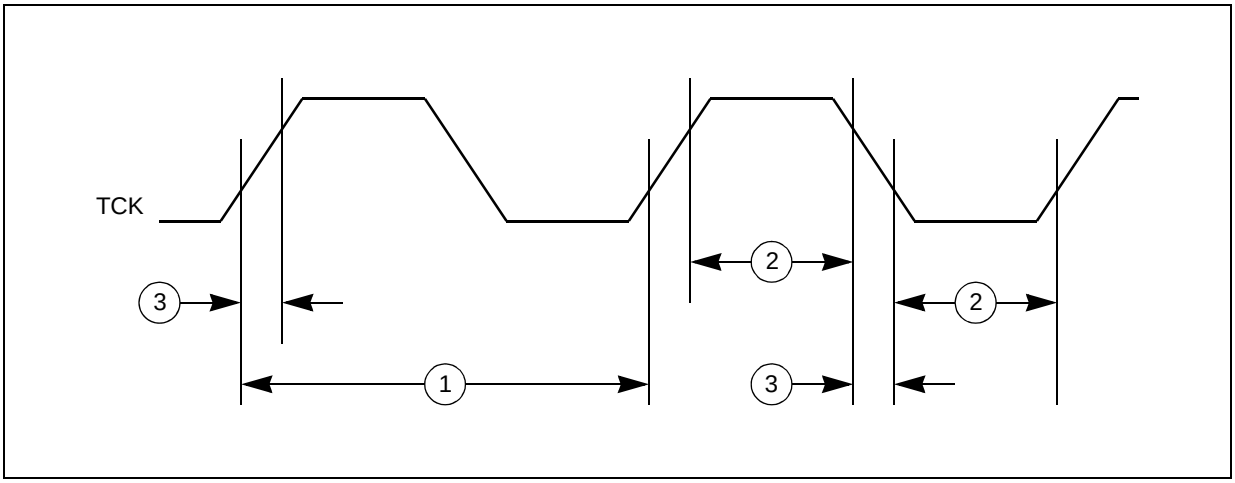
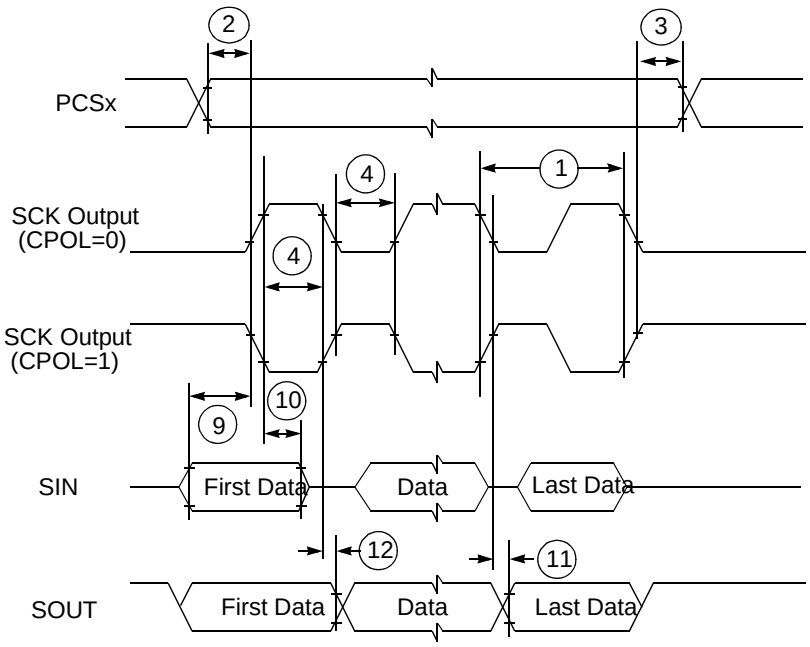


Table 41. DSPI timing(1) (continued)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

1. All timing are provided with 50 pF capacitance on output, 1 ns transition time on input signal

Figure 29. DSPI classic SPI timing – Master, CPHA = 0



Note: Numbers shown reference *Table 41*.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5 Ordering information

Figure 40. Commercial product code structure

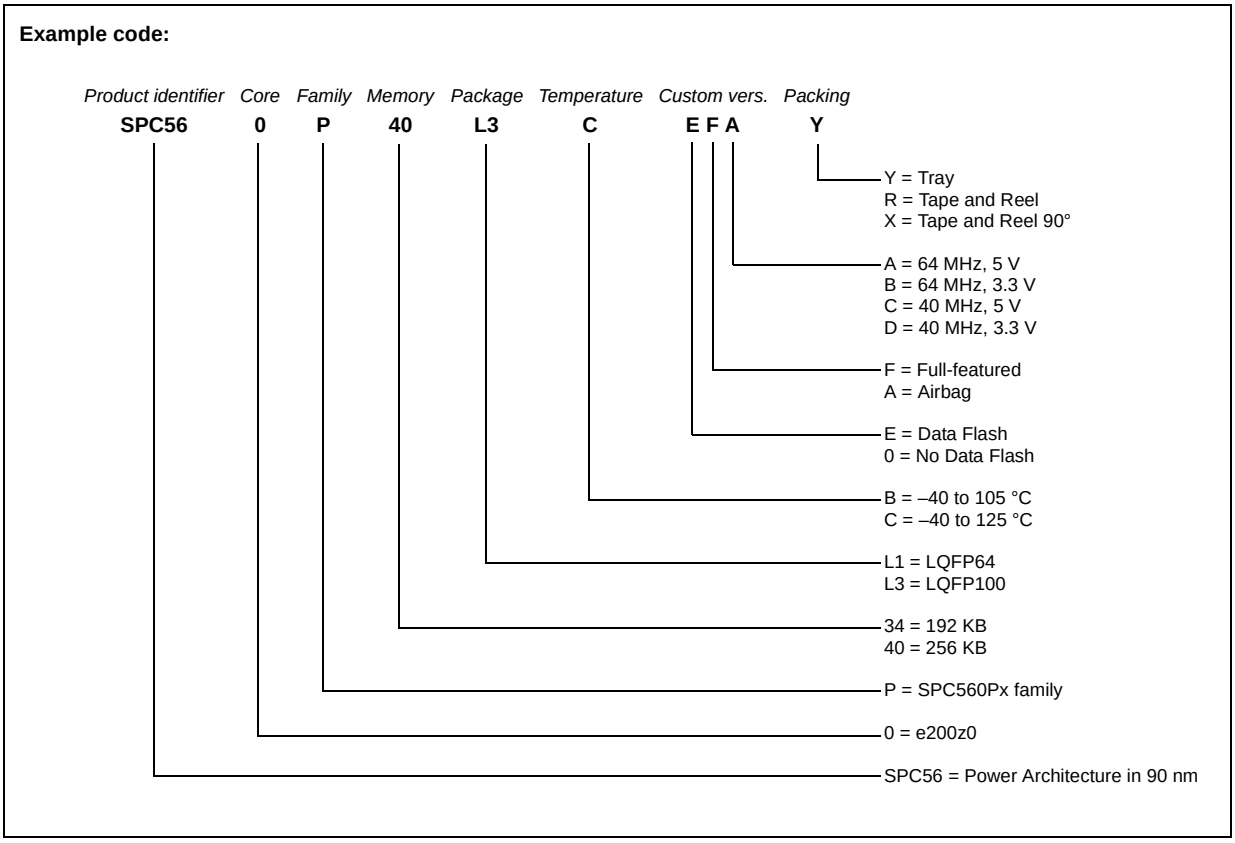


Table 45. Document revision history (continued)

Date	Revision	Changes
21-May-2010	2 (continued)	– Updated the “DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 0)“ section: – Deleted all rows concerning $\overline{\text{RESET}}$ – Deleted “I_{VPP}“ row – Added the max value for C_{IN} Added the “I/O pad current specification“ section Updated the Order codes table. Added “Appendix A”
23-Dec-2010	3	“Introduction” section: – Changed title (was “Overview“) – Updated contents “SPC560P34/SPC560P40 device comparison” table: – Added sentence above table – Removed “FlexRay” row – “FlexCAN” row: removed link to footnote 2 for SPC560P34 – Updated “Safety port” row for SPC560P34 – Updated “DSPI” row for SPC560P34 “SPC560P34/SPC560P40 block diagram”: added the following blocks: MC_CGM, MC_ME, MC_PCU, MC_RGM, CRC, and SSCM Added “SPC560P34/SPC560P40 series block summary” table “Pin muxing” section: removed information on “Symmetric pads” “Electrical characteristics” section: – Updated “Caution” note – Demoted “NVUSRO register” section to subsection of “DC electrical characteristics” section – “NVUSRO register” section: deleted “NVUSRO[WATCHDOG_EN] field description“ section Updated “EMI testing specifications” table “Low voltage monitor electrical characteristics” table: updated $V_{MLVDDOK\_H}$ max value “DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)” table: removed $_{VOL\_SYM}$, and V_{OH_SYM} rows “Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)” table: – $I_{DD\_LV\_CORE}$, RUN—Maximum mode, 40/64 MHz: updated typ/max values – $I_{DD\_LV\_CORE}$, RUN—Airbag mode, 40/64 MHz: updated typ/max values – $I_{DD\_LV\_CORE}$, RUN—Maximum mode, “P” parameter classification: removed – I_{DD_FLASH}: removed rows – I_{DD_ADC}, Maximum mode: updated typ/max values – I_{DD_OSC}: updated max value Updated “DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)” table “Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)” table: – $I_{DD\_LV\_CORE}$, RUN—Maximum mode, 40/64 MHz: updated typ/max values – $I_{DD\_LV\_CORE}$, RUN—Airbag mode, 40/64 MHz: updated typ/max values – I_{DD_FLASH}: removed rows – I_{DD_ADC}, Maximum mode: updated typ/max values – I_{DD_OSC}: updated max value Added “I/O consumption” table Removed “I/O weight” table

Table 45. Document revision history (continued)

Date	Revision	Changes
23-Dec-2010	3 (continued)	Updated “Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)” table Updated “Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)” table “Input clock characteristics” table: updated f_{CLK} max value “PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)” table: – Updated supply voltage range for V_{DDPLL} in the table title – Updated f_{SCM} max value – Updated C_{JITTER} row – Updated f_{MOD} max value Updated “16 MHz RC oscillator electrical characteristics” table Updated “ADC conversion characteristics” table “Program and erase specifications” table: – $T_{wprogram}$: updated initial max and max values – T_{BKPRG}, 64 KB: updated initial max and max values – added information about “erase time” for Data Flash “Flash module life” table: – P/E, 32 KB: added typ value – P/E, 128 KB: added typ value Replaced “Pad AC specifications (5.0 V, NVUSRO[PAD3V5V] = 0)” and “Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)” tables with “Output pin transition times” table “JTAG pin AC electrical characteristics” table: – t_{TDOV}: updated max value – t_{TDOHZ}: added min value and removed max value “Nexus debug port timing” table: removed the rows “t_{MCYC}”, “t_{MDOV}”, “t_{MSEOV}”, and “t_{EVTOV}” Updated “External interrupt timing (IRQ pin)” table Updated “FlexCAN timing” table Updated “DSPI timing” table Updated “Ordering information” section

Table 45. Document revision history (continued)

Date	Revision	Changes
13-May-2011	4 (continued)	Commercial product code structure: Replaced “Conditioning” with “Packing” *Table 44*: added “DUT”, “NPN”, and “RISC”
22-Dec-2011	5	Updated *Table 1: Device summary* Updated *Section 1.5.28: Nexus Development Interface (NDI)* *Section Table 2.: SPC560P34/SPC560P40 device comparison*: changed Nexus L1+ with Nexus Class 1 *Table 7: Pin muxing*: removed E[0] row *Table 9: Absolute maximum ratings*: updated minumum and maximum values for TV_{DD} parameter *Section 3.10: DC electrical characteristics*: Removed oscillator margin. Removed Section NVUSRO[OSCILLATOR_MARGIN] field description and Table NVUSRO[OSCILLATOR_MARGIN] field description Updated *Section 3.8.1: Voltage regulator electrical characteristics* Updated *Section Figure 10.: Voltage regulator configuration* *Table 16: Voltage regulator electrical characteristics*: added L_{Reg} row, updated condition for C_{DEC1}, C_{DEC2} and C_{DEC3} Removed “Order codes” tables
20-Dec-2012	6	*Table 9 (Absolute maximum ratings)*: updated TV_{DD} parameter, the minimum value to 3.0 V/s, added note on minimum value, and the maximum value to 0.5 V/µs *Table 20 (Supply current (5.0 V, NVUSRO[PAD3V5V] = 0))*: added $I_{DD\_HV\_REG}$ row *Table 22 (Supply current (3.3 V, NVUSRO[PAD3V5V] = 1))*: added $I_{DD\_HV\_REG}$ row Updated *Section 3.14.1, Input impedance and ADC accuracy* *Table 30 (ADC conversion characteristics)*: renamed “R_{SW1}” in “R_{SW}” *Table 31 (Program and erase specifications)*: added t_{ESRT} row
18-Sep-2013	7	Updated Disclaimer.