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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p40l3beaay

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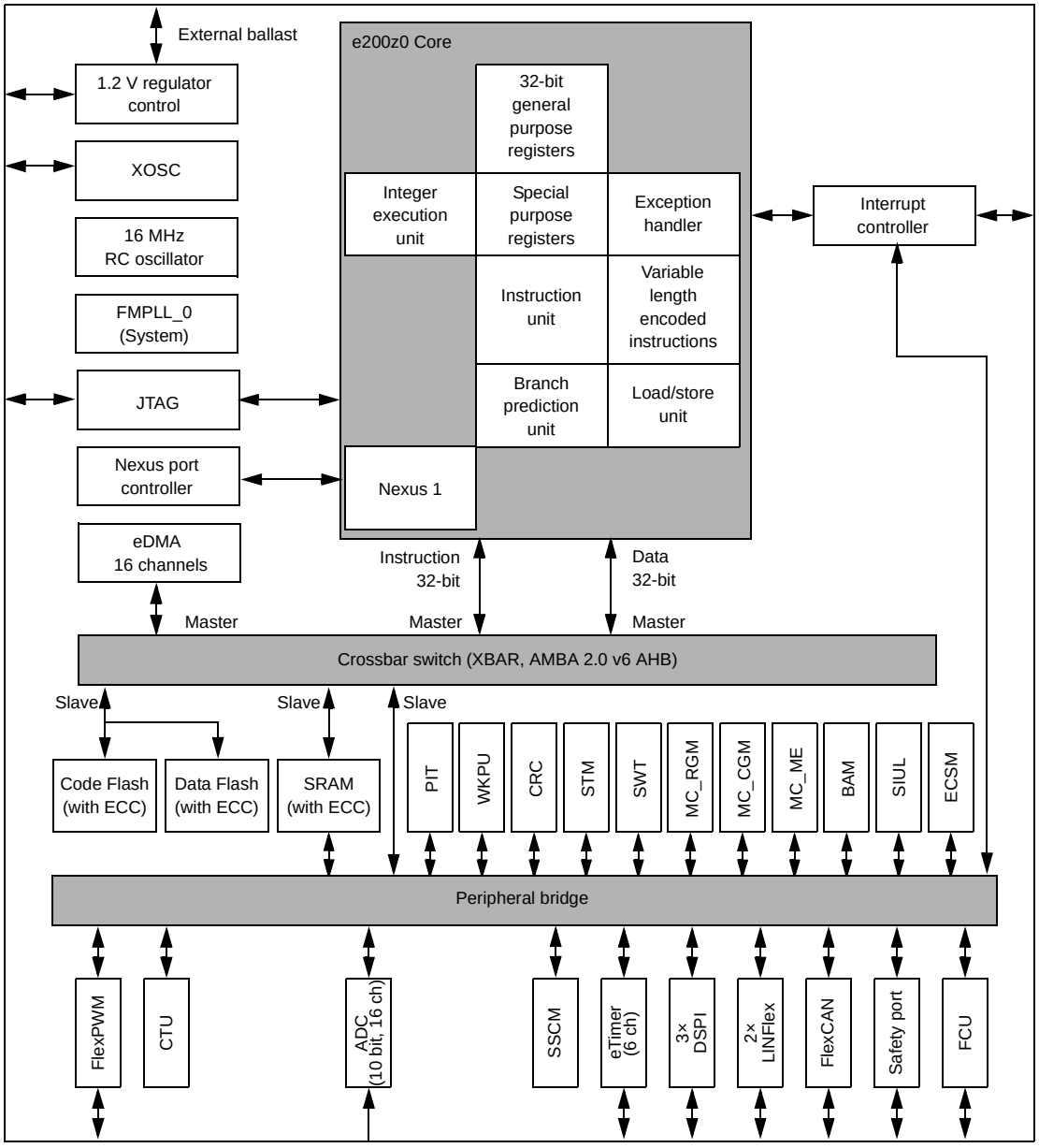
Table 2. SPC560P34/SPC560P40 device comparison (continued)

Feature		SPC560P34 Full-featured	SPC560P40 Full-featured
eDMA (enhanced direct memory access) channels		16	
FlexCAN (controller area network)		1(1)	2(1),(2)
Safety port		No	Yes (via second FlexCAN module)
FCU (fault collection unit)		Yes	
CTU (cross triggering unit)		Yes	Yes
eTimer		1 (16-bit, 6 channels)	
FlexPWM (pulse-width modulation) channels		8 (capture capabity not supported)	8 (capture capability not supported)
Analog-to-digital converter (ADC)		1 (10-bit, 16 channels)	
LINFlex		2 (1 × Master/Slave, 1 × Master only)	2 (1 × Master/Slave, 1 × Master only)
DSPI (deserial serial peripheral interface)		2	3
CRC (cyclic redundancy check) unit		Yes	
Junction temperature sensor		No	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Nexus Class 1)	
Supply	Digital power supply(3)	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		LQFP64 LQFP100	
Temperature	Standard ambient temperature	–40 to 125 °C	

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a safety port with a bit rate as high as 8 Mbit/s at 64 MHz.
3. The different supply voltages vary according to the part number ordered.

SPC560P34/SPC560P40 is available in two configurations having different features: Full-featured and airbag. *Table 3* shows the main differences between the two versions of the SPC560P40 MCU.

Figure 1. Block diagram (SPC560P40 full-featured configuration)



Legend:

ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System Integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

Table 4. SPC560P34/SPC560P40 series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Is the interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures. For pin signal descriptions, please refer to *Table 7*.

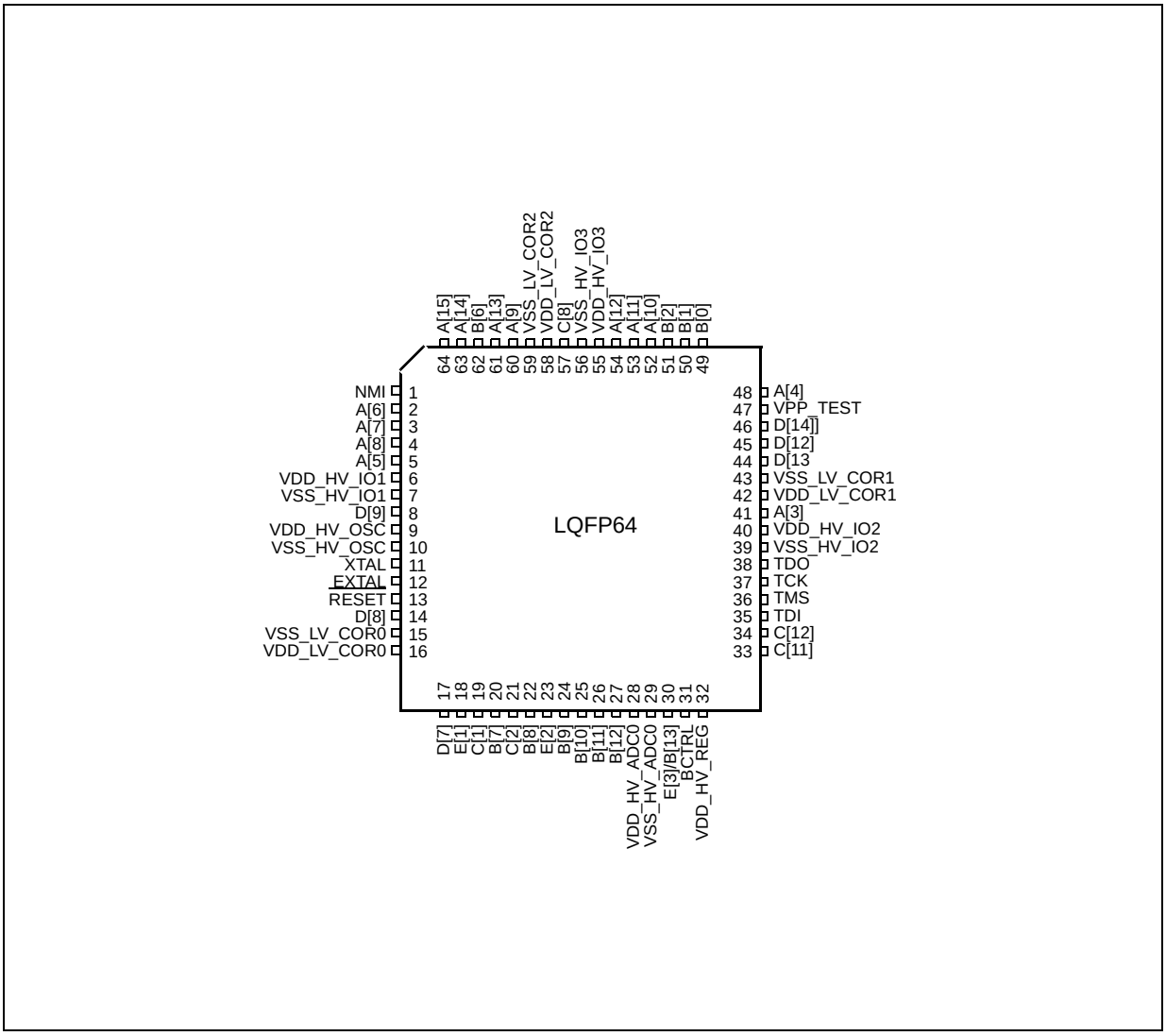


Figure 2. 64-pin LQFP pinout – Full featured configuration (top view)

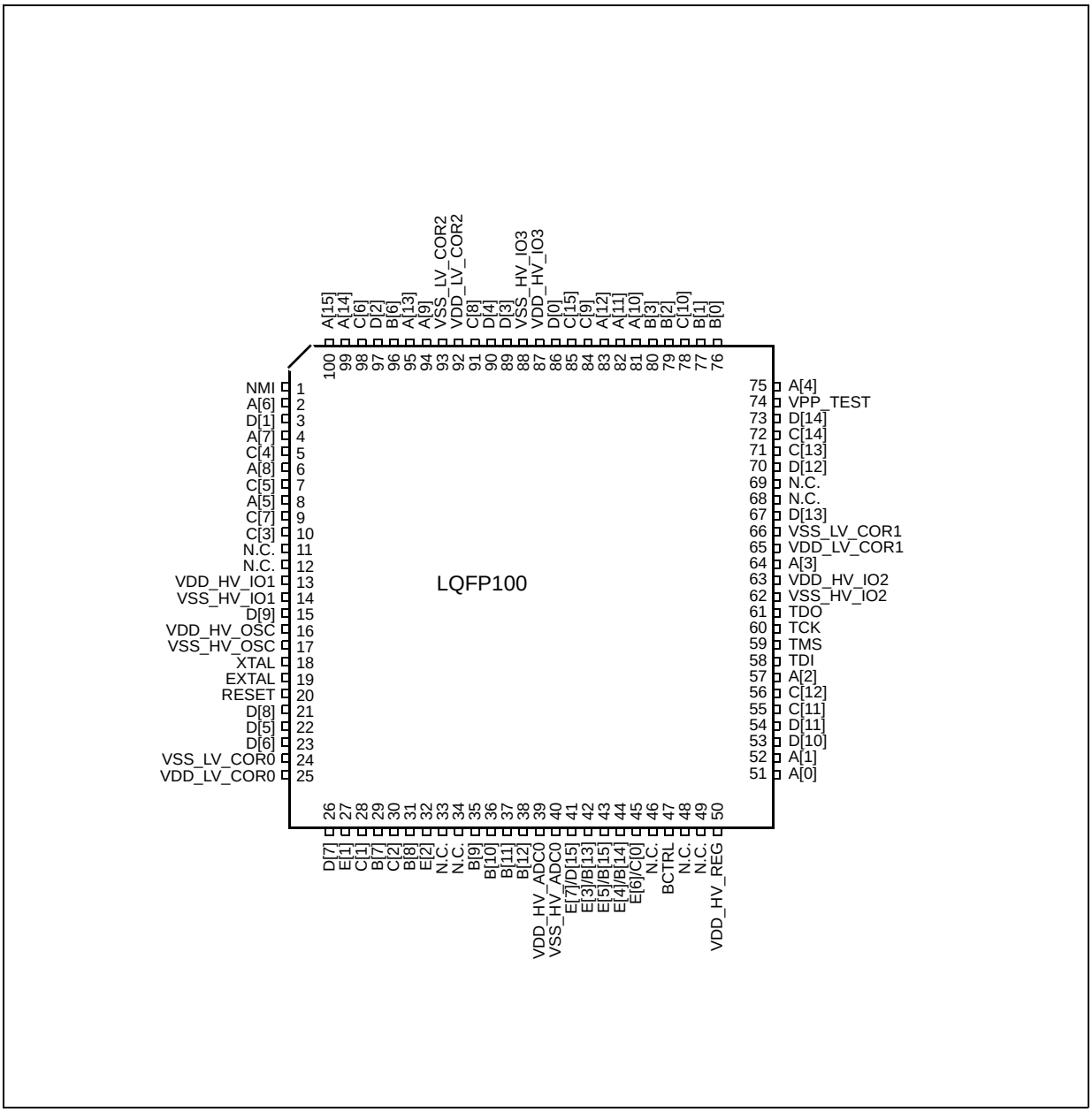


Figure 4. 100-pin LQFP pinout – Full featured configuration (top view)

Table 5. Supply pins (continued)

Supply		Pin	
Symbol	**Description**	**64-pin**	**100-pin**
$V_{DD\_LV\_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	58	92
$V_{SS\_LV\_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD\_LV\_COR}$ pin.	59	93

1. Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on $V_{DD\_HV\_ADCx}$/$V_{SS\_HV\_ADCx}$ pins.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC560P34/SPC560P40 devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective pad configuration register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad speed(1)		Pin	
			SRC = 0	SRC = 1	64-pin	100-pin
Dedicated pins						
NMI	Non-maskable Interrupt	Input only	Slow	—	1	1
XTAL	Analog output of the oscillator amplifier circuit—needs to be grounded if oscillator is used in bypass mode	—	—	—	11	18
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode Analog input for the clock generator when the oscillator is in bypass mode	—	—	—	12	19
TDI	JTAG test data input	Input only	Slow	—	35	58
TMS	JTAG state machine control	Input only	Slow	—	36	59
TCK	JTAG clock	Input only	Slow	—	37	60
TDO	JTAG test data output	Output only	Slow	Fast	38	61
Reset pin						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	13	20
Test pin						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	47	74

1. SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2.2.3 Pin multiplexing

Table 7 defines the pin list and muxing for the SPC560P34/SPC560P40 devices.

Each row of *Table 7* shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

SPC560P34/SPC560P40 devices provide three main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see “Pad AC Specifications” in the device datasheet.

Table 7. Pin muxing

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O I/O O I	Slow	Medium	—	51
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	—	52
A[2]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O — O I I I	Slow	Medium	—	57
A[3]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	41	64

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD — DEBUG[2] EIRQ[17]	SIUL LIN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	51	79
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — — DEBUG[3] RXD	SIUL — — SSCM LIN_0	I/O — — — I	Slow	Medium	—	80
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] CLKOUT CS2 — EIRQ[18]	SIUL Control DSPI_2 — SIUL	I/O O O — I	Slow	Medium	62	96
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LIN_0	Input only	—	—	20	29
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input only	—	—	22	31
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIUL — — — ADC_0	Input only	—	—	24	35
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIUL — — — ADC_0	Input only	—	—	25	36

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 —	GPIO[33] — — — AN[2]	SIUL — — — ADC_0	Input only	—	—	19	28
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 —	GPIO[34] — — — AN[3]	SIUL — — — ADC_0	Input only	—	—	21	30
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 —	GPIO[35] CS1 — TXD EIRQ[21]	SIUL DSPI_0 — LIN_1 SIUL	I/O O — O I	Slow	Medium	—	10
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 —	GPIO[36] CS0 X[1] DEBUG[4] EIRQ[22]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O I/O O — I	Slow	Medium	—	5
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 —	GPIO[37] SCK — DEBUG[5] EIRQ[23]	SIUL DSPI_0 — SSCM SIUL	I/O I/O — — I	Slow	Medium	—	7
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT B[1] DEBUG[6] EIRQ[24]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O O O — I	Slow	Medium	—	98
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 —	GPIO[39] — A[1] DEBUG[7] SIN	SIUL — FlexPWM_0 SSCM DSPI_0	I/O — O — I	Slow	Medium	—	9
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3	GPIO[40] CS1 — CS6	SIUL DSPI_1 — DSPI_0	I/O O — O	Slow	Medium	57	91

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3	GPIO[49] — — EXT_TRG	SIUL — — CTU_0	I/O — — O	Slow	Medium	—	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3	GPIO[50] — — X[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	97
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] — — A[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	89
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] — — B[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	90
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] —	SIUL DSPI_0 FCU_0 —	I/O O O —	Slow	Medium	—	22
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 — — FAULT[1]	SIUL DSPI_0 — — FlexPWM_0	I/O O — — I	Slow	Medium	—	23
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3	GPIO[55] CS3 F[1] CS4	SIUL DSPI_1 FCU_0 DSPI_0	I/O O O O	Slow	Medium	17	26
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2 — CS5	SIUL DSPI_1 — DSPI_0	I/O O — O	Slow	Medium	14	21
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIUL FlexPWM_0 LIN_1 —	I/O O O —	Slow	Medium	8	15
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	53

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	44
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input only	—	—	—	43
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input only	—	—	—	45
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input only	—	—	—	41

1. ALT0 is the primary (default) function for each port after reset.
2. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 → ALT0; PCR.PA = 01 → ALT1; PCR.PA = 10 → ALT2; PCR.PA = 11 → ALT3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
3. Module included on the MCU.
4. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
5. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
6. ADC0.AN emulates ADC1.AN. This feature is used to provide software compatibility between SPC560P34/SPC560P40 and SPC560P50. Refer to ADC chapter of reference manual for more details.

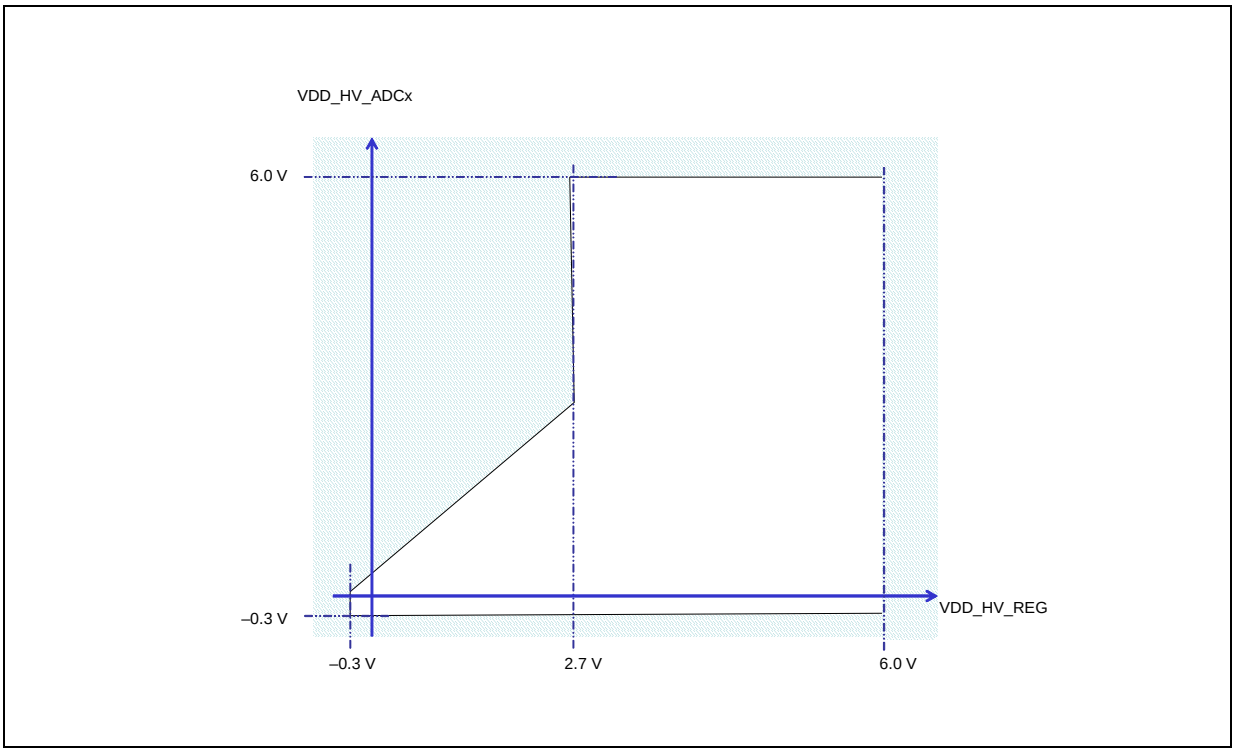


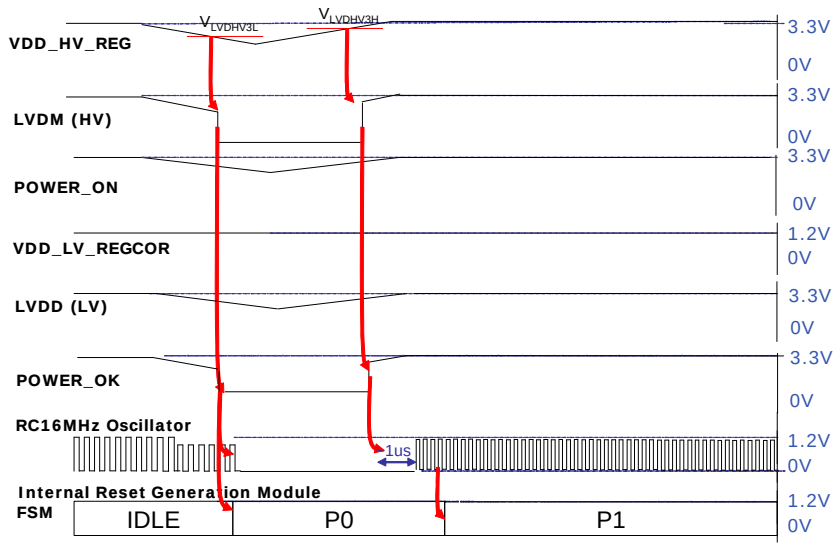
Figure 7. Independent ADC supply (–0.3 V ≤ $V_{DD\_HV\_REG}$ ≤ 6.0 V)

3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	

Figure 13. Brown-out typical sequence



3.10 DC electrical characteristics

3.10.1 NVUSRO register

Portions of the device configuration, such as high voltage supply and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. *Table 18* shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 18. PAD3V5V field description

Value(1)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. Default manufacturing value before flash initialization is ‘1’ (3.3 V).

3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 23*.

Table 23. I/O supply segment

Package	Supply segment				
	1	2	3	4	5
LQFP100	pin15–pin26	pin27–pin46	pin51–pin61	pin64–pin86	pin89–pin10
LQFP64	pin8–pin17	pin18–pin30	pin33–pin38	pin41–pin54	pin57–pin5

Table 24. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	

Table 24. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.11 Main oscillator electrical characteristics

The SPC560P34/SPC560P40 provides an oscillator/resonator driver.

Table 25. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{OSC}	SR	—	Oscillator frequency		4	40	MHz
g_m	—	P	Transconductance		6.5	25	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin		1	—	V
t_{OSCSU}	—	T	Start-up time[1],[2]		8	—	ms
C_L	CC	T	XTAL load capacitance[3]	4 MHz	5	30	pf
		T		8 MHz	5	26	
		T		12 MHz	5	23	
		T		16 MHz	5	19	
		T		20 MHz	5	16	
		T		40 MHz	5	8	

1. The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL
3. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

Table 26. Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{OSC}	SR	—	Oscillator frequency		4	40	MHz
g_m	—	P	Transconductance		4	20	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin		1	—	V
t_{OSCSU}	—	T	Start-up time(1),(2)		8	—	ms
C_L	CC	T	XTAL load capacitance(3)	4 MHz	5	30	pf
		T		8 MHz	5	26	
		T		12 MHz	5	23	
		T		16 MHz	5	19	
		T		20 MHz	5	16	
		T		40 MHz	5	8	

1. The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL
3. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

Table 27. Input clock characteristics

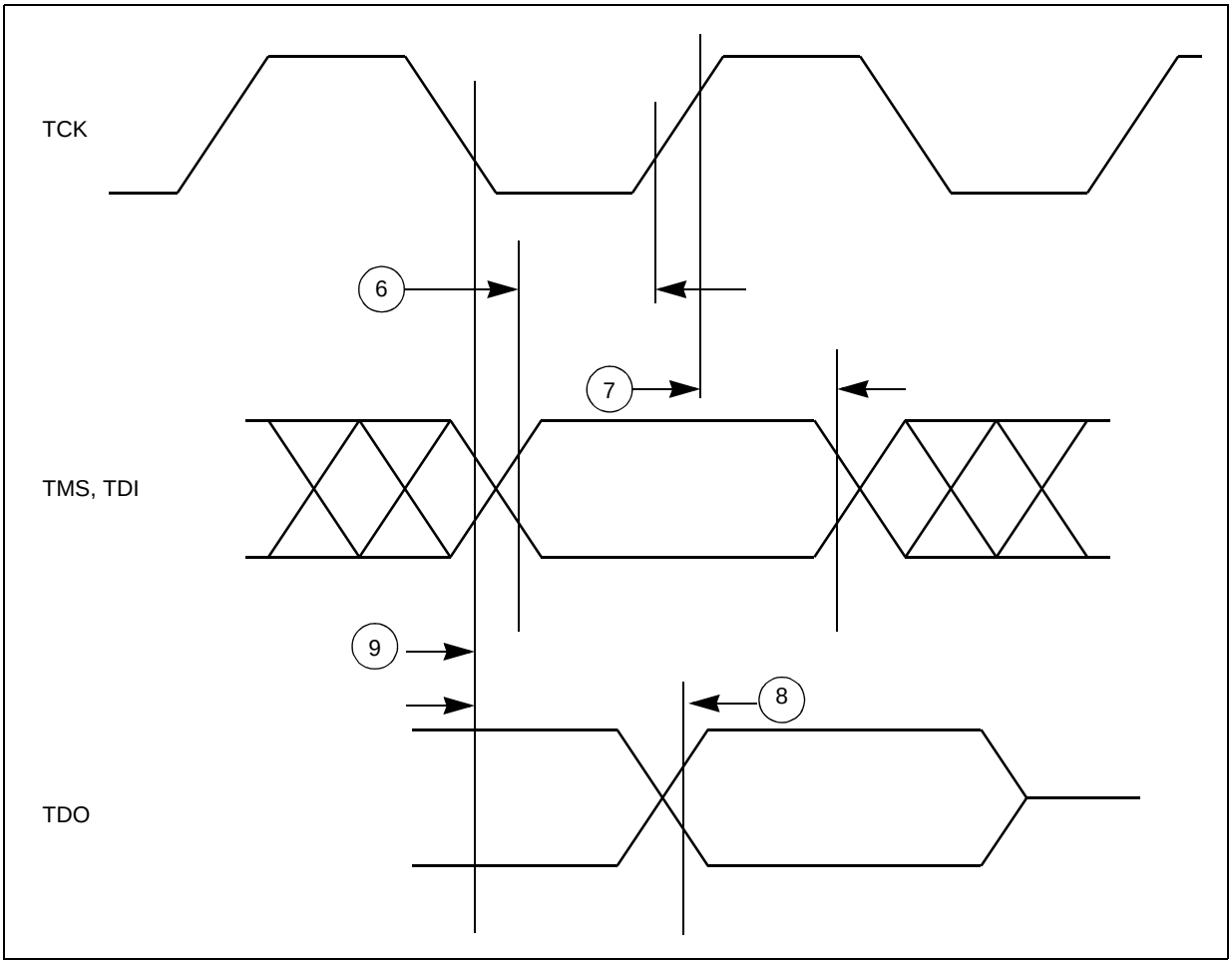
Symbol		Parameter	Value			Unit
			Min	Typ	Max	
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	64	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.12 FMPLL electrical characteristics

Table 28. FMPLL electrical characteristics

Symbol	C	Parameter	Conditions(1)	Value		Unit
				Min	Max	
$f_{ref\_crystal}$ f_{ref_ext}	D	PLL reference frequency range(2)	Crystal reference	4	40	MHz
f_{PLLIN}	D	Phase detector input frequency range (after pre-divider)	—	4	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	16	64	MHz

Figure 27. Nexus TDI, TMS, TDO timing



3.17.4 External interrupt timing (IRQ pin)

Table 40. External interrupt timing(1)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{IPWL}	CC	D	IRQ pulse width low	—	4	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	4	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time(2)	—	4 + N (3)	—	t_{CYC}

1. IRQ timing specified at f_{SYS} = 64 MHz and $V_{DD\_HV\_IOx}$ = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.
3. N = ISR time to clear the flag