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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p40l3beabr

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Table 2. SPC560P34/SPC560P40 device comparison (continued)

Feature		SPC560P34 Full-featured	SPC560P40 Full-featured
eDMA (enhanced direct memory access) channels		16	
FlexCAN (controller area network)		1(1)	2(1),(2)
Safety port		No	Yes (via second FlexCAN module)
FCU (fault collection unit)		Yes	
CTU (cross triggering unit)		Yes	Yes
eTimer		1 (16-bit, 6 channels)	
FlexPWM (pulse-width modulation) channels		8 (capture capabity not supported)	8 (capture capability not supported)
Analog-to-digital converter (ADC)		1 (10-bit, 16 channels)	
LINFlex		2 (1 × Master/Slave, 1 × Master only)	2 (1 × Master/Slave, 1 × Master only)
DSPI (deserial serial peripheral interface)		2	3
CRC (cyclic redundancy check) unit		Yes	
Junction temperature sensor		No	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Nexus Class 1)	
Supply	Digital power supply(3)	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		LQFP64 LQFP100	
Temperature	Standard ambient temperature	–40 to 125 °C	

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a safety port with a bit rate as high as 8 Mbit/s at 64 MHz.
3. The different supply voltages vary according to the part number ordered.

SPC560P34/SPC560P40 is available in two configurations having different features: Full-featured and airbag. *Table 3* shows the main differences between the two versions of the SPC560P40 MCU.

1.5.22 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the SPC560P34/SPC560P40 features the following:

- Supports LIN Master mode (both instances), LIN Slave mode (only one instance) and UART mode
- LIN state machine compliant to LIN1.3, 2.0 and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to 8 data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features:
  - Autonomous LIN header handling
  - Autonomous LIN response handling
  - Optional discarding of irrelevant LIN responses using ID filter
- UART mode:
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

1.5.23 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC560P34/SPC560P40 MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 8 chip select lines available:
  - 8 on DSPI_0
  - 4 each on DSPI_1 and DSPI_2
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- Queueing operation possible through use of the I/O processor or eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.24 Pulse width modulator (FlexPWM)

The pulse width modulator module (PWM) contains four PWM submodules each of which is set up to control a single half-bridge power stage. There are also three fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

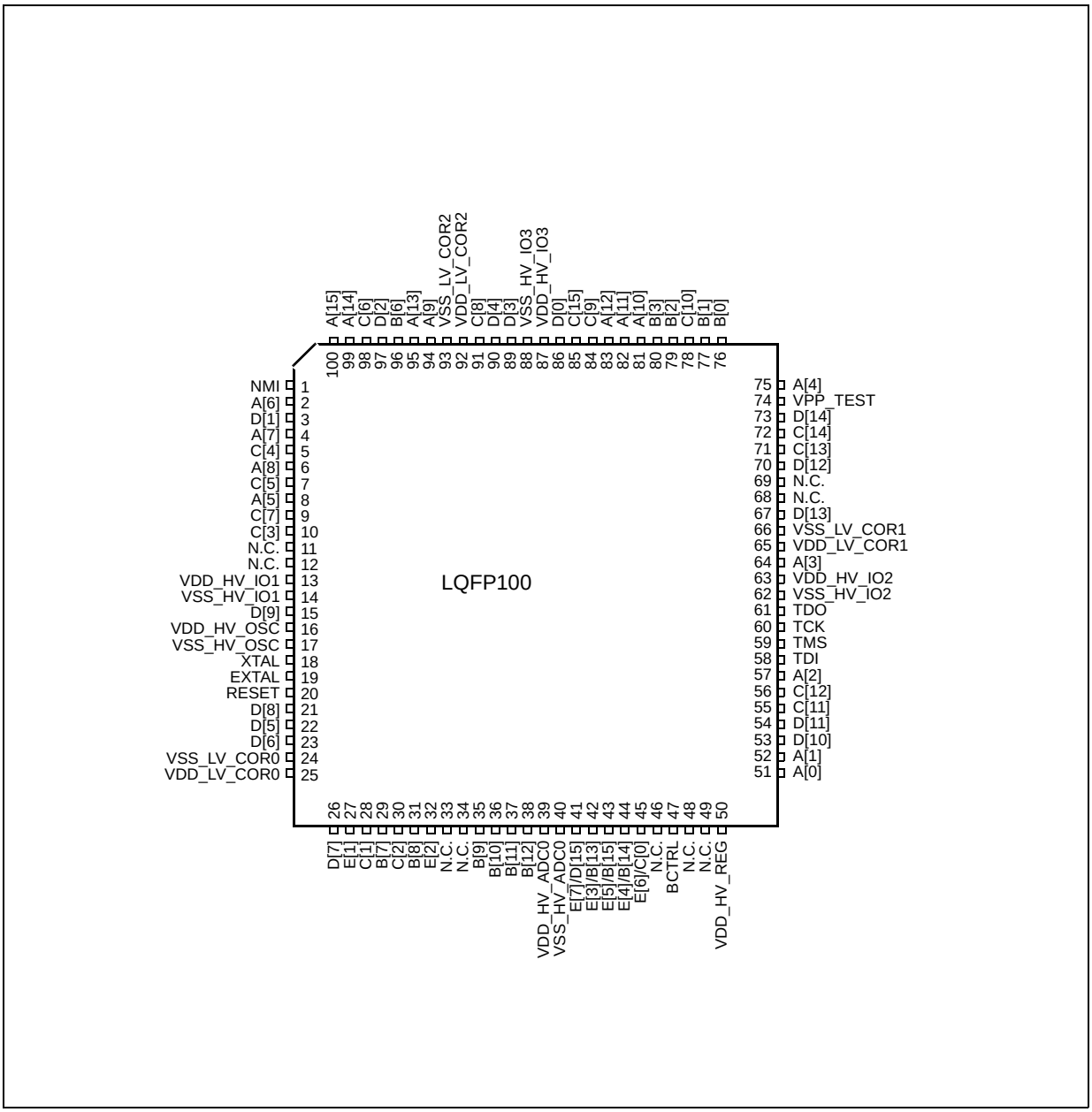


Figure 5. 100-pin LQFP pinout – Airbag configuration (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC560P34/SPC560P40 devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC560P34/SPC560P40 devices.

Table 5. Supply pins

Supply		Pin	
Symbol	**Description**	**64-pin**	**100-pin**
VREG control and power supply pins. Pins available on 64-pin and 100-pin packages			
BCTRL	Voltage regulator external NPN ballast base control pin	31	47
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	32	50
ADC_0 reference and supply voltage. Pins available on 64-pin and 100-pin packages			
$V_{DD\_HV\_ADC0}$(1)	ADC_0 supply and high reference voltage	28	39
$V_{SS\_HV\_ADC0}$	ADC_0 ground and low reference voltage	29	40
Power supply pins (3.3 V or 5.0 V). Pins available on 64-pin and 100-pin packages			
$V_{DD\_HV\_IO1}$	Input/output supply voltage	6	13
$V_{SS\_HV\_IO1}$	Input/output ground	7	14
$V_{DD\_HV\_IO2}$	Input/output supply voltage and data Flash memory supply voltage	40	63
$V_{SS\_HV\_IO2}$	Input/output ground and Flash memory HV ground	39	62
$V_{DD\_HV\_IO3}$	Input/output supply voltage and code Flash memory supply voltage	55	87
$V_{SS\_HV\_IO3}$	Input/output ground and code Flash memory HV ground	56	88
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	9	16
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	10	17
Power supply pins (1.2 V). Pins available on 64-pin and 100-pin packages			
$V_{DD\_LV\_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	16	25
$V_{SS\_LV\_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	15	24
$V_{DD\_LV\_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	42	65
$V_{SS\_LV\_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	43	66

Table 5. Supply pins (continued)

Supply		Pin	
Symbol	**Description**	**64-pin**	**100-pin**
$V_{DD\_LV\_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	58	92
$V_{SS\_LV\_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD\_LV\_COR}$ pin.	59	93

1. Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on $V_{DD\_HV\_ADCx}$/$V_{SS\_HV\_ADCx}$ pins.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC560P34/SPC560P40 devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective pad configuration register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad speed(1)		Pin	
			SRC = 0	SRC = 1	64-pin	100-pin
Dedicated pins						
NMI	Non-maskable Interrupt	Input only	Slow	—	1	1
XTAL	Analog output of the oscillator amplifier circuit—needs to be grounded if oscillator is used in bypass mode	—	—	—	11	18
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode Analog input for the clock generator when the oscillator is in bypass mode	—	—	—	12	19
TDI	JTAG test data input	Input only	Slow	—	35	58
TMS	JTAG state machine control	Input only	Slow	—	36	59
TCK	JTAG clock	Input only	Slow	—	37	60
TDO	JTAG test data output	Output only	Slow	Fast	38	61
Reset pin						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	13	20
Test pin						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	47	74

1. SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

Table 9. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(2)	
I_{INJSUM}	S R	Absolute sum of all input currents during overload condition	—	–50	50	mA
T_{STG}	S R	Storage temperature	—	–55	150	°C
T_J	S R	Junction temperature under bias	—	–40	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages.
3. The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 300$ mV.
4. Guaranteed by device validation.
5. Minimum value of TV_{DD} must be guaranteed until $V_{DD\_HV\_REG}$ reaches 2.6 V (maximum value of V_{PORH})
6. Only when $V_{DD\_HV\_IOx} < 5.2$ V

Figure 6 shows the constraints of the different power supplies.

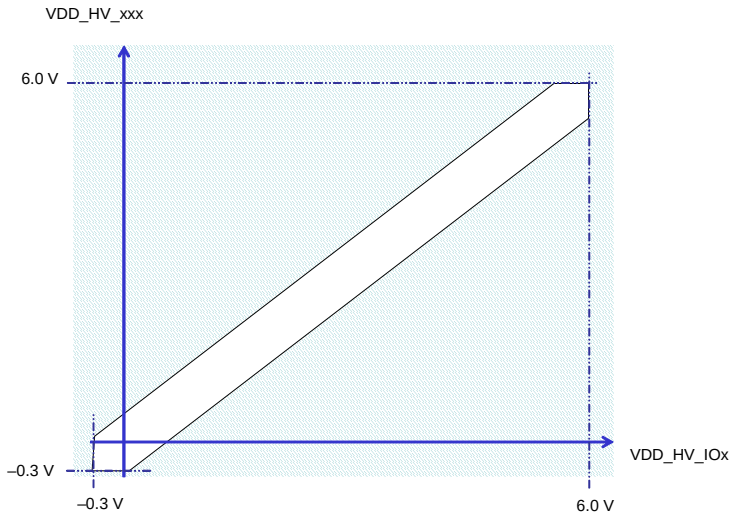


Figure 6. Power supplies constraints (–0.3 V ≤ $V_{DD\_HV\_IOx}$ ≤ 6.0 V)

The SPC560P34/SPC560P40 supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. *Figure 7* shows the constraints of the ADC power supply.

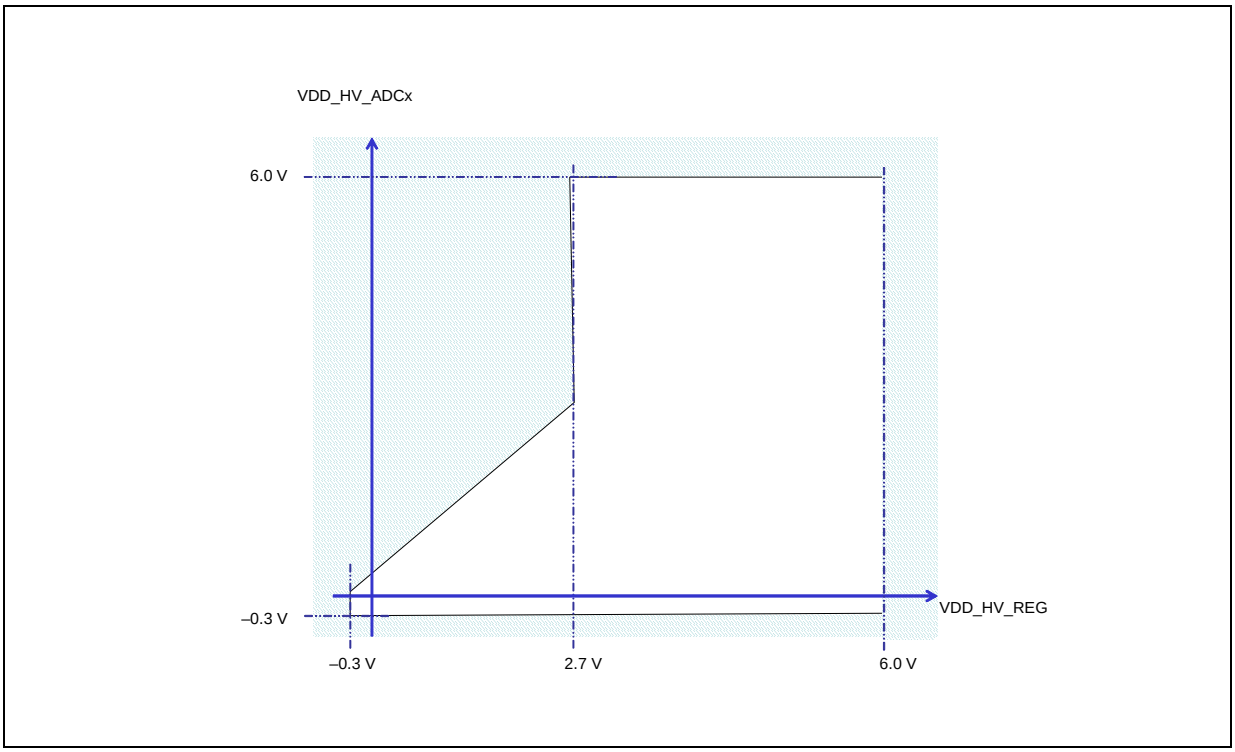


Figure 7. Independent ADC supply (–0.3 V ≤ $V_{DD\_HV\_REG}$ ≤ 6.0 V)

3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. LQFP thermal characteristics

Symbol	Parameter	Conditions	Typical value		Unit
			100-pin	64-pin	
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	63	57	°C/W
		Four layer board—2s2p	51	41	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board(2)	Four layer board—2s2p	33	22	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	15	13	°C/W
Ψ_{JB}	Junction-to-board, natural convection(4)	Operating conditions	33	22	°C/W
Ψ_{JC}	Junction-to-case, natural convection(5)	Operating conditions	1	1	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as RthJB or Theta-JB.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1: $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

memory and 16 MHz RC oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated modules are set into a safe state.

Figure 11. Power-up typical sequence

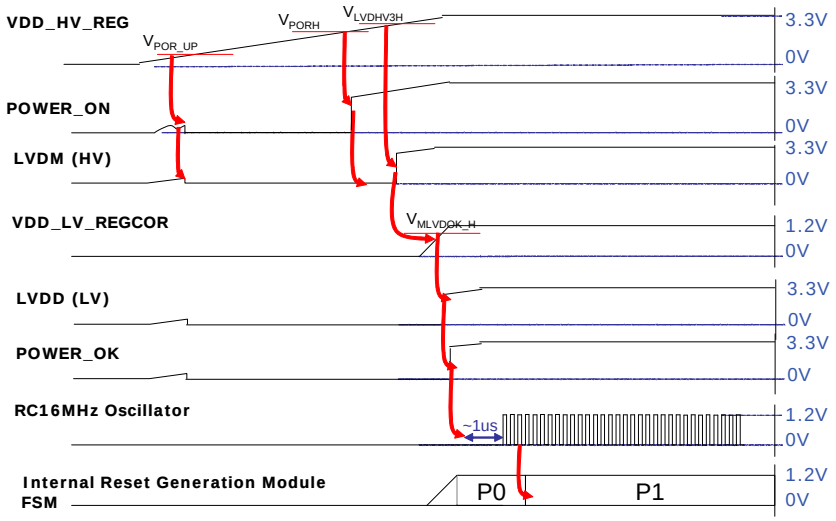


Figure 12. Power-down typical sequence

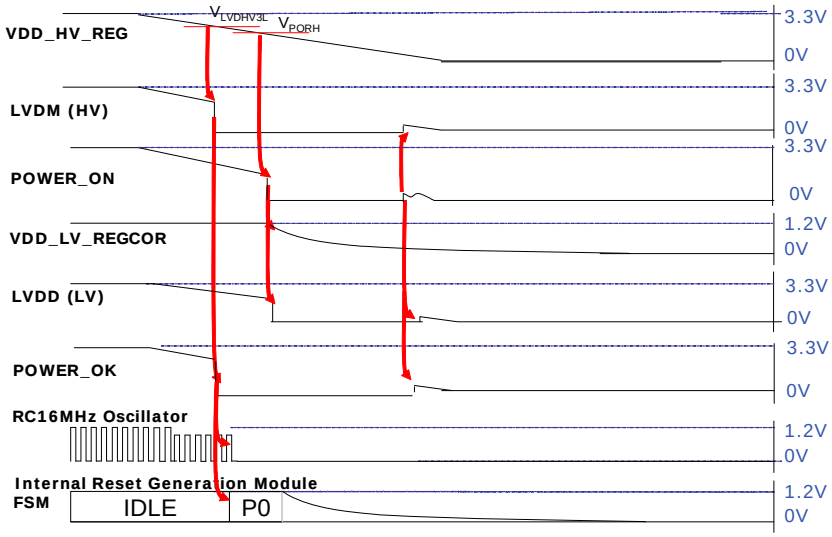
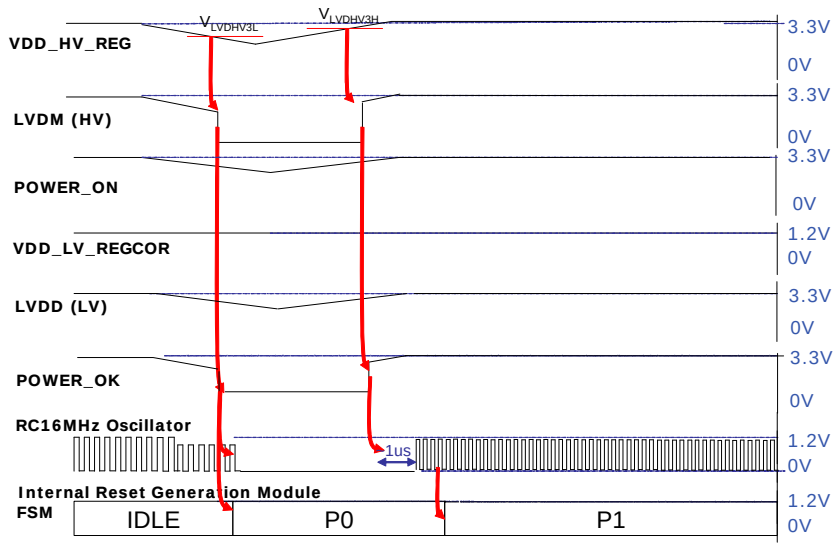


Figure 13. Brown-out typical sequence



3.10 DC electrical characteristics

3.10.1 NVUSRO register

Portions of the device configuration, such as high voltage supply and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. *Table 18* shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 18. PAD3V5V field description

Value(1)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. Default manufacturing value before flash initialization is ‘1’ (3.3 V).

Table 24. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.11 Main oscillator electrical characteristics

The SPC560P34/SPC560P40 provides an oscillator/resonator driver.

Table 25. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{OSC}	SR	—	Oscillator frequency		4	40	MHz
g_m	—	P	Transconductance		6.5	25	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin		1	—	V
t_{OSCSU}	—	T	Start-up time[1],[2]		8	—	ms
C_L	CC	T	XTAL load capacitance[3]	4 MHz	5	30	pf
		T		8 MHz	5	26	
		T		12 MHz	5	23	
		T		16 MHz	5	19	
		T		20 MHz	5	16	
		T		40 MHz	5	8	

1. The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL
3. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

Table 28. FMPLL electrical characteristics (continued)

Symbol	C	Parameter		Conditions[1]	Value		Unit
					Min	Max	
f_{FREE}	P	Free-running frequency		Measured using clock division—typically /16	20	150	MHz
t_{CYC}	D	System clock period		—	—	1 / f_{SYS}	ns
f_{LORL}	D	Loss of reference frequency window[3]		Lower limit	1.6	3.7	MHz
f_{LORH}	D			Upper limit	24	56	
f_{SCM}	D	Self-clocked mode frequency[4],[5]		—	20	150	MHz
C_{JITTER}	T	CLKOUT period jitter[6],[7],[8],[9]	Short-term jitter[10]	f_{SYS} maximum	–4	4	% f_{CLKOUT}
			Long-term jitter (average over 2 ms interval)	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 64 MHz, 4000 cycles	—	10	ns
t_{lpll}	D	PLL lock time[11], [12]		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	–6	6	% f_{SYS}
f_{UL}	D	Frequency un-LOCK range		—	–18	18	% f_{SYS}
f_{CS}	D	Modulation depth		Center spread	±0.25	±4.0 (13)	% f_{SYS}
f_{DS}	D			Down spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency[14]		—	—	70	kHz

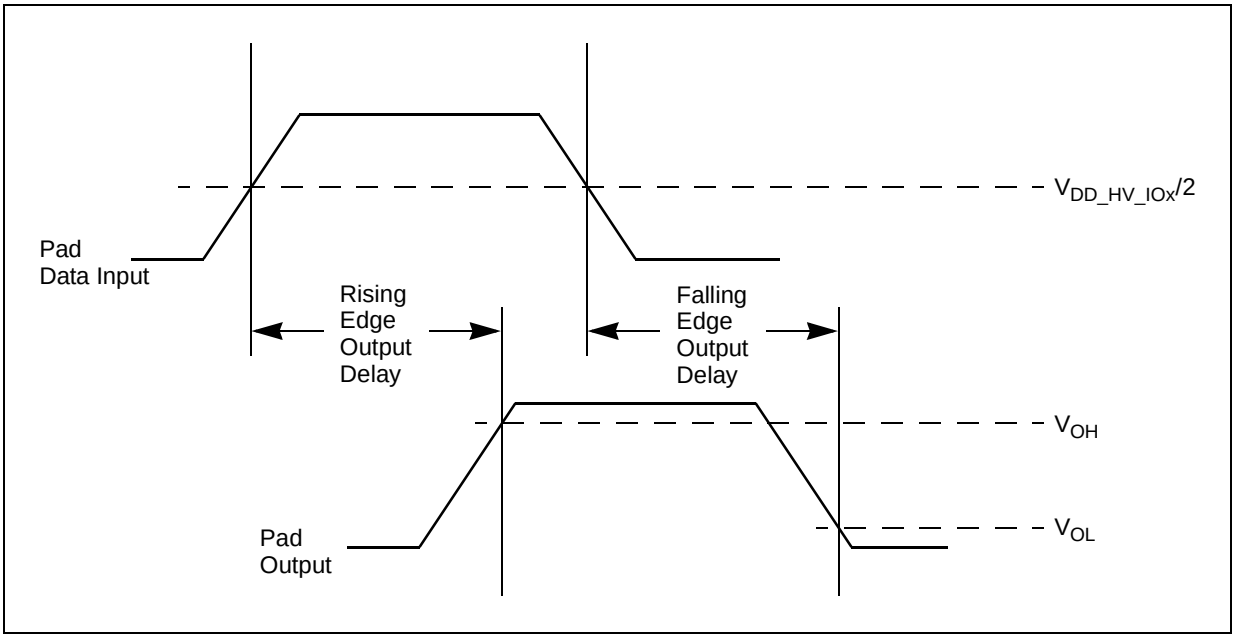
1. $V_{DD\_LV\_CORx}$ = 1.2 V ±10%; V_{SS} = 0 V; T_A = –40 to 125 °C, unless otherwise specified
2. Considering operation with PLL not bypassed.
3. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
4. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
5. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
6. This value is determined by the crystal manufacturer and board design.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DD\_LV\_COR0}$ and $V_{SS\_LV\_COR0}$ and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
8. Proper PC board layout procedures must be followed to achieve specifications.
9. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
10. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
12. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
13. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
14. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

Table 36. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	
t_{SYM}[3]	CC	T	Symmetric transition time, same drive strength between N and P transistor	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	4	ns
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified.
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).
3. Transition timing of both positive and negative slopes will differ maximum 50%.

Figure 19. Pad output delay



3.17 AC timing characteristics

3.17.1 $\overline{\text{RESET}}$ pin characteristics

The SPC560P34/SPC560P40 implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 20. Start-up reset requirements

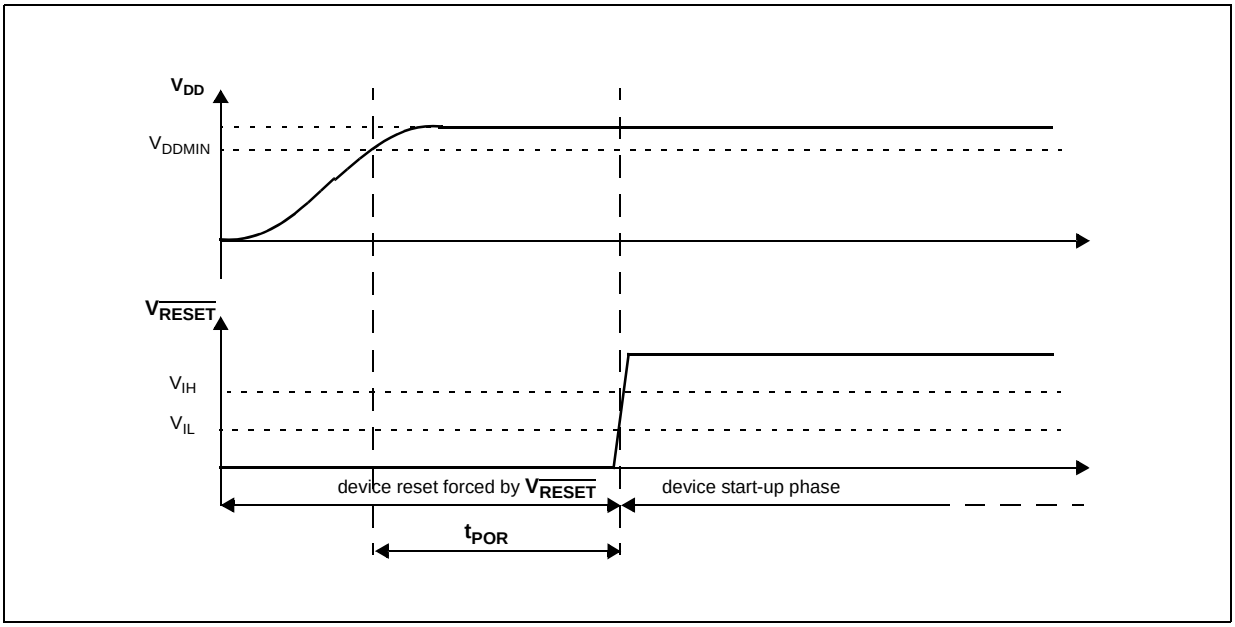


Figure 21. Noise filtering on reset signal

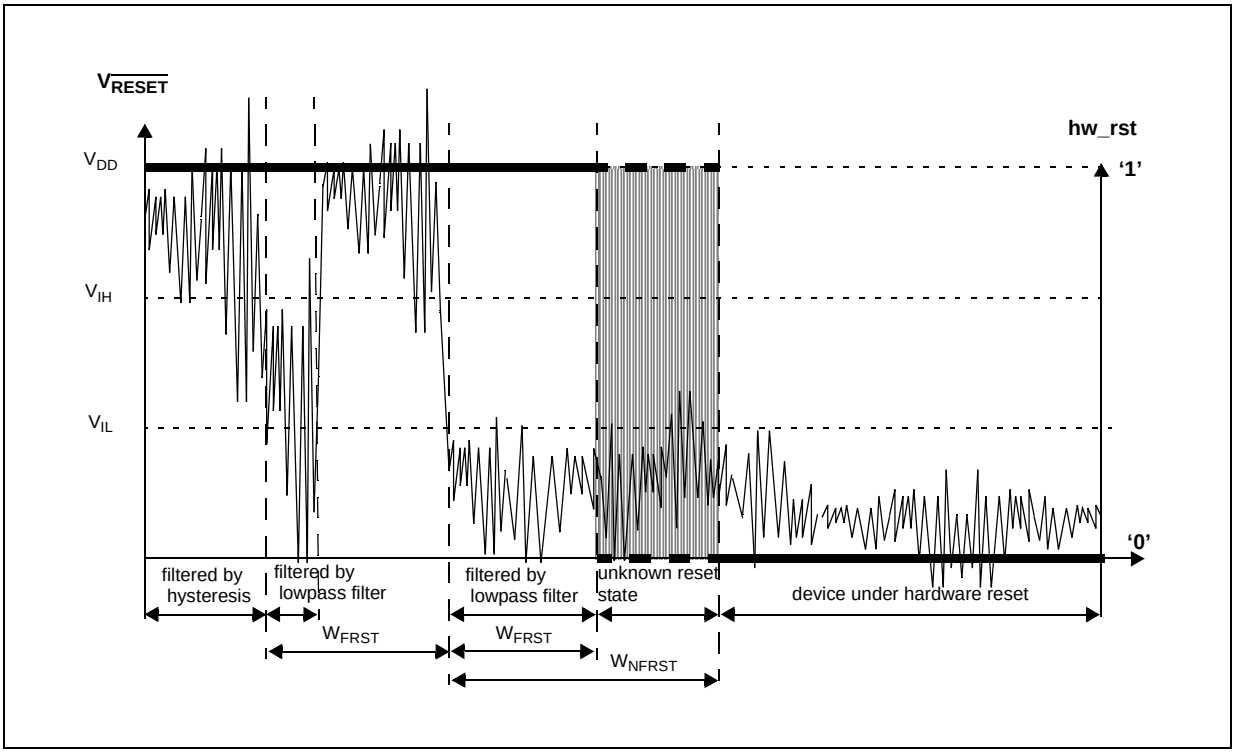
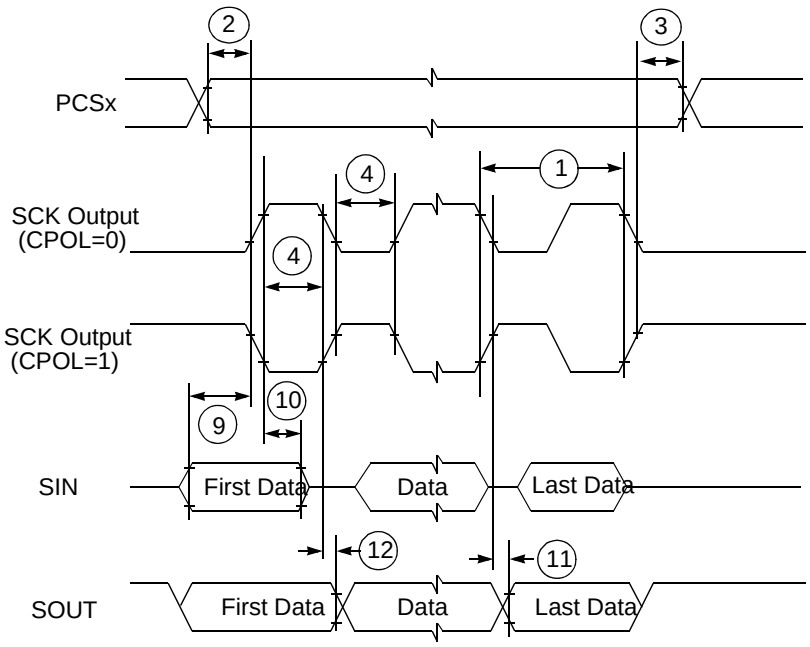


Table 41. DSPI timing(1) (continued)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

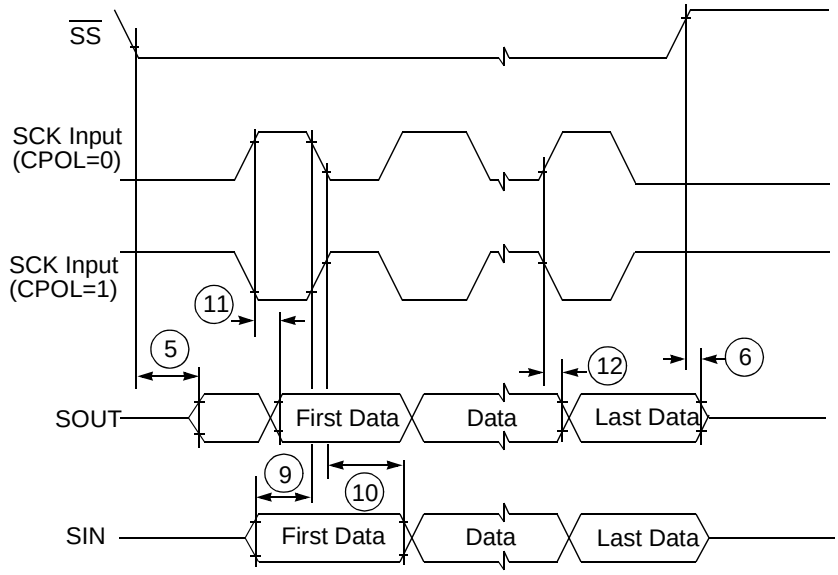
1. All timing are provided with 50 pF capacitance on output, 1 ns transition time on input signal

Figure 29. DSPI classic SPI timing – Master, CPHA = 0



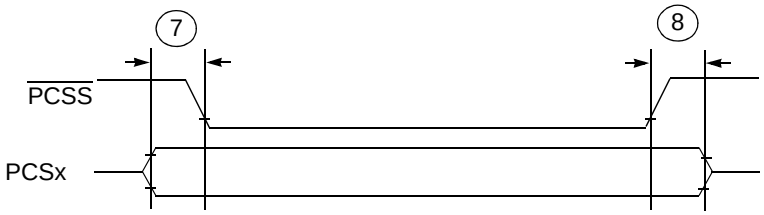
Note: Numbers shown reference *Table 41*.

Figure 36. DSPI modified transfer format timing – Slave, CPHA = 1



Note: Numbers shown reference *Table 41*.

Figure 37. DSPI PCS Strobe ($\overline{\text{PCSS}}$) timing



Note: Numbers shown reference *Table 41*.

Revision history

Table 45. Document revision history

Date	Revision	Changes
01-Sep-2009	1	Initial release.
21-May-2010	2	Editorial updates Updated the following items in the “SPC560P34/SPC560P40 device comparison” table: – The heading – The “SRAM” row – The “FlexCAN” row – The “CTU” row – The “FlexPWM” row – The “LINFlex” row – The “DSPI” row – The “Nexus” row Updated the “SPC560P34/SPC560P40 device configuration difference” table: – Editorial updates – Added the “CTU” row – Deleted the “temperature” row – Swapped the content of Airbag and Full Featured cells Added the “Wakeup unit” block in the SPC560P34/SPC560P40 block diagram Updated the “Absolute Maximum Ratings“ table Updated the “Recommended operating conditions (5.0 V)“ table Updated the “Recommended operating conditions (3.3 V)“ table Updated the “Thermal characteristics for 100-pin LQFP“ table: – Ψ_{JT}: changed the typical value Updated the “EMI testing specifications“ table: replaced all values in “Level (Max)“ column with TBD Updated the “Electrical characteristics“ section: – Added the “Introduction” section – Added the “Parameter classification“ section – Added the “NVUSRO register“ section – Added the “Power supplies constraints (–0.3 V ≤ $V_{DD\_HV\_IOx}$ ≤ 6.0 V)” figure – Added the “Independent ADC supply (–0.3 V ≤ $V_{DD\_HV\_REG}$ ≤ 6.0 V)“ figure – Added the “Power supplies constraints (3.0 V ≤ $V_{DD\_HV\_IOx}$ ≤ 5.5 V)“ figure – Added the “Independent ADC supply (3.0 V ≤ $V_{DD\_HV\_REG}$ ≤ 5.5 V)“ figure Updated the “Power management electrical characteristics” section Updated the “Power Up/Down sequencing” section Updated the “DC electrical characteristics“ section – Deleted the “NVUSRO register” section – Updated the “DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)“ section: – Deleted all rows concerning $\overline{\text{RESET}}$ – Deleted “I_{VPP}“ row – Added the max value for C_{IN}