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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p40l3befby

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2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures. For pin signal descriptions, please refer to *Table 7*.

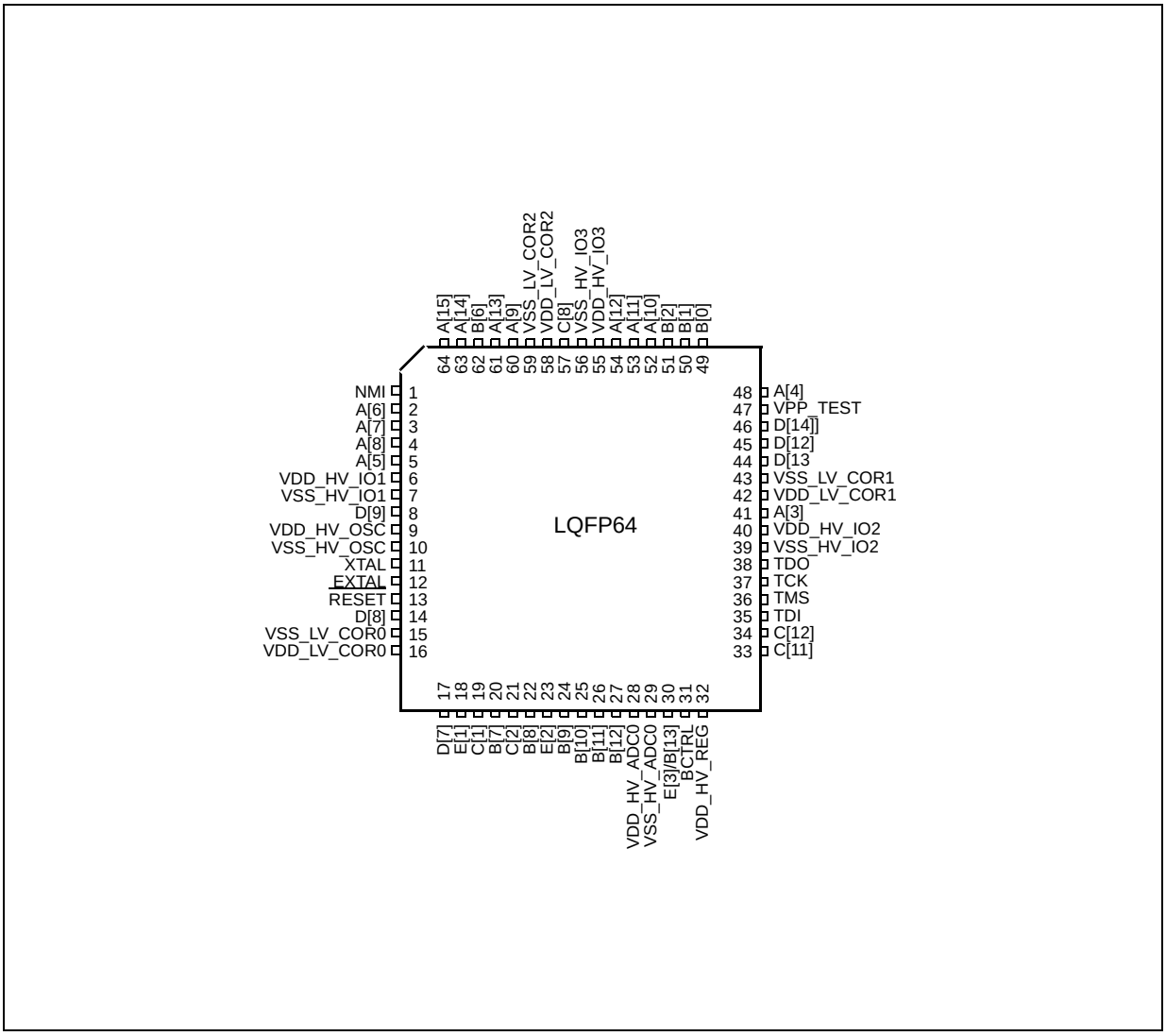


Figure 2. 64-pin LQFP pinout – Full featured configuration (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC560P34/SPC560P40 devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC560P34/SPC560P40 devices.

Table 5. Supply pins

Supply		Pin	
Symbol	**Description**	**64-pin**	**100-pin**
VREG control and power supply pins. Pins available on 64-pin and 100-pin packages			
BCTRL	Voltage regulator external NPN ballast base control pin	31	47
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	32	50
ADC_0 reference and supply voltage. Pins available on 64-pin and 100-pin packages			
$V_{DD\_HV\_ADC0}$(1)	ADC_0 supply and high reference voltage	28	39
$V_{SS\_HV\_ADC0}$	ADC_0 ground and low reference voltage	29	40
Power supply pins (3.3 V or 5.0 V). Pins available on 64-pin and 100-pin packages			
$V_{DD\_HV\_IO1}$	Input/output supply voltage	6	13
$V_{SS\_HV\_IO1}$	Input/output ground	7	14
$V_{DD\_HV\_IO2}$	Input/output supply voltage and data Flash memory supply voltage	40	63
$V_{SS\_HV\_IO2}$	Input/output ground and Flash memory HV ground	39	62
$V_{DD\_HV\_IO3}$	Input/output supply voltage and code Flash memory supply voltage	55	87
$V_{SS\_HV\_IO3}$	Input/output ground and code Flash memory HV ground	56	88
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	9	16
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	10	17
Power supply pins (1.2 V). Pins available on 64-pin and 100-pin packages			
$V_{DD\_LV\_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	16	25
$V_{SS\_LV\_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	15	24
$V_{DD\_LV\_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	42	65
$V_{SS\_LV\_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	43	66

2.2.3 Pin multiplexing

Table 7 defines the pin list and muxing for the SPC560P34/SPC560P40 devices.

Each row of *Table 7* shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

SPC560P34/SPC560P40 devices provide three main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see “Pad AC Specifications” in the device datasheet.

Table 7. Pin muxing

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O I/O O I	Slow	Medium	—	51
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	—	52
A[2]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O — O I I I	Slow	Medium	—	57
A[3]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	41	64

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK A[0] A[2] EIRQ[10]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O O I	Slow	Medium	53	82
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT A[2] B[2] EIRQ[11]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O O O O I	Slow	Medium	54	83
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[13] — B[2] — SIN FAULT[0] EIRQ[12]	SIUL — FlexPWM_0 — DSPI_2 FlexPWM_0 SIUL	I/O — O — I I I	Slow	Medium	61	95
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD — — EIRQ[13]	SIUL Safety Port_0 — — SIUL	I/O O — — I	Slow	Medium	63	99
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — — — RXD EIRQ[14]	SIUL — — — Safety Port_0 SIUL	I/O — — — I I	Slow	Medium	64	100
Port B (16-bit)									
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD — DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	49	76
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] — — DEBUG[1] RXD EIRQ[16]	SIUL — — SSCM FlexCAN_0 SIUL	I/O — — — I I	Slow	Medium	50	77

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3	GPIO[41] CS3 — X[3]	SIUL DSPI_2 — FlexPWM_0	I/O O — O	Slow	Medium	—	84
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3 —	GPIO[42] CS2 — A[3] FAULT[1]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — O I	Slow	Medium	—	78
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[4] CS2 —	SIUL eTimer_0 DSPI_2 —	I/O I/O O —	Slow	Medium	33	55
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	GPIO[44] ETC[5] CS3 —	SIUL eTimer_0 DSPI_2 —	I/O I/O O —	Slow	Medium	34	56
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[45] — — — EXT_IN EXT_SYNC	SIUL — — — CTU_0 FlexPWM_0	I/O — — — I I	Slow	Medium	—	71
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3	GPIO[46] — EXT_TGR —	SIUL — CTU_0 —	I/O — O —	Slow	Medium	—	72
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[47] — — A[1] EXT_IN EXT_SYNC	SIUL — — FlexPWM_0 CTU_0 FlexPWM_0	I/O — — O I I	Slow	Medium	—	85
Port D (16-bit)									
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] — — B[1]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	86

Table 10. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
$V_{DD\_HV\_ADC0}$	SR	5.0 V ADC_0 supply and high reference voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG}$ – 0.1	—	
$V_{SS\_HV\_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(3),(4)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(3),(4)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 60 MHz	–40	125	°C
			f_{CPU} = 64 MHz	–40	105	°C

1. Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 100$ mV.
3. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
4. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.
   – $V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.
   – $V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_RECORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Table 11. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V

3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 23*.

Table 23. I/O supply segment

Package	Supply segment				
	1	2	3	4	5
LQFP100	pin15–pin26	pin27–pin46	pin51–pin61	pin64–pin86	pin89–pin10
LQFP64	pin8–pin17	pin18–pin30	pin33–pin38	pin41–pin54	pin57–pin5

Table 24. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	

3.13 16 MHz RC oscillator electrical characteristics

Table 29. 16 MHz RC oscillator electrical characteristics

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–5	—	5	%

3.14 Analog-to-digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) analog-to-digital converter.

Figure 15. ADC characteristics and error definitions

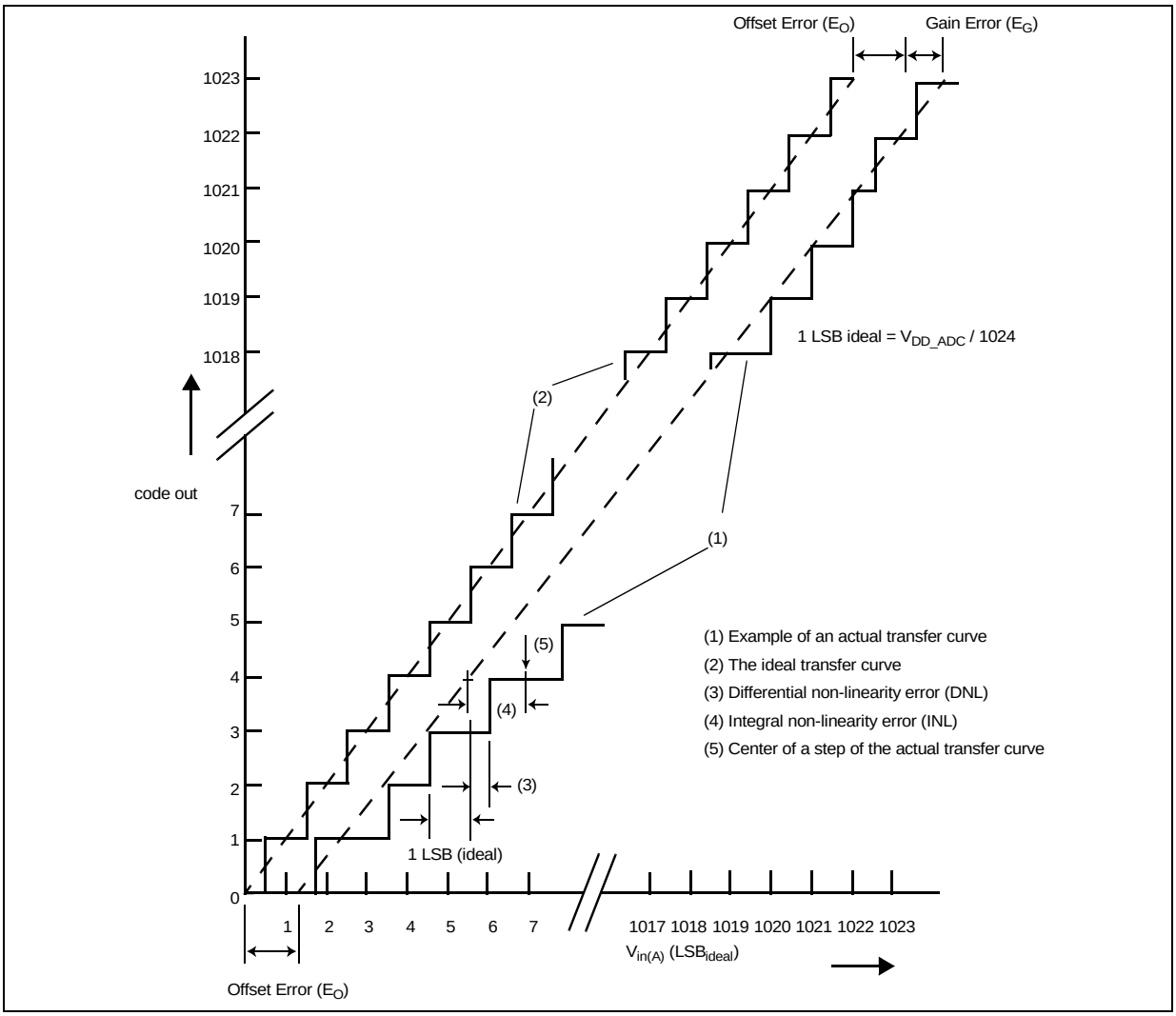
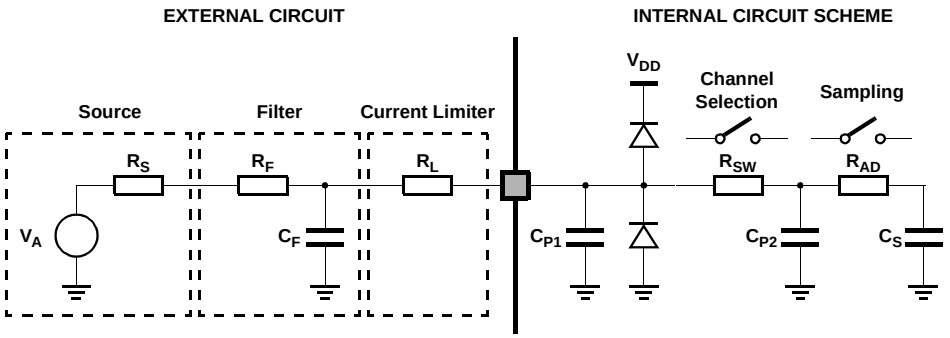


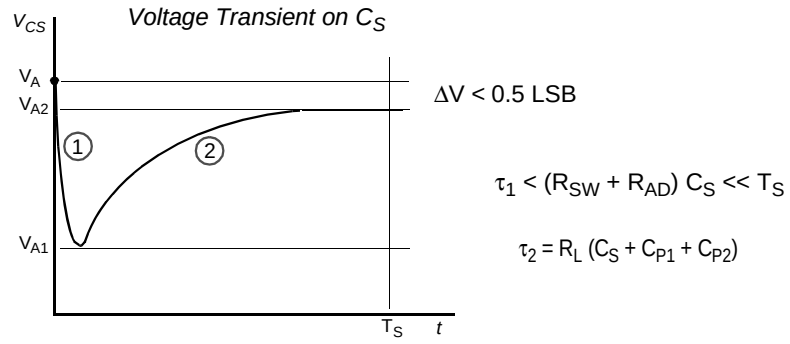
Figure 16. Input equivalent circuit



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW}: Channel selection switch impedance
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1} and C_{P2})
C_S: Sampling capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch closed).

Figure 17. Transient behavior during sampling phase



In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Equation 9

$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

Figure 25. Nexus output timing

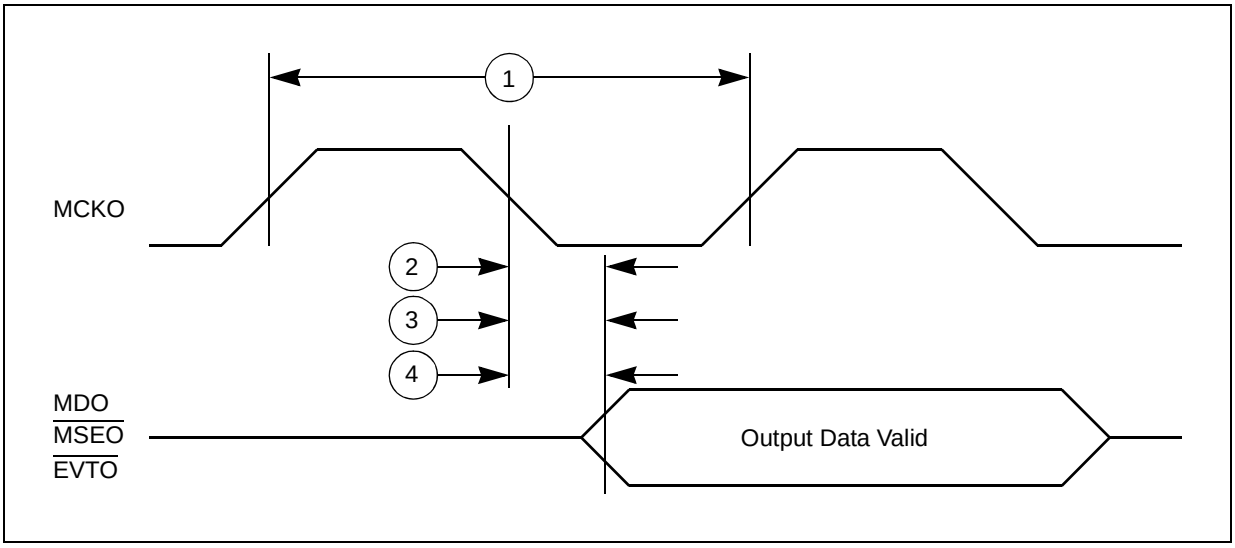


Figure 26. Nexus event trigger and test clock timing

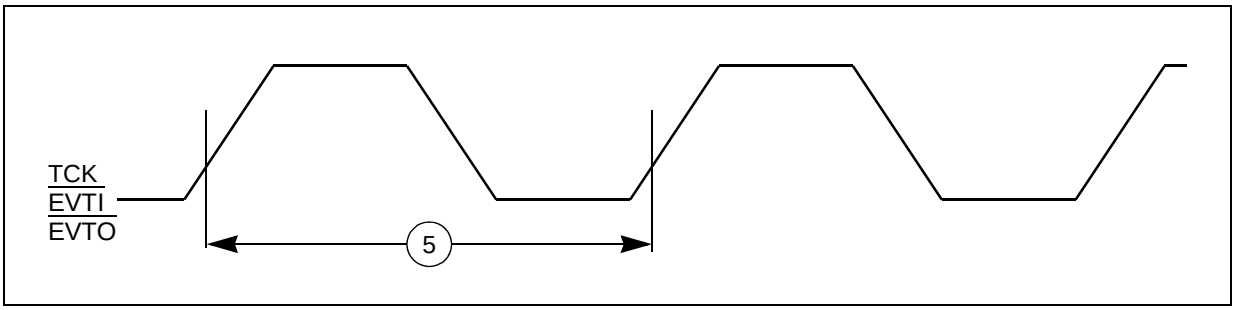
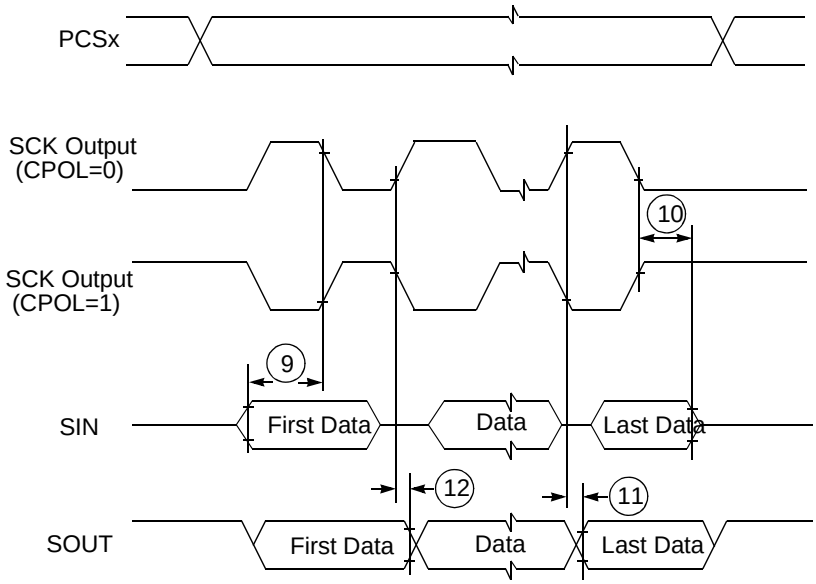
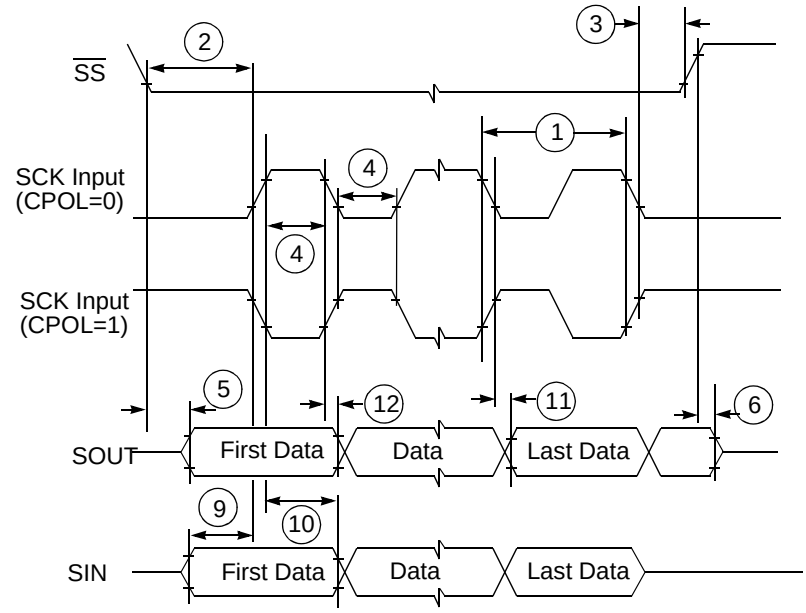


Figure 30. DSPI classic SPI timing – Master, CPHA = 1



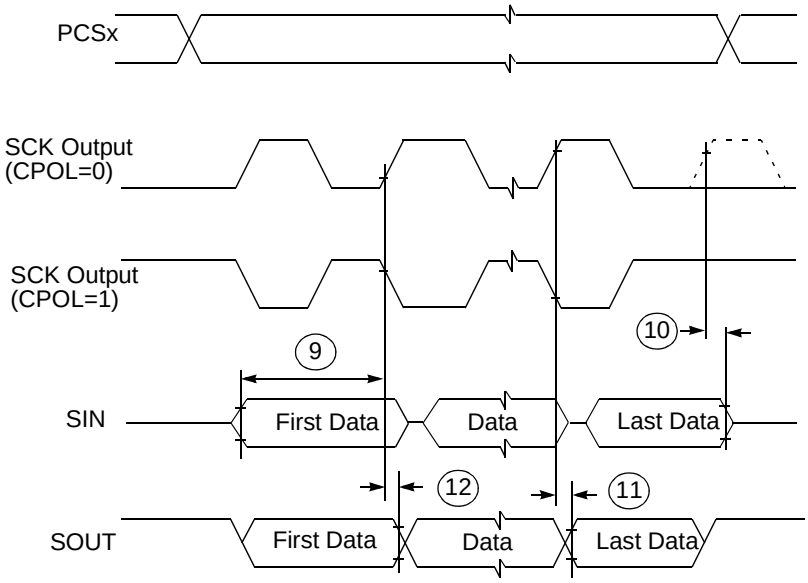
Note: Numbers shown reference *Table 41*.

Figure 31. DSPI classic SPI timing – Slave, CPHA = 0



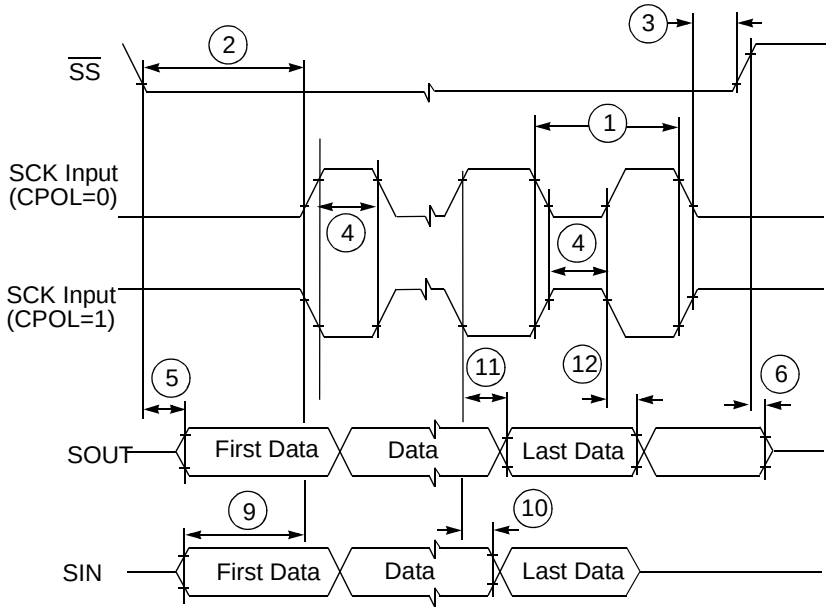
Note: Numbers shown reference *Table 41*.

Figure 34. DSPI modified transfer format timing – Master, CPHA = 1



Note: Numbers shown reference *Table 41*.

Figure 35. DSPI modified transfer format timing – Slave, CPHA = 0



Note: Numbers shown reference *Table 41*.

4.2.2 LQFP64 mechanical outline drawing

Figure 39. LQFP64 package mechanical drawing

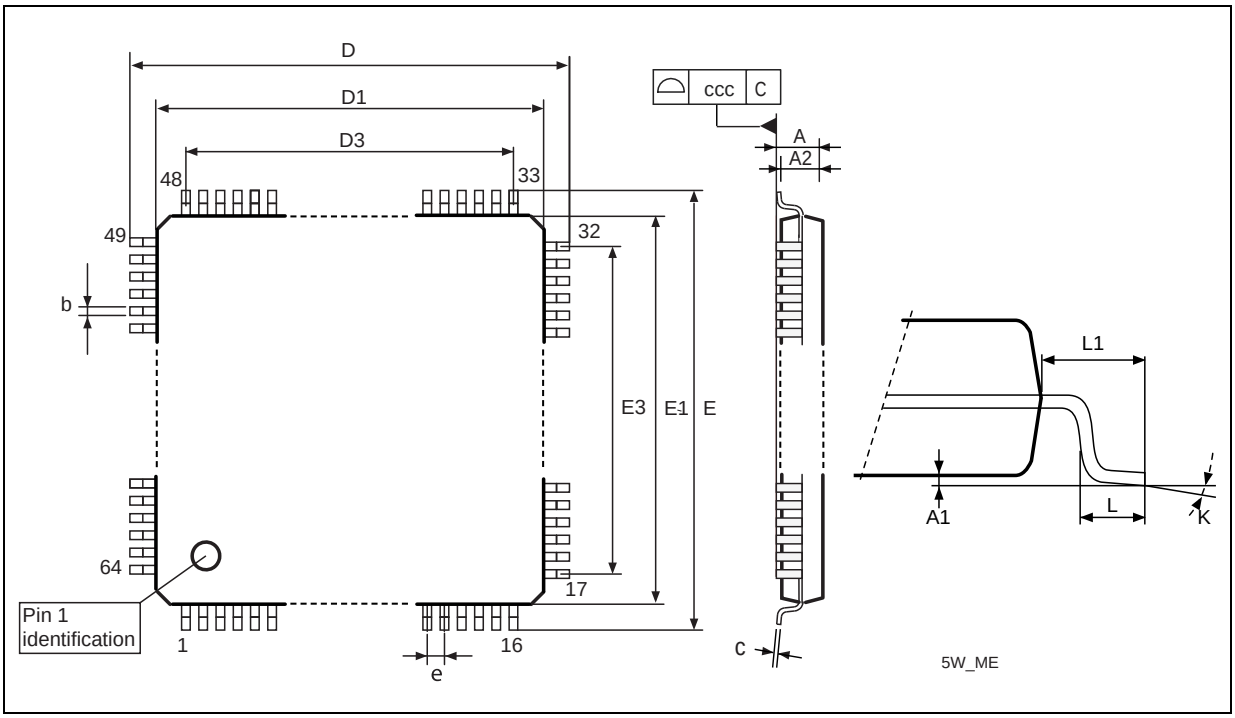


Table 43. LQFP64 package mechanical data

Symbol	Dimensions					
	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.6	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.0059
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	—	0.2	0.0035	—	0.0079
D	11.8	12	12.2	0.4646	0.4724	0.4803
D1	9.8	10	10.2	0.3858	0.3937	0.4016
D3	—	7.5	—	—	0.2953	—
E	11.8	12	12.2	0.4646	0.4724	0.4803
E1	9.8	10	10.2	0.3858	0.3937	0.4016
E3	—	7.5	—	—	0.2953	—
e	—	0.5	—	—	0.0197	—
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1	—	1	—	—	0.0394	—

Table 43. LQFP64 package mechanical data (continued)

Symbol	Dimensions					
	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc[2]	0.08			0.0031		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. Tolerance

Appendix A Abbreviations

Table 44 lists abbreviations used in this document.

Table 44. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
DUT	Device under test
ECC	Error code correction
EVTO	Event out
GPIO	General purpose input / output
MC	Modulus counter
MCKO	Message clock out
MCU	Microcontroller unit
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
NPN	Negative-positive-negative
NVUSRO	Non-volatile user options register
PTF	Post trimming frequency
PWM	Pulse width modulation
RISC	Reduced instruction set computer
SCK	Serial communications clock
SOUT	Serial data out
TBC	To be confirmed
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Table 45. Document revision history (continued)

Date	Revision	Changes
23-Dec-2010	3 (continued)	Updated “Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)” table Updated “Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)” table “Input clock characteristics” table: updated f_{CLK} max value “PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)” table: – Updated supply voltage range for V_{DDPLL} in the table title – Updated f_{SCM} max value – Updated C_{JITTER} row – Updated f_{MOD} max value Updated “16 MHz RC oscillator electrical characteristics” table Updated “ADC conversion characteristics” table “Program and erase specifications” table: – $T_{wprogram}$: updated initial max and max values – T_{BKPRG}, 64 KB: updated initial max and max values – added information about “erase time” for Data Flash “Flash module life” table: – P/E, 32 KB: added typ value – P/E, 128 KB: added typ value Replaced “Pad AC specifications (5.0 V, NVUSRO[PAD3V5V] = 0)” and “Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)” tables with “Output pin transition times” table “JTAG pin AC electrical characteristics” table: – t_{TDOV}: updated max value – t_{TDOHZ}: added min value and removed max value “Nexus debug port timing” table: removed the rows “t_{MCYC}”, “t_{MDOV}”, “t_{MSEOV}”, and “t_{EVTOV}” Updated “External interrupt timing (IRQ pin)” table Updated “FlexCAN timing” table Updated “DSPI timing” table Updated “Ordering information” section

Table 45. Document revision history (continued)

Date	Revision	Changes
13-May-2011	4	Editorial and formatting changes throughout Cover page features list: • changed core feature “64 MHz” to “Up to 64 MHz” • changed Data flash memory “64 (4 × 16) KB” to “Additional 64 (4 × 16) KB” • changed “1 FlexCAN interface” to “Up to 2 FlexCAN interface” Updated Device summary Section “Introduction“: Reorganized contents SPC560P40 device configuration differences: Editorial changes to indicate that the table concerns only the SPC560P40 devices); removed “DSPI” row Block diagram (SPC560P40 full-featured configuration): reorganized blocks above and below peripheral bridge; made arrow going from peripheral bridge to crossbar switch bidirectional; removed SPC560P34 part number from title Added section “Features details” 64-pin and 100-pin LQFP pinout diagrams: replaced instances of HV_AD0 with HV_ADC0 System pins: updated “XTAL” and “EXTAL” rows Updated LQFP thermal characteristics Updated EMI testing specifications section “Voltage regulator electrical characteristics“: removed BCP56 from named BJTs; replaced two configuration diagrams and two electrical characteristics tables with single diagram and single table Voltage regulator electrical characteristics: updated $V_{DD\_LV\_REGCOR}$ row Low voltage monitor electrical characteristics: updated $V_{MLVDDOK\_H}$ max value—was 1.15 V; is 1.145 V Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): changed symbol $I_{DD\_LV\_CORE}$ to $I_{DD\_LV\_CORx}$; changed parameter classification from T to P for $I_{DD\_LV\_CORx}$ RUN—Maximum mode at 64 MHz; added I_{DD_FLASH} characteristics; replaced instances of “Airbag” mode with “Typical mode” Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): changed symbol $I_{DD\_LV\_CORE}$ to $I_{DD\_LV\_CORx}$; replaced instances of “Airbag” mode with “Typical mode” DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): corrected parameter description for V_{OL_F}—was “Fast, high level output voltage”; is “Fast, low level output voltage” Added *Section 3.10.4, Input DC electrical characteristics definition* Main oscillator output electrical characteristics tables: replaced instances of EXTAL with XTAL; added load capacitance parameter FMPLL electrical characteristics: updated conditions and table title; removed f_{sys} row; updated $f_{FMPLLOUT}$ values; replaced instances of V_{DDPLL} with $V_{DD\_LV\_COR0}$; replaced instances of V_{SSPLL} with $V_{SS\_LV\_COR0}$ 16 MHz RC oscillator electrical characteristics: removed rows $\Delta_{RCMTRIM}$ and $\Delta_{RCMSTEP}$ ADC characteristics and error definitions: updated symbols ADC conversion characteristics: updated symbols; added row t_{ADC_PU} Added *Section 3.15.2, Flash memory power supply DC characteristics* Added *Section 3.15.3, Start-up/Switch-off timings* Removed section “Generic timing diagrams” Updated Start-up reset requirements diagram Removed FlexCAN timing characteristics RESET electrical characteristics: added row for t_{POR} In the range of figures “DSPI Classic SPI Timing — Master, CPHA = 0” to “DSPI PCS Strobe (PCSS) Timing”: added note Updated Order codes