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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p40l3cefbr

Table 3. SPC560P40 device configuration differences

Feature	Configuration	
	Airbag	Full-featured
SRAM (with ECC)	16 KB	20 KB
FlexCAN (controller area network)	1	2
Safety port	No	Yes (via second FlexCAN module)
FlexPWM (pulse-width modulation) channels	No	8 (capture capability not supported)
CTU (cross triggering unit)	No	Yes

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC560P34/SPC560P40 MCU. *Table 2* summarizes the functions of the blocks.

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC560P34/SPC560P40:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module running at the same frequency as the e200z0h core
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency: 4–40 MHz
- Maximum output frequency: 64 MHz
- Voltage controlled oscillator (VCO)—frequency 256–512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the FMPLL to relock
- Frequency-modulated PLL
  - Modulation enabled/disabled through software
  - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency): programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.10 Main oscillator

The main oscillator provides these features:

- Input frequency range: 4–40 MHz
- Crystal input mode or oscillator input mode
- PLL reference

1.5.11 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

- 4 general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel usable as trigger for a DMA request

1.5.13 System timer module (STM)

The STM implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, a safety relay)
- Faults are latched into a register

1.5.22 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the SPC560P34/SPC560P40 features the following:

- Supports LIN Master mode (both instances), LIN Slave mode (only one instance) and UART mode
- LIN state machine compliant to LIN1.3, 2.0 and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to 8 data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features:
  - Autonomous LIN header handling
  - Autonomous LIN response handling
  - Optional discarding of irrelevant LIN responses using ID filter
- UART mode:
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

1.5.25 eTimer

The SPC560P34/SPC560P40 includes one eTimer module which provides six 16-bit general purpose up/down timer/counter units with the following features:

- Clock frequency same as that used for the e200z0h core
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (quad decoder mode)
- Maximum count rate
  - External event counting: max. count rate = peripheral clock/2
  - Internal clock counting: max. count rate = peripheral clock
- Counters are:
  - Cascadable
  - Preloadable
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Pins available as GPIO when timer functionality not in use

1.5.26 Analog-to-digital converter (ADC) module

The ADC module provides the following features:

Analog part:

- 1 on-chip analog-to-digital converter
  - 10-bit AD resolution
  - 1 sample and hold unit
  - Conversion time, including sampling time, less than 1 µs (at full precision)
  - Typical sampling time is 150 ns minimum (at full precision)
  - DNL/INL ±1 LSB
  - TUE < 1.5 LSB
  - Single-ended input signal up to 3.3 V/5.0 V
  - 3.3 V/5.0 V input reference voltage
  - ADC and its reference can be supplied with a voltage independent from V_{DDIO}
  - ADC supply can be equal or higher than V_{DDIO}
  - ADC supply and ADC reference are not independent from each other (both internally bonded to same pad)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK A[0] A[2] EIRQ[10]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O O I	Slow	Medium	53	82
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT A[2] B[2] EIRQ[11]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O O O O I	Slow	Medium	54	83
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[13] — B[2] — SIN FAULT[0] EIRQ[12]	SIUL — FlexPWM_0 — DSPI_2 FlexPWM_0 SIUL	I/O — O — I I I	Slow	Medium	61	95
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD — — EIRQ[13]	SIUL Safety Port_0 — — SIUL	I/O O — — I	Slow	Medium	63	99
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — — — RXD EIRQ[14]	SIUL — — — Safety Port_0 SIUL	I/O — — — I I	Slow	Medium	64	100
Port B (16-bit)									
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD — DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	49	76
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] — — DEBUG[1] RXD EIRQ[16]	SIUL — — SSCM FlexCAN_0 SIUL	I/O — — — I I	Slow	Medium	50	77

Table 7. Pin muxing (continued)

Port pin	PCR register	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	44
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input only	—	—	—	43
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input only	—	—	—	45
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input only	—	—	—	41

1. ALT0 is the primary (default) function for each port after reset.
2. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 → ALT0; PCR.PA = 01 → ALT1; PCR.PA = 10 → ALT2; PCR.PA = 11 → ALT3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
3. Module included on the MCU.
4. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
5. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
6. ADC0.AN emulates ADC1.AN. This feature is used to provide software compatibility between SPC560P34/SPC560P40 and SPC560P50. Refer to ADC chapter of reference manual for more details.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max[2]	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$[3]	SR	3.3 V/5.0 V input/output supply voltage (supply). Code flash memory supply with $V_{DD\_HV\_IO3}$ and data flash memory with $V_{DD\_HV\_IO2}$	—	–0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	3.3 V/5.0 V input/output supply voltage (ground). Code flash memory ground with $V_{SS\_HV\_IO3}$ and data flash memory with $V_{SS\_HV\_IO2}$	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V/5.0 V crystal oscillator amplifier supply voltage (supply)	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_OSC}$	SR	3.3 V/5.0 V crystal oscillator amplifier supply voltage (ground)	—	–0.1	0.1	V
$V_{DD\_HV\_ADC0}$	SR	3.3 V/5.0 V ADC_0 supply and high-reference voltage	$V_{DD\_HV\_REG}$ < 2.7 V	–0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	–0.3	6.0	
$V_{SS\_HV\_ADC0}$	SR	3.3 V/5.0 V ADC_0 ground and low-reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V/5.0 V voltage-regulator supply voltage	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up[4] with respect to ground (V_{SS})	—	3.0[5]	500 x 10^3 (0.5 [V/µs])	V/s
$V_{DD\_LV\_CORx}$	CC	1.2 V supply pins for core logic (supply)	—	–0.1	1.5	V
$V_{SS\_LV\_CORx}$	SR	1.2 V supply pins for core logic (ground)	—	–0.1	0.1	V
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$)	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3[6]	
I_{INJPAD}	SR	Input current on any pin during overload condition	—	–10	10	mA

3.8.2 Voltage monitor electrical characteristics

The device implements a power on reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors low voltage digital power domain

Table 17. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25 °C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5 V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5 V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC560P34/SPC560P40 implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5 V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash

memory and 16 MHz RC oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated modules are set into a safe state.

Figure 11. Power-up typical sequence

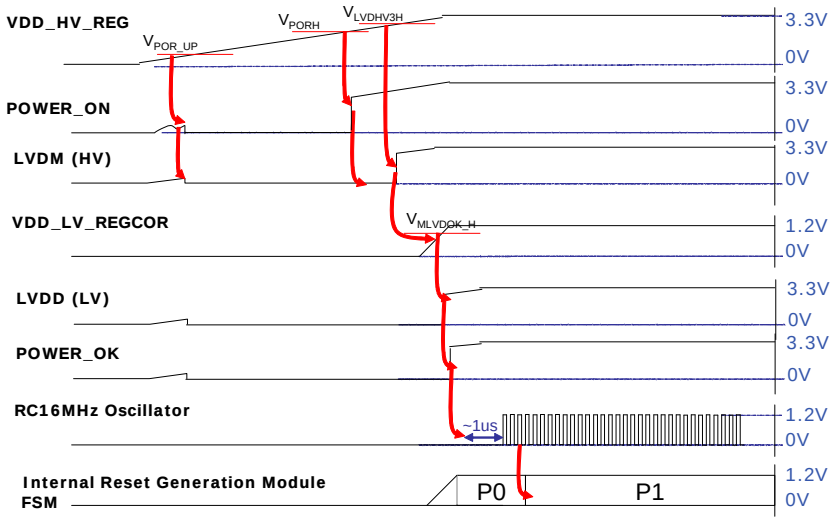


Figure 12. Power-down typical sequence

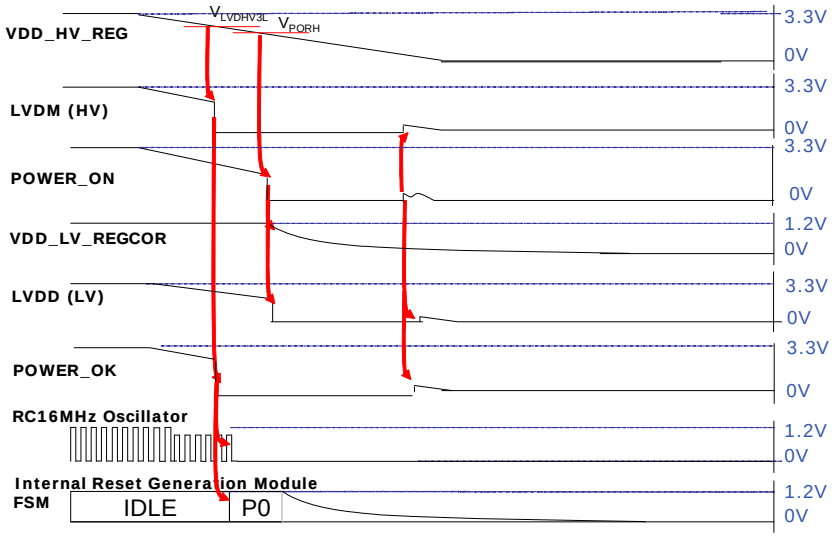


Table 26. Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{OSC}	SR	—	Oscillator frequency		4	40	MHz
g_m	—	P	Transconductance		4	20	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin		1	—	V
t_{OSCSU}	—	T	Start-up time(1),(2)		8	—	ms
C_L	CC	T	XTAL load capacitance(3)	4 MHz	5	30	pf
		T		8 MHz	5	26	
		T		12 MHz	5	23	
		T		16 MHz	5	19	
		T		20 MHz	5	16	
		T		40 MHz	5	8	

1. The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL
3. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

Table 27. Input clock characteristics

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	64	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.12 FMPLL electrical characteristics

Table 28. FMPLL electrical characteristics

Symbol	C	Parameter	Conditions(1)	Value		Unit
				Min	Max	
$f_{ref\_crystal}$ f_{ref_ext}	D	PLL reference frequency range(2)	Crystal reference	4	40	MHz
f_{PLLIN}	D	Phase detector input frequency range (after pre-divider)	—	4	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	16	64	MHz

Table 28. FMPLL electrical characteristics (continued)

Symbol	C	Parameter		Conditions[1]	Value		Unit
					Min	Max	
f_{FREE}	P	Free-running frequency		Measured using clock division—typically /16	20	150	MHz
t_{CYC}	D	System clock period		—	—	1 / f_{SYS}	ns
f_{LORL}	D	Loss of reference frequency window[3]		Lower limit	1.6	3.7	MHz
f_{LORH}	D			Upper limit	24	56	
f_{SCM}	D	Self-clocked mode frequency[4],[5]		—	20	150	MHz
C_{JITTER}	T	CLKOUT period jitter[6],[7],[8],[9]	Short-term jitter[10]	f_{SYS} maximum	–4	4	% f_{CLKOUT}
			Long-term jitter (average over 2 ms interval)	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 64 MHz, 4000 cycles	—	10	ns
t_{lpll}	D	PLL lock time[11], [12]		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	–6	6	% f_{SYS}
f_{UL}	D	Frequency un-LOCK range		—	–18	18	% f_{SYS}
f_{CS}	D	Modulation depth		Center spread	±0.25	±4.0 (13)	% f_{SYS}
f_{DS}	D			Down spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency[14]		—	—	70	kHz

1. $V_{DD\_LV\_CORx}$ = 1.2 V ±10%; V_{SS} = 0 V; T_A = –40 to 125 °C, unless otherwise specified
2. Considering operation with PLL not bypassed.
3. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
4. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
5. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
6. This value is determined by the crystal manufacturer and board design.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DD\_LV\_COR0}$ and $V_{SS\_LV\_COR0}$ and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
8. Proper PC board layout procedures must be followed to achieve specifications.
9. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
10. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
12. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
13. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
14. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

Figure 23. JTAG test access port timing

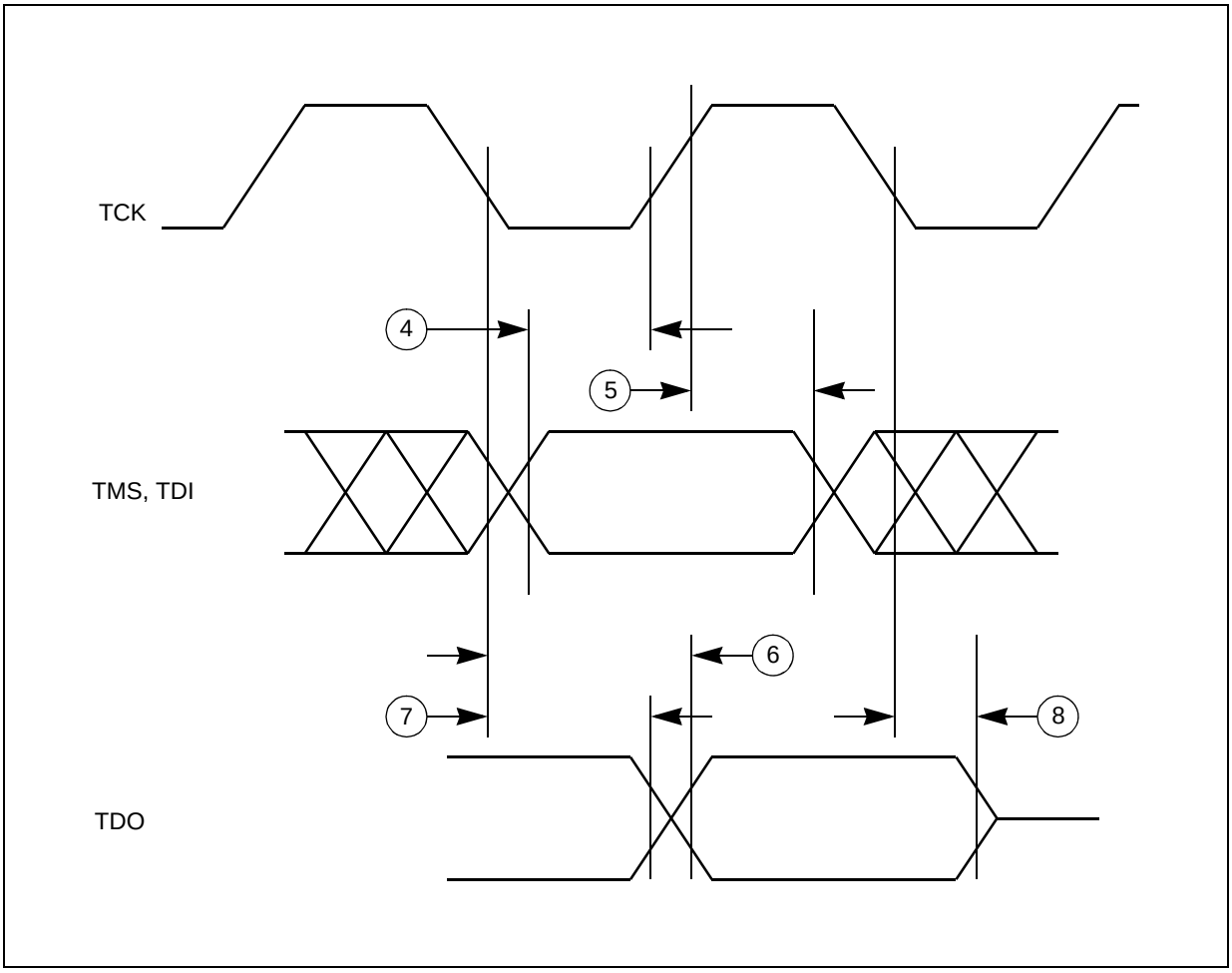
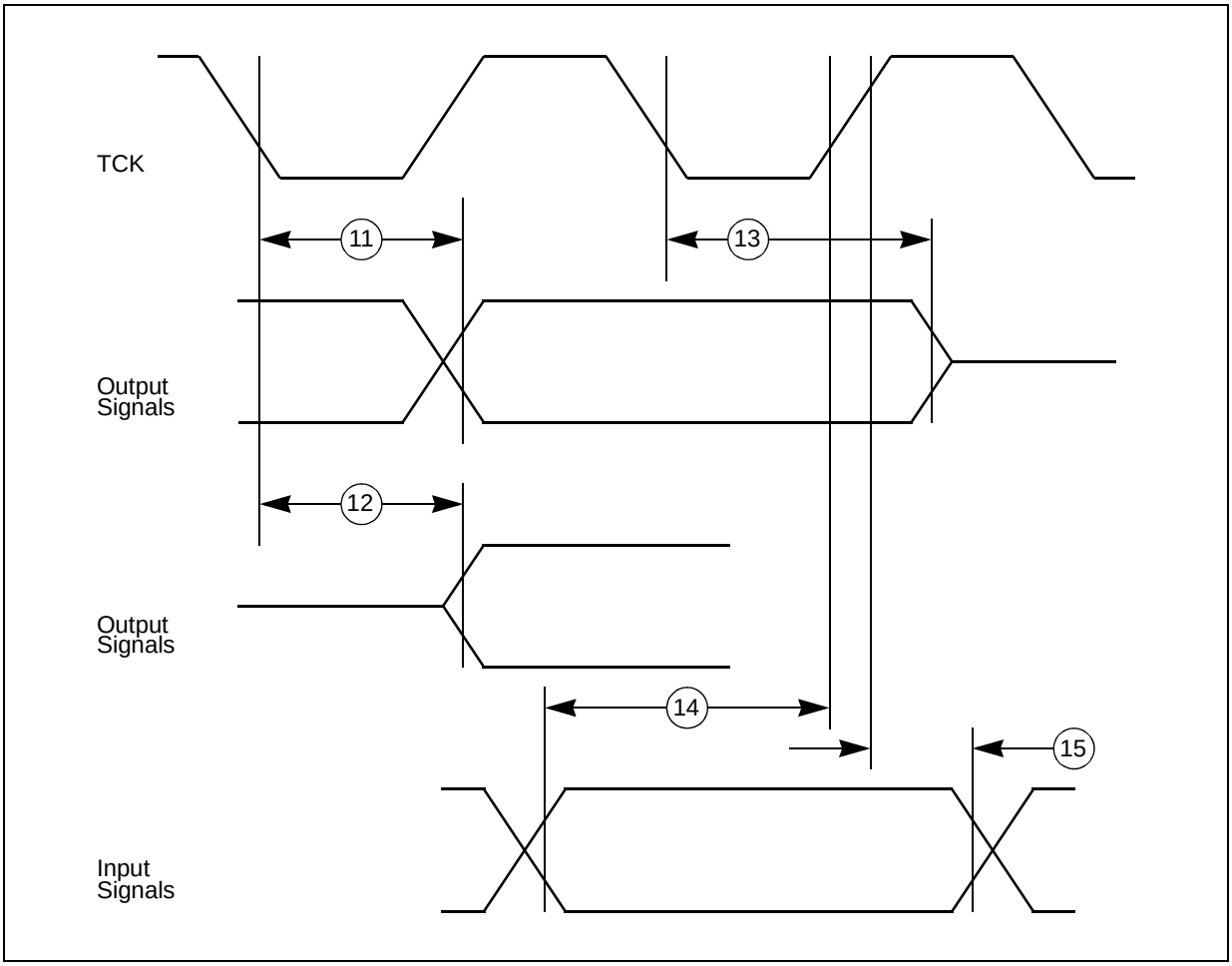


Figure 24. JTAG boundary scan timing



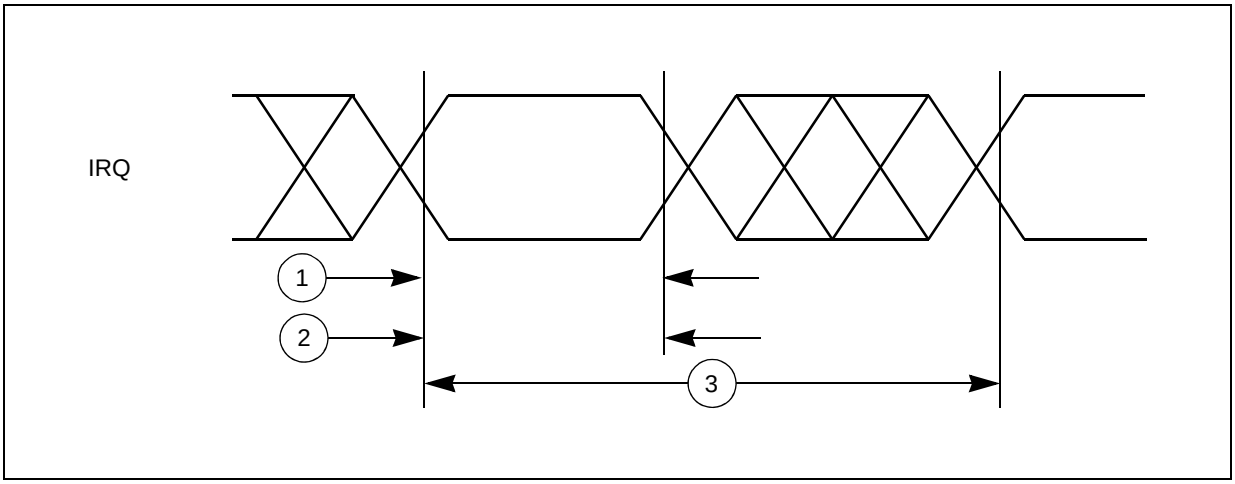
3.17.3 Nexus timing

Table 39. Nexus debug port timing(1)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	4(2)	—	—	t_{CYC}
2	t_{NTDIS}	CC	D	TDI data setup time	5	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	5	—	—	ns
3	t_{NTDIH}	CC	D	TDI data hold time	25	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	25	—	—	ns
4	t_{TDOV}	CC	D	TCK low to TDO data valid	10	—	20	ns
5	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	—	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. Lower frequency is required to be fully compliant to standard.

Figure 28. External interrupt timing



3.17.5 DSPI timing

Table 41. DSPI timing(1)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	60	—	ns
					Slave (MTFE = 0)	60	—	
2	t_{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	26	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	30	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT high impedance or invalid	—	16	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	35	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	35	—	
					Master (MTFE = 1, CPHA = 1)	35	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	–5	—	

Table 42. LQFP100 package mechanical data

Symbol	Dimensions					
	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc[2]	0.08			0.0031		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. Tolerance

5 Ordering information

Figure 40. Commercial product code structure

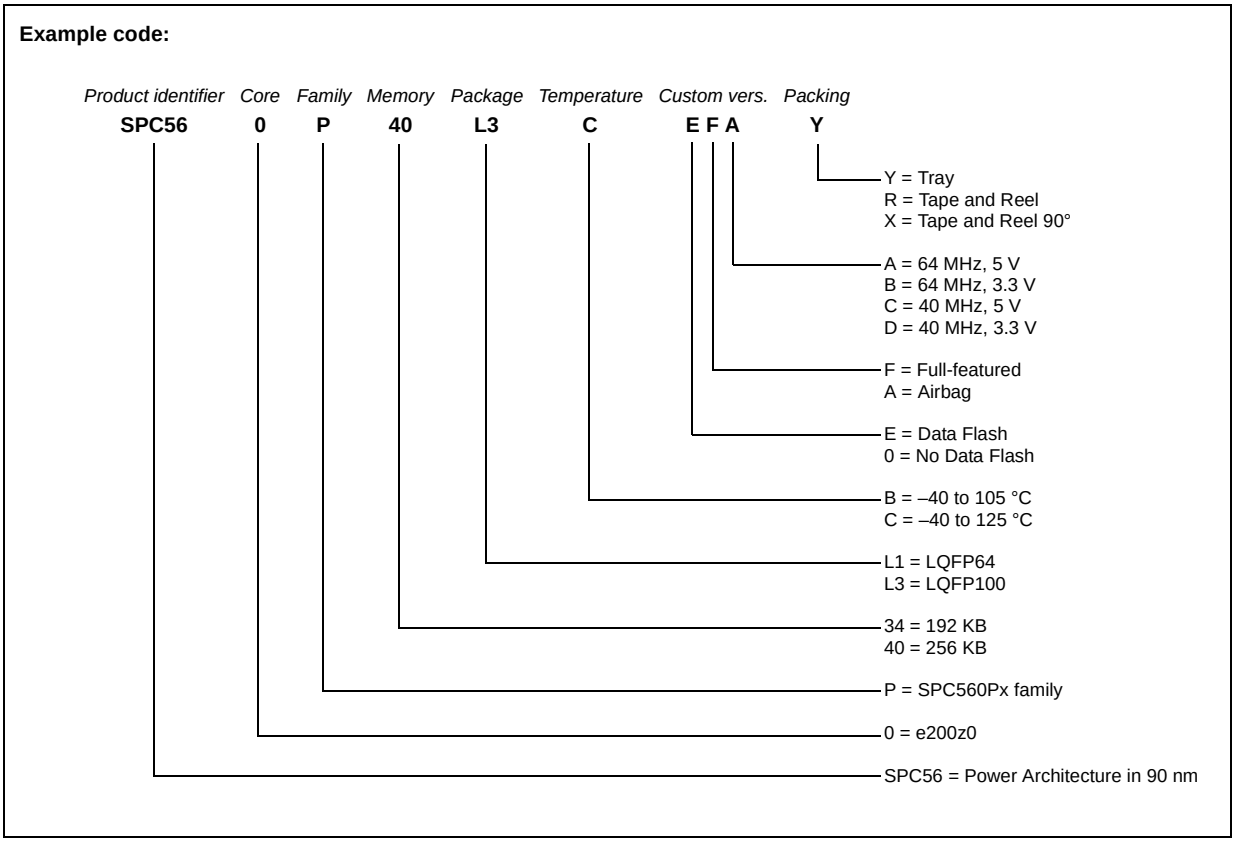


Table 45. Document revision history (continued)

Date	Revision	Changes
13-May-2011	4	Editorial and formatting changes throughout Cover page features list: • changed core feature “64 MHz” to “Up to 64 MHz” • changed Data flash memory “64 (4 × 16) KB” to “Additional 64 (4 × 16) KB” • changed “1 FlexCAN interface” to “Up to 2 FlexCAN interface” Updated Device summary Section “Introduction“: Reorganized contents SPC560P40 device configuration differences: Editorial changes to indicate that the table concerns only the SPC560P40 devices); removed “DSPI” row Block diagram (SPC560P40 full-featured configuration): reorganized blocks above and below peripheral bridge; made arrow going from peripheral bridge to crossbar switch bidirectional; removed SPC560P34 part number from title Added section “Features details” 64-pin and 100-pin LQFP pinout diagrams: replaced instances of HV_AD0 with HV_ADC0 System pins: updated “XTAL” and “EXTAL” rows Updated LQFP thermal characteristics Updated EMI testing specifications section “Voltage regulator electrical characteristics“: removed BCP56 from named BJTs; replaced two configuration diagrams and two electrical characteristics tables with single diagram and single table Voltage regulator electrical characteristics: updated $V_{DD\_LV\_REGCOR}$ row Low voltage monitor electrical characteristics: updated $V_{MLVDDOK\_H}$ max value—was 1.15 V; is 1.145 V Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): changed symbol $I_{DD\_LV\_CORE}$ to $I_{DD\_LV\_CORx}$; changed parameter classification from T to P for $I_{DD\_LV\_CORx}$ RUN—Maximum mode at 64 MHz; added I_{DD_FLASH} characteristics; replaced instances of “Airbag” mode with “Typical mode” Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): changed symbol $I_{DD\_LV\_CORE}$ to $I_{DD\_LV\_CORx}$; replaced instances of “Airbag” mode with “Typical mode” DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): corrected parameter description for V_{OL_F}—was “Fast, high level output voltage”; is “Fast, low level output voltage” Added *Section 3.10.4, Input DC electrical characteristics definition* Main oscillator output electrical characteristics tables: replaced instances of EXTAL with XTAL; added load capacitance parameter FMPLL electrical characteristics: updated conditions and table title; removed f_{sys} row; updated $f_{FMPLLOUT}$ values; replaced instances of V_{DDPLL} with $V_{DD\_LV\_COR0}$; replaced instances of V_{SSPLL} with $V_{SS\_LV\_COR0}$ 16 MHz RC oscillator electrical characteristics: removed rows $\Delta_{RCMTRIM}$ and $\Delta_{RCMSTEP}$ ADC characteristics and error definitions: updated symbols ADC conversion characteristics: updated symbols; added row t_{ADC_PU} Added *Section 3.15.2, Flash memory power supply DC characteristics* Added *Section 3.15.3, Start-up/Switch-off timings* Removed section “Generic timing diagrams” Updated Start-up reset requirements diagram Removed FlexCAN timing characteristics RESET electrical characteristics: added row for t_{POR} In the range of figures “DSPI Classic SPI Timing — Master, CPHA = 0” to “DSPI PCS Strobe (PCSS) Timing”: added note Updated Order codes