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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	8
Number of Gates	-
Number of I/O	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LCC (J-Lead)
Supplier Device Package	20-PLCC (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/gal16v8d-10lji">https://www.e-xfl.com/product-detail/lattice-semiconductor/gal16v8d-10lji</a>

## Features

- **HIGH PERFORMANCE E<sup>2</sup>CMOS® TECHNOLOGY**
  - 3.5 ns Maximum Propagation Delay
  - $F_{max} = 250$  MHz
  - 3.0 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - 75mA Typ  $I_{cc}$  on Low Power Device
  - 45mA Typ  $I_{cc}$  on Quarter Power Device
- **ACTIVE PULL-UPS ON ALL PINS**
- **E<sup>2</sup> CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **LEAD-FREE PACKAGE OPTIONS**

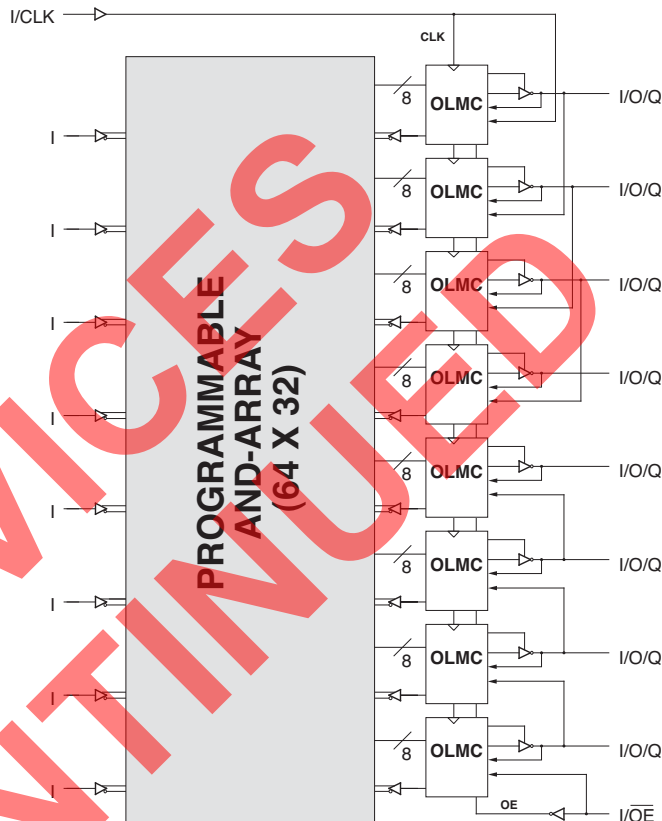
## Description

The GAL16V8, at 3.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E<sup>2</sup>) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

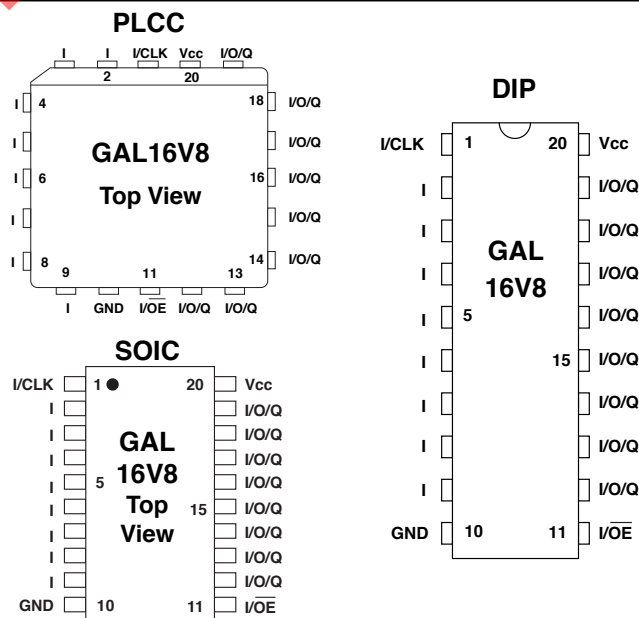
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 are the PAL architectures listed in the table of the macrocell description section. GAL16V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

## Functional Block Diagram



## Pin Configuration



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August 2006

## Lead-Free Packaging

### Commercial Grade Specifications

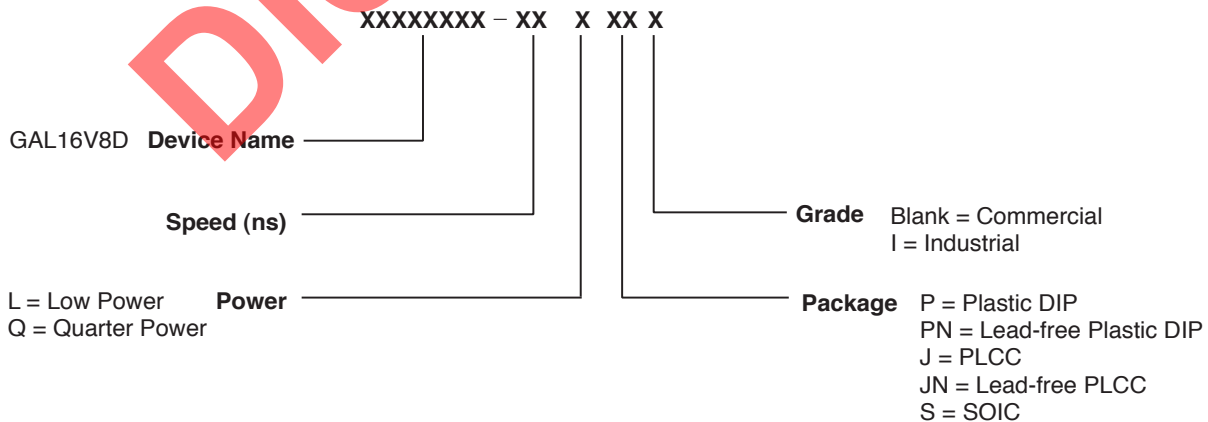
Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
3.5	2.5	3.0	115	GAL16V8D-3LJN <sup>1</sup>	Lead-Free 20-Lead PLCC
5	3	4	115	GAL16V8D-5LJN	Lead-Free 20-Lead PLCC
7.5	7	5	115	GAL16V8D-7LPN	Lead-Free 20-Pin Plastic DIP
			115	GAL16V8D-7LJN	Lead-Free 20-Lead PLCC
10	10	7	55	GAL16V8D-10QPN	Lead-Free 20-Pin Plastic DIP
			55	GAL16V8D-10QJN	Lead-Free 20-Lead PLCC
			115	GAL16V8D-10LPN	Lead-Free 20-Pin Plastic DIP
			115	GAL16V8D-10LJN	Lead-Free 20-Lead PLCC
15	12	10	55	GAL16V8D-15QPN	Lead-Free 20-Pin Plastic DIP
			55	GAL16V8D-15QJN	Lead-Free 20-Lead PLCC
			90	GAL16V8D-15LPN	Lead-Free 20-Pin Plastic DIP
			90	GAL16V8D-15LJN	Lead-Free 20-Lead PLCC
25	15	12	55	GAL16V8D-25QPN	Lead-Free 20-Pin Plastic DIP
			55	GAL16V8D-25QJN	Lead-Free 20-Lead PLCC
			90	GAL16V8D-25LPN	Lead-Free 20-Pin Plastic DIP
			90	GAL16V8D-25LJN	Lead-Free 20-Lead PLCC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

### Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	130	GAL16V8D-7LJN <sup>1</sup>	Lead-Free 20-Lead PLCC
			130	GAL16V8D-7LPNI	Lead-Free 20-Pin Plastic DIP
10	10	7	130	GAL16V8D-10LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-10LPNI	Lead-Free 20-Pin Plastic DIP
15	12	10	130	GAL16V8D-15LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-15LPNI	Lead-Free 20-Pin Plastic DIP
20	13	11	65	GAL16V8D-20QJNI	Lead-Free 20-Lead PLCC
			65	GAL16V8D-20QPNI	Lead-Free 20-Pin Plastic DIP
25	15	12	65	GAL16V8D-25QJNI	Lead-Free 20-Lead PLCC
			65	GAL16V8D-25QPNI	Lead-Free 20-Pin Plastic DIP
			130	GAL16V8D-25LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-25LPNI	Lead-Free 20-Pin Plastic DIP

### Part Number Description



## Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8 can emulate. It also shows the OLMC mode under which the GAL16V8 emulates the PAL architecture.

PAL Architectures Emulated by GAL16V8	GAL16V8 Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

## Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1 and pin 11 are permanently configured

as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins ( pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/IC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered" <sup>1</sup>	"Complex" <sup>1</sup>	"Simple" <sup>1</sup>	GAL16V8A
PLDesigner	P16V8R <sup>2</sup>	P16V8C <sup>2</sup>	P16V8C <sup>2</sup>	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS <sup>3</sup>	G16V8

1) Used with **Configuration** keyword.

2) Prior to Version 2.0 support.

3) Supported on Version 1.20 or later.

## Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

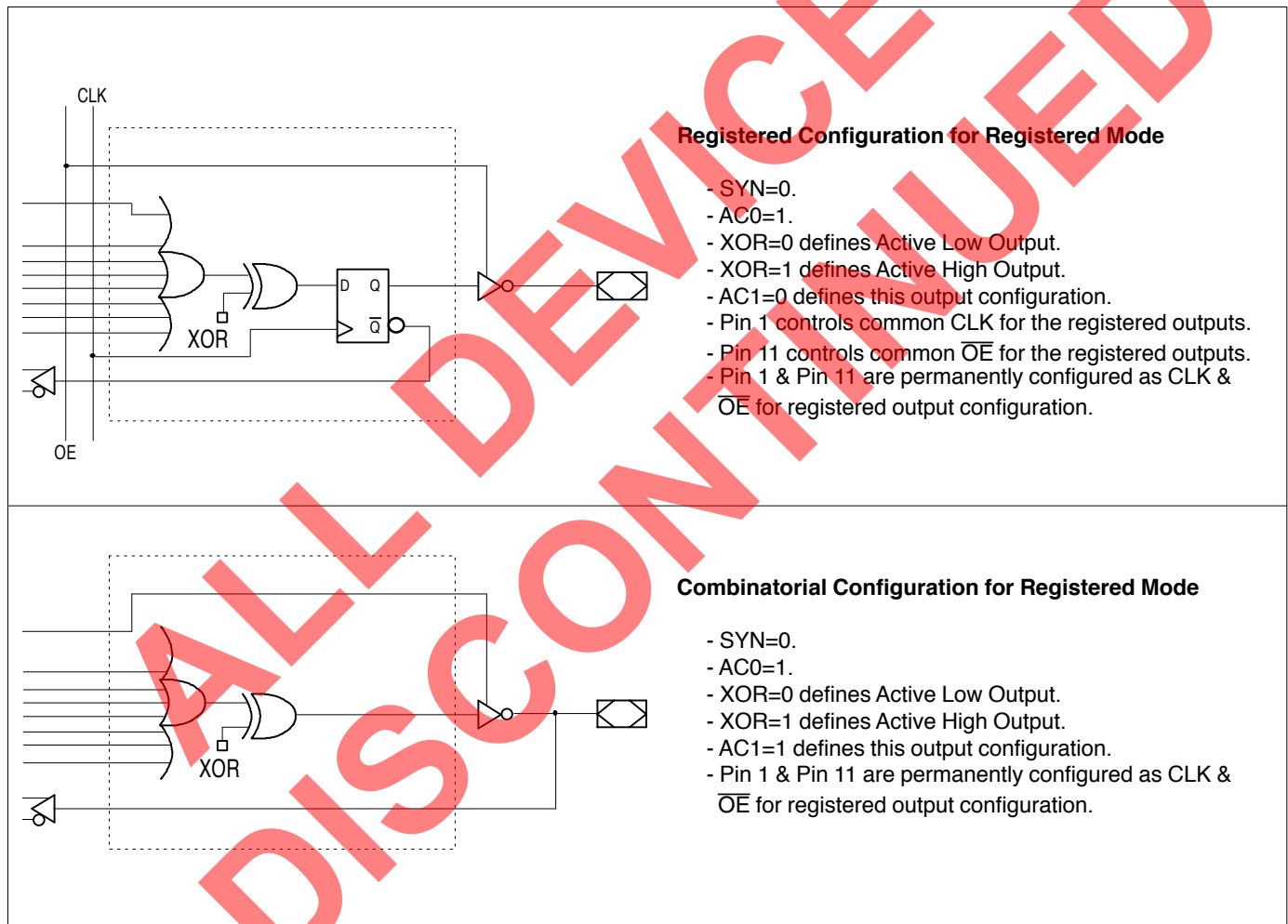
Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode.

Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/O's have seven product terms per output.

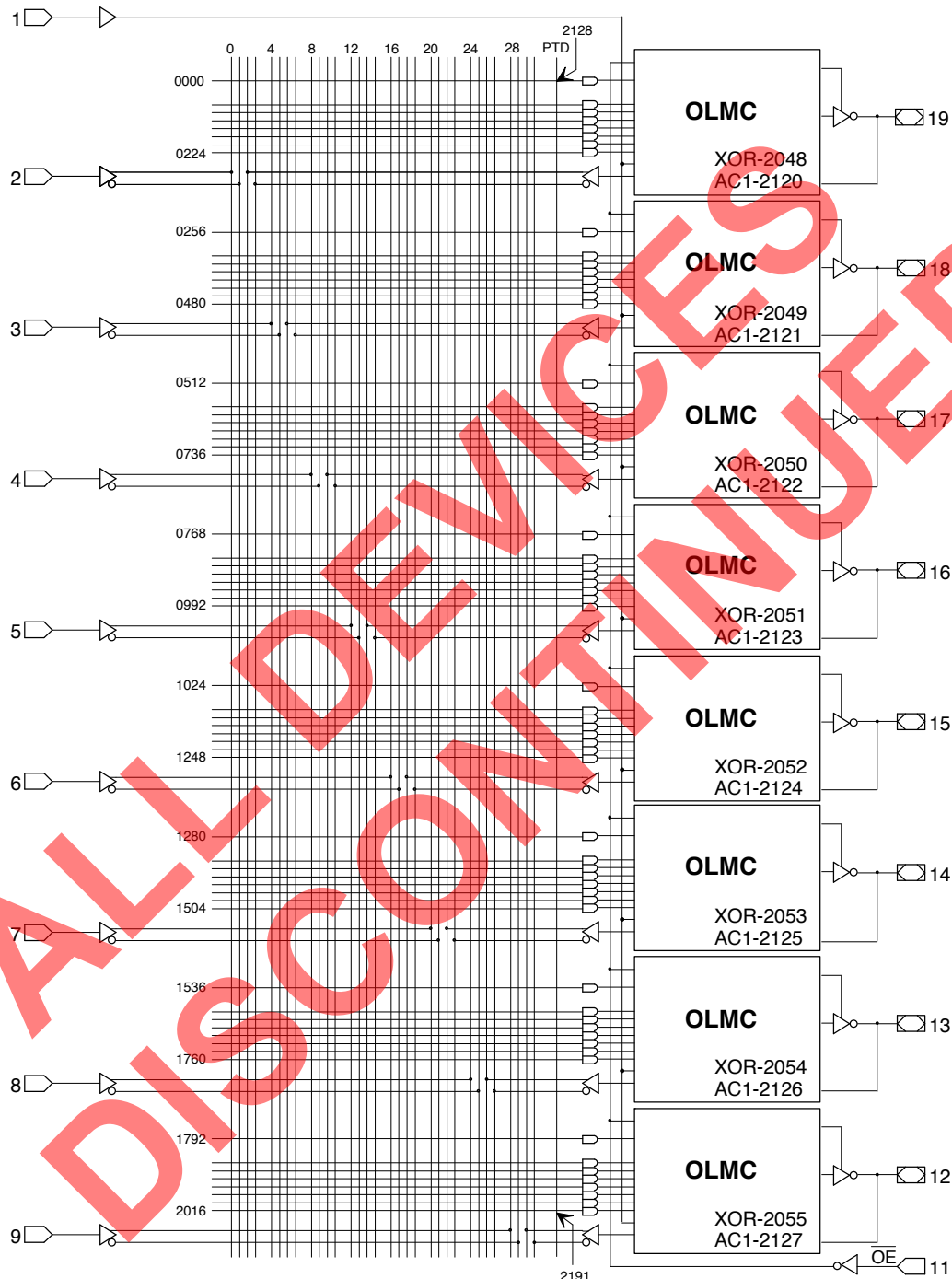
The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

**Registered Mode Logic Diagram**

**DIP & PLCC Package Pinouts**



**64-USER ELECTRONIC SIGNATURE FUSES**

2056, 2057, ....	.... 2118, 2119
Byte 7   Byte 6   ....	.... Byte 1   Byte 0

M L  
S S  
B B

SYN-2192  
AC0-2193

## Complex Mode

In the Complex mode, macrocells are configured as output only or I/O functions.

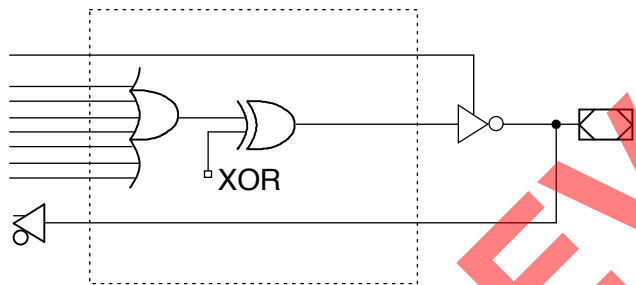
Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capa-

bility. Designs requiring eight I/O's can be implemented in the Registered mode.

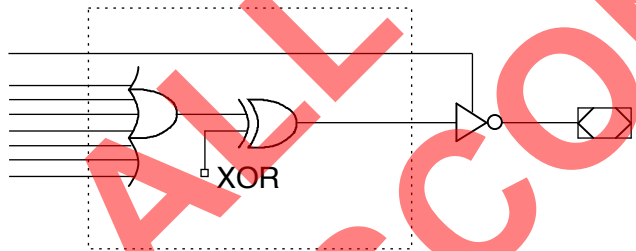
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



**Combinatorial I/O Configuration for Complex Mode**

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 13 through Pin 18 are configured to this function.



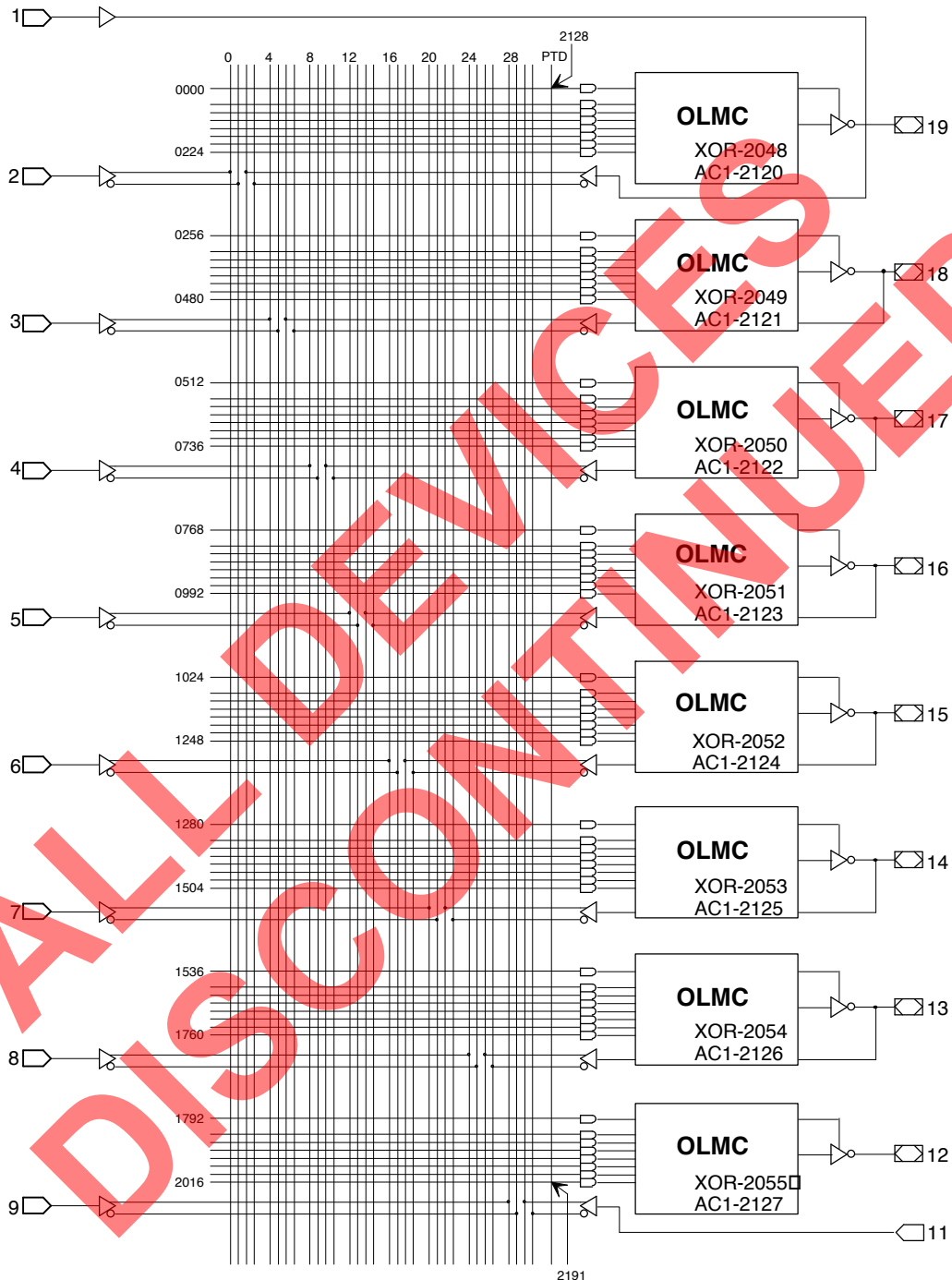
**Combinatorial Output Configuration for Complex Mode**

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

**Complex Mode Logic Diagram**

**DIP & PLCC Package Pinouts**



**64-USER ELECTRONIC SIGNATURE FUSES**

2056, 2057, ....	.... 2118, 2119
Byte 7   Byte 6   ....	.... Byte 1   Byte 0
M	L
S	S
B	B

SYN-2192  
AC0-2193



## Simple Mode

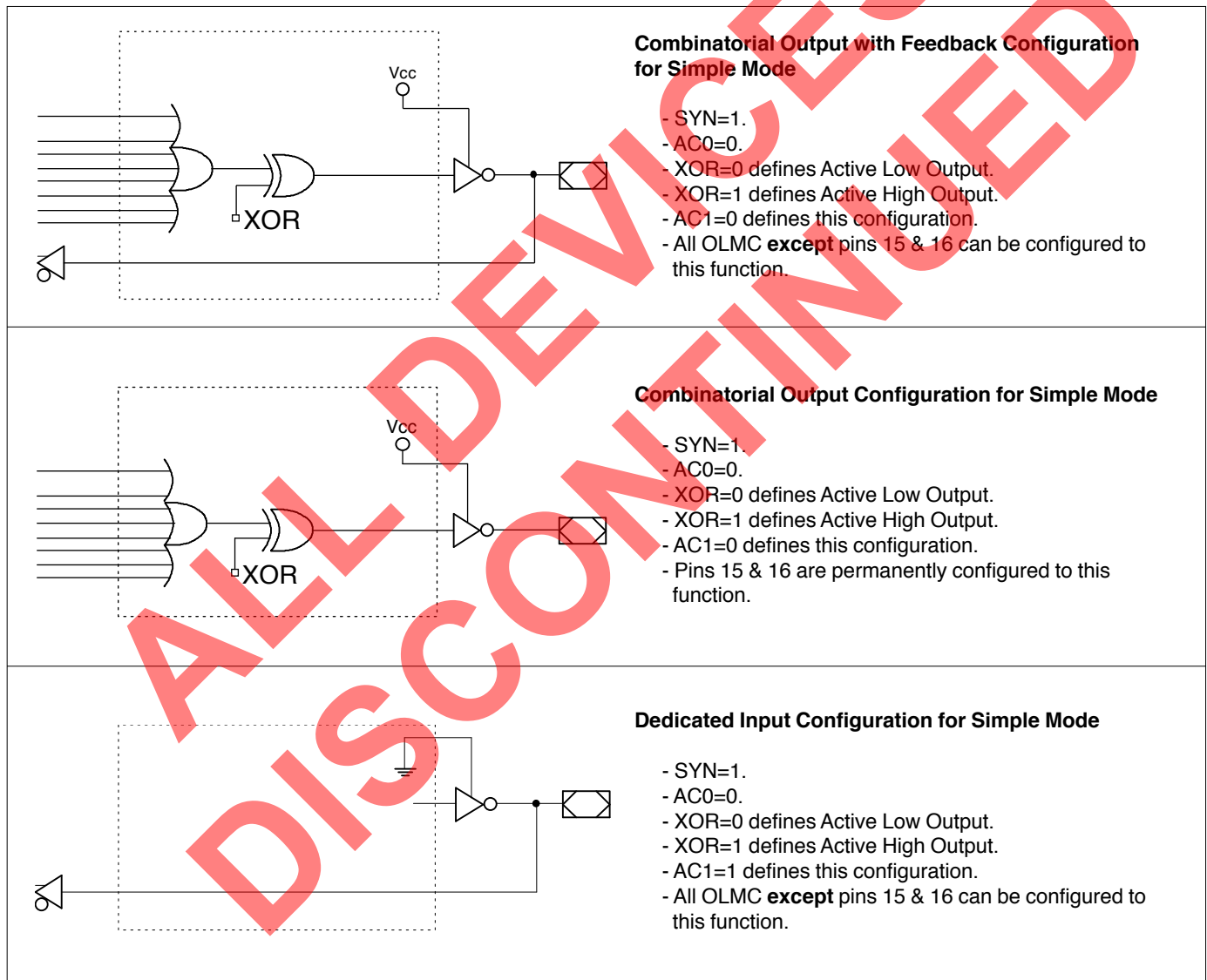
In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used as input or I/O pins, and are only available as dedicated outputs.

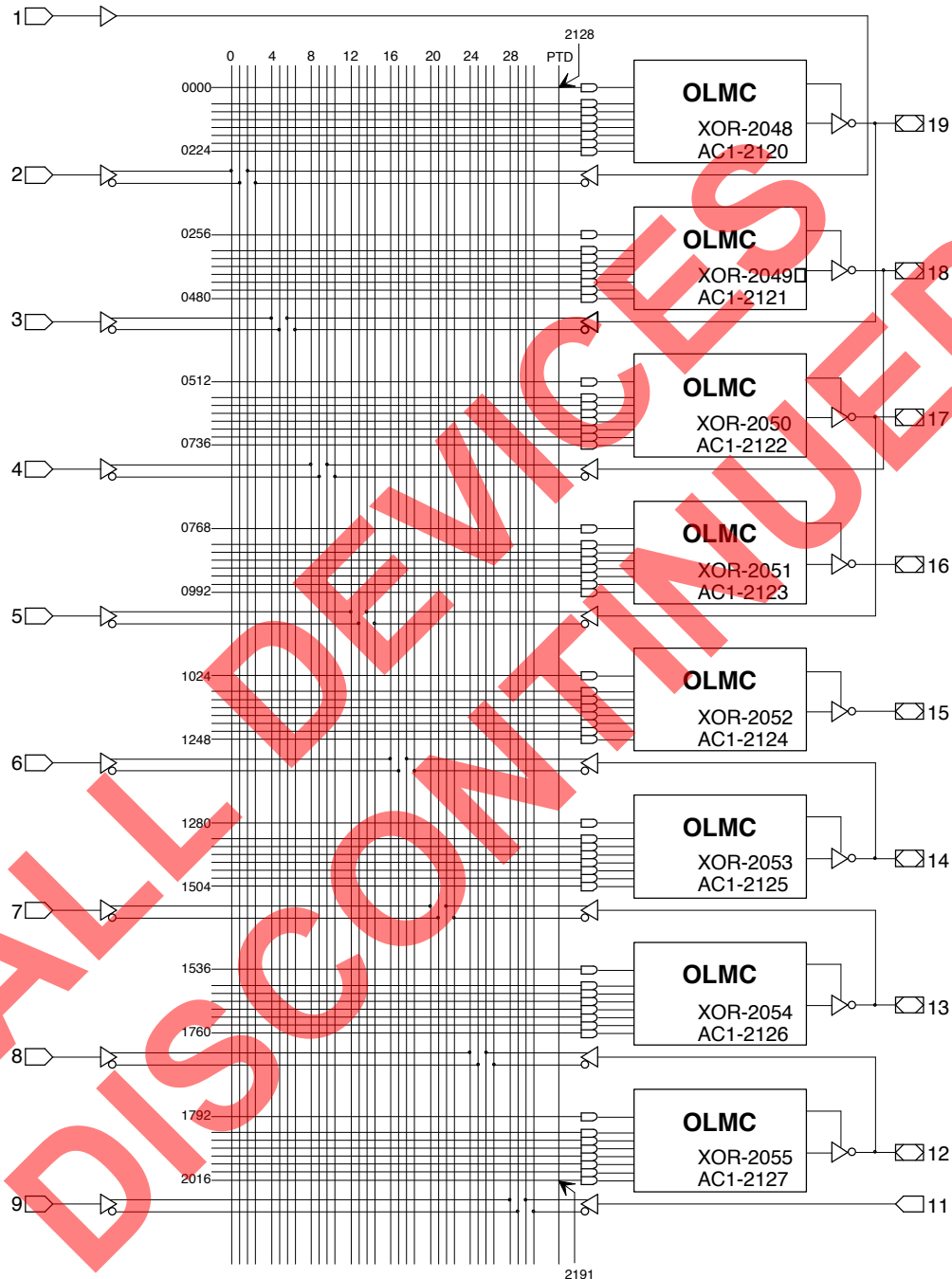
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

**Simple Mode Logic Diagram**

**DIP & PLCC Package Pinouts**



**64-USER ELECTRONIC SIGNATURE FUSES**

2056, 2057, ....	.... 2118, 2119
Byte 7   Byte 6 ....	.... Byte 1   Byte 0

M L  
S S  
B B

SYN-2192  
AC0-2193

## Absolute Maximum Ratings<sup>(1)</sup>

Supply voltage  $V_{CC}$  ..... -0.5 to +7V  
 Input voltage applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Off-state output voltage applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Storage Temperature ..... -65 to 150°C  
 Ambient Temperature with

Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## Recommended Operating Conditions

### Commercial Devices:

Ambient Temperature ( $T_A$ ) ..... 0 to 75°C  
 Supply voltage ( $V_{CC}$ )  
 with Respect to Ground ..... +4.75 to +5.25V

### Industrial Devices:

Ambient Temperature ( $T_A$ ) ..... -40 to 85°C  
 Supply voltage ( $V_{CC}$ )  
 with Respect to Ground ..... +4.50 to +5.50V

## DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>3</sup>	MAX.	UNITS
<b>V<sub>IL</sub></b>	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
<b>V<sub>IH</sub></b>	Input High Voltage		2.0	—	$V_{CC} + 1$	V
<b>I<sub>IL</sub></b> <sup>1</sup>	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
<b>I<sub>IH</sub></b>	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
<b>V<sub>OL</sub></b>	Output Low Voltage	$I_{OL} = MAX.$ $V_{IN} = V_{IL}$ or $V_{IH}$	—	—	0.5	V
<b>V<sub>OH</sub></b>	Output High Voltage	$I_{OH} = MAX.$ $V_{IN} = V_{IL}$ or $V_{IH}$	2.4	—	—	V
<b>I<sub>OL</sub></b>	Low Level Output Current	L-3/-5 & -7 (Ind. PLCC)	—	—	16	mA
		L-7 (Except Ind. PLCC)/-10/-15/-25 Q-10/-15/-20/-25	—	—	24	mA
<b>I<sub>OH</sub></b>	High Level Output Current		—	—	-3.2	mA
<b>I<sub>OS</sub></b> <sup>2</sup>	Output Short Circuit Current	$V_{CC} = 5V$ $V_{OUT} = 0.5V$ $T_A = 25^\circ C$	-30	—	-150	mA

### COMMERCIAL

<b>I<sub>CC</sub></b>	Operating Power Supply Current	$V_{IL} = 0.5V$ $V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L-3/-5/-7/-10	—	75	115	mA
			L-15/-25	—	75	90	mA
			Q-10/-15/-25	—	45	55	mA

### INDUSTRIAL

<b>I<sub>CC</sub></b>	Operating Power Supply Current	$V_{IL} = 0.5V$ $V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L-7/-10/-15/-25	—	75	130	mA
			Q-20/-25	—	45	65	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second.  $V_{out} = 0.5V$  was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.

3) Typical values are at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$

## AC Switching Characteristics

Over Recommended Operating Conditions

			COM		COM		COM / IND		
PARAMETER	TEST COND <sup>1</sup> .	DESCRIPTION	-3		-5		-7		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>pd</sub>	A	Input or I/O to Comb. Output	1	3.5	1	5	1	7.5	ns
t <sub>co</sub>	A	Clock to Output Delay	1	3	1	4	1	5	ns
t <sub>cf</sub> <sup>2</sup>	—	Clock to Feedback Delay	—	2.5	—	3	—	3	ns
t <sub>su</sub>	—	Setup Time, Input or Feedback before Clock↑	2.5	—	3	—	5	—	ns
t <sub>h</sub>	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
f <sub>max</sub> <sup>3</sup>	A	Maximum Clock Frequency with External Feedback, 1/(t <sub>su</sub> + t <sub>co</sub> )	182	—	142.8	—	100	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t <sub>su</sub> + t <sub>cf</sub> )	200	—	166	—	125	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	166	—	125	—	MHz
t <sub>wh</sub>	—	Clock Pulse Duration, High	2 <sup>4</sup>	—	3 <sup>4</sup>	—	4	—	ns
t <sub>wl</sub>	—	Clock Pulse Duration, Low	2 <sup>4</sup>	—	3 <sup>4</sup>	—	4	—	ns
t <sub>en</sub>	B	Input or I/O to Output Enabled	—	4.5	1	6	1	9	ns
	B	$\overline{OE}$ to Output Enabled	—	4.5	1	6	1	6	ns
t <sub>dis</sub>	C	Input or I/O to Output Disabled	—	4.5	1	5	1	9	ns
	C	$\overline{OE}$ to Output Disabled	—	4.5	1	5	1	6	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f<sub>max</sub> with internal feedback. Refer to **f<sub>max</sub> Descriptions** section.

3) Refer to **f<sub>max</sub> Descriptions** section. Characterized but not 100% tested.

4) Characterized but not 100% tested.

## Capacitance (T<sub>A</sub> = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C <sub>I</sub>	Input Capacitance	8	pF	V <sub>CC</sub> = 5.0V, V <sub>I</sub> = 2.0V
C <sub>I/O</sub>	I/O Capacitance	8	pF	V <sub>CC</sub> = 5.0V, V <sub>I/O</sub> = 2.0V

\*Characterized but not 100% tested.

## AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND <sup>1</sup> .	DESCRIPTION	COM / IND		COM / IND		IND		COM / IND		UNITS
			-10		-15		-20		-25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>pd</sub>	A	Input or I/O to Comb. Output	3	10	3	15	3	20	3	25	ns
t <sub>co</sub>	A	Clock to Output Delay	2	7	2	10	2	11	2	12	ns
t <sub>cf</sub> <sup>2</sup>	—	Clock to Feedback Delay	—	6	—	8	—	9	—	10	ns
t <sub>su</sub>	—	Setup Time, Input or Fdbk before Clk ↑	7.5	—	12	—	13	—	15	—	ns
t <sub>h</sub>	—	Hold Time, Input or Fdbk after Clk ↑	0	—	0	—	0	—	0	—	ns
f <sub>max</sub> <sup>3</sup>	A	Maximum Clock Frequency with External Feedback, 1/(t <sub>su</sub> + t <sub>co</sub> )	66.7	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t <sub>su</sub> + t <sub>cf</sub> )	71.4	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	50	—	41.6	—	MHz
t <sub>wh</sub>	—	Clock Pulse Duration, High	6	—	8	—	10	—	12	—	ns
t <sub>wl</sub>	—	Clock Pulse Duration, Low	6	—	8	—	10	—	12	—	ns
t <sub>en</sub>	B	Input or I/O to Output Enabled	1	10	—	15	—	18	—	20	ns
	B	$\overline{\text{OE}}$ to Output Enabled	1	10	—	15	—	18	—	20	ns
t <sub>dis</sub>	C	Input or I/O to Output Disabled	1	10	—	15	—	18	—	20	ns
	C	$\overline{\text{OE}}$ to Output Disabled	1	10	—	15	—	18	—	20	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from **f<sub>max</sub>** with internal feedback. Refer to **f<sub>max</sub> Descriptions** section.

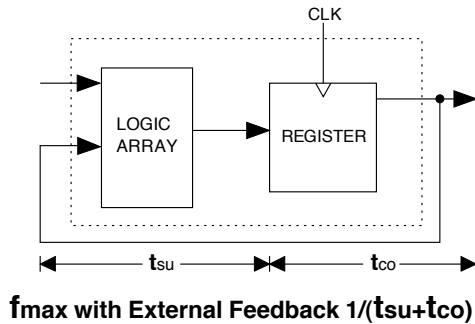
3) Refer to **f<sub>max</sub> Descriptions** section. Characterized but not 100% tested.

## Capacitance (T<sub>A</sub> = 25°C, f = 1.0 MHz)

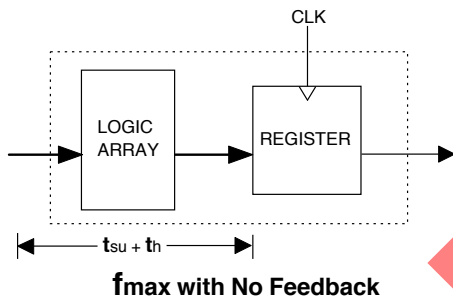
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C <sub>I</sub>	Input Capacitance	8	pF	V <sub>CC</sub> = 5.0V, V <sub>I</sub> = 2.0V
C <sub>I/O</sub>	I/O Capacitance	8	pF	V <sub>CC</sub> = 5.0V, V <sub>I/O</sub> = 2.0V

\*Characterized but not 100% tested.

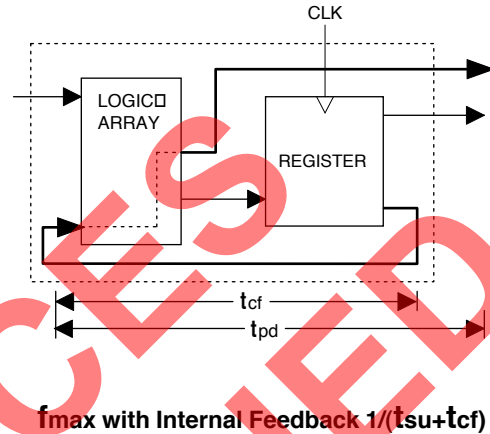
## f<sub>max</sub> Descriptions



**Note:** f<sub>max</sub> with external feedback is calculated from measured tsu and tco.



**Note:** f<sub>max</sub> with no feedback may be less than  $1/(t_{wh} + t_{wl})$ . This is to allow for a clock duty cycle of other than 50%.



**Note:** tcf is a calculated value, derived by subtracting tsu from the period of f<sub>max</sub> w/internal feedback ( $t_{cf} = 1/f_{max} - t_{su}$ ). The value of tcf is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to tcf + tpd.

## Switching Test Conditions

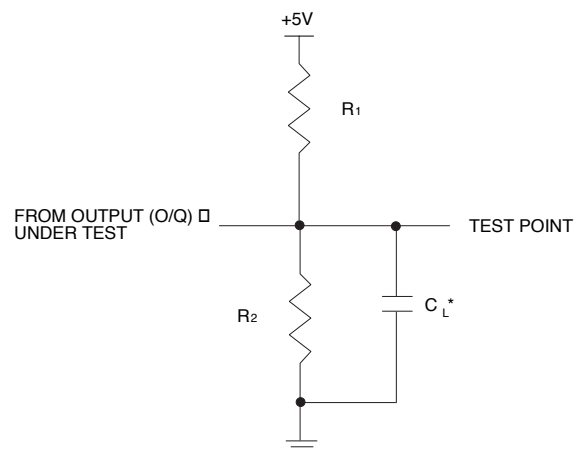
Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL16V8D-10 (and slower)	2 – 3ns 10% – 90%
	GAL16V8D-3/-5/-7	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See figure at right

3-state levels are measured 0.5V from steady-state active level.

Table 2-0003/16V8

**GAL16V8D (except -3) Output Load Conditions (see figure above)**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>
A	200Ω	390Ω	50pF
B	∞	390Ω	50pF
C	200Ω	390Ω	5pF

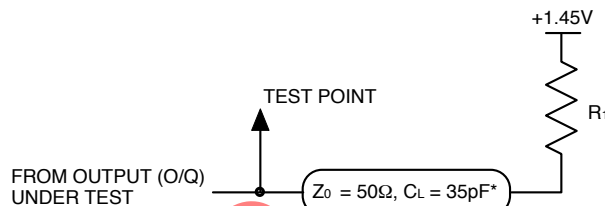


\*C<sub>L</sub> INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

### Switching Test Conditions (Continued)

**GAL16V8D-3 Output Load Conditions (see figure at right)**

Test Condition		R <sub>1</sub>	C <sub>L</sub>
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



\*C<sub>i</sub> includes test fixture and probe capacitance.

### Electronic Signature

An electronic signature is provided in every GAL16V8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

## Security Cell

A security cell is provided in the GAL16V8 devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

## Latch-Up Protection

GAL16V8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

## Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

## Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

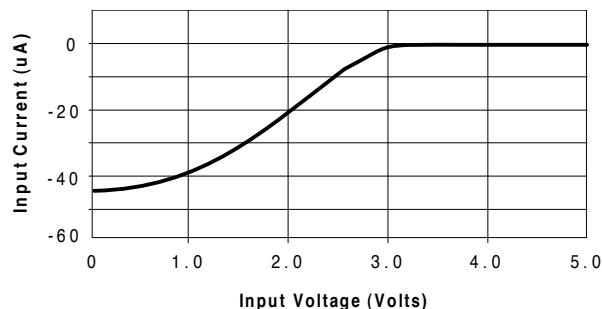
GAL16V8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

# Input Buffers

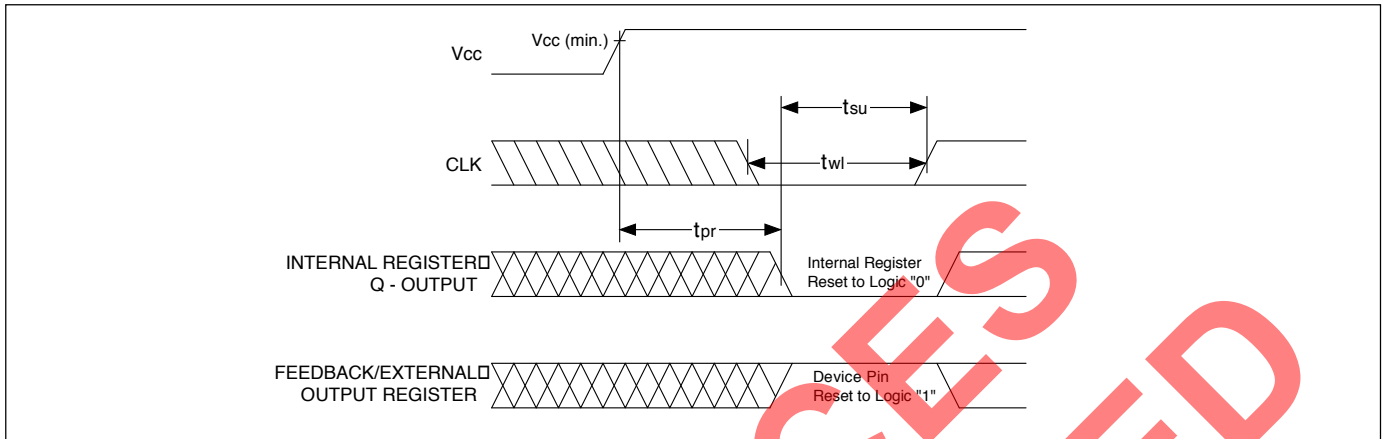
GAL16V8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL16V8 input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V<sub>CC</sub>, or Ground. Doing this will tend to improve noise immunity and reduce I<sub>CC</sub> for the device.

### Typical Input Pull-up Characteristic



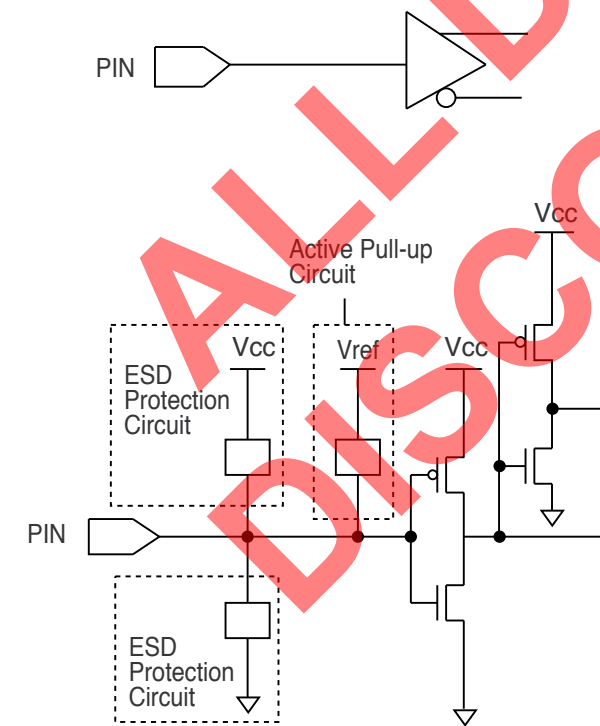
## Power-Up Reset



Circuitry within the GAL16V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time ( $t_{pr}$ , 1  $\mu$ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

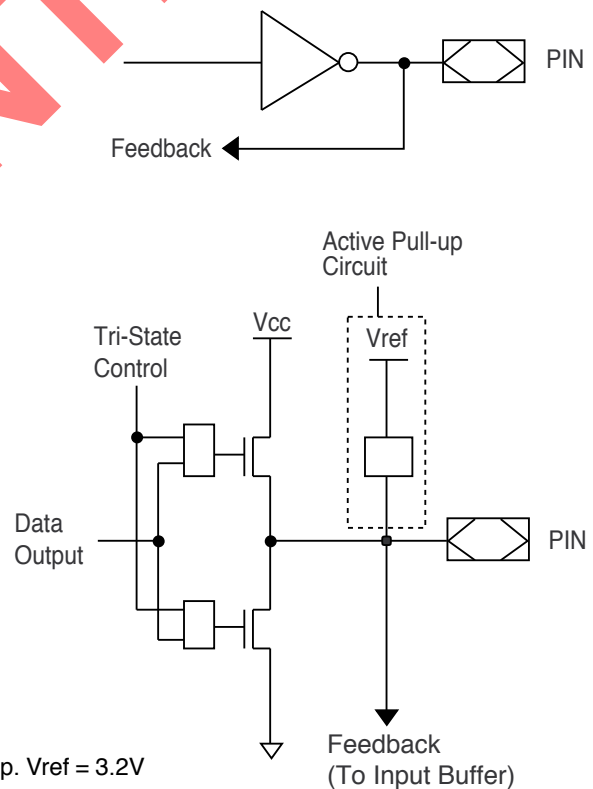
conditions must be met to provide a valid power-up reset of the device. First, the  $V_{CC}$  rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of  $t_{PR}$  time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

## Input/Output Equivalent Schematics



Typ. Vref = 3.2V

### Typical Input

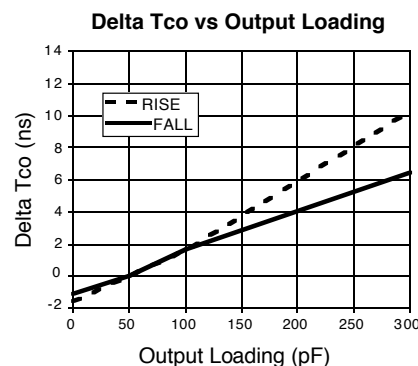
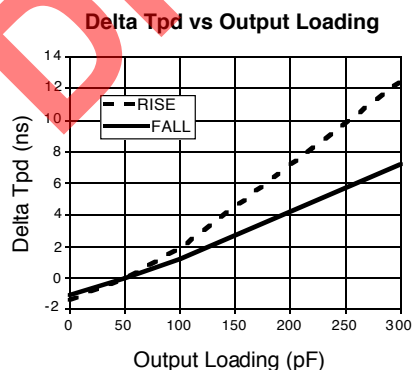
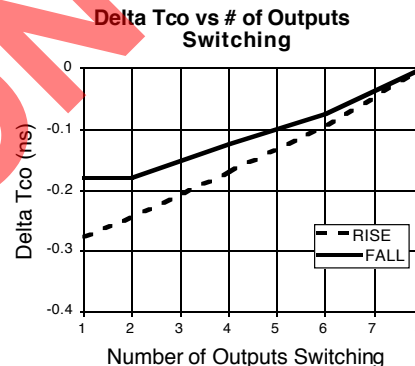
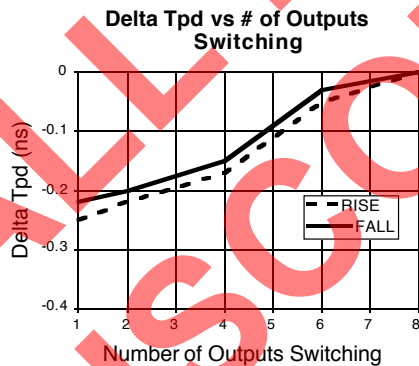
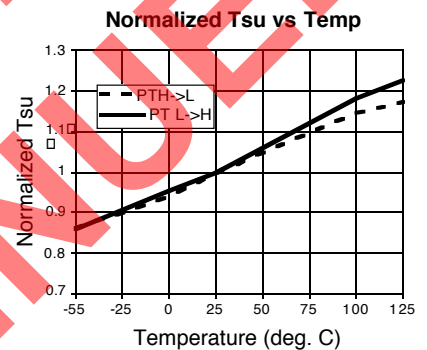
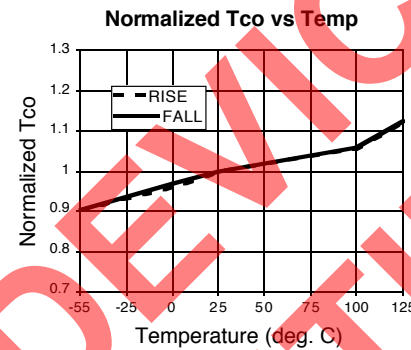
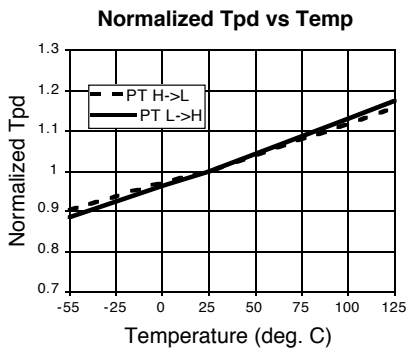
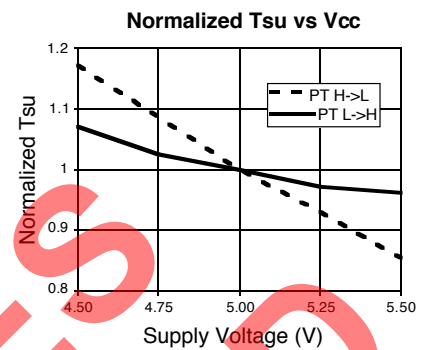
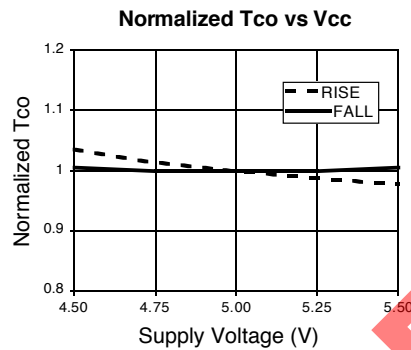
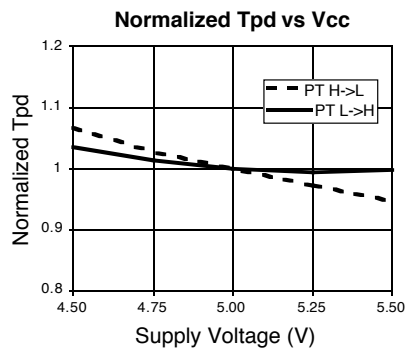


Typ. Vref = 3.2V

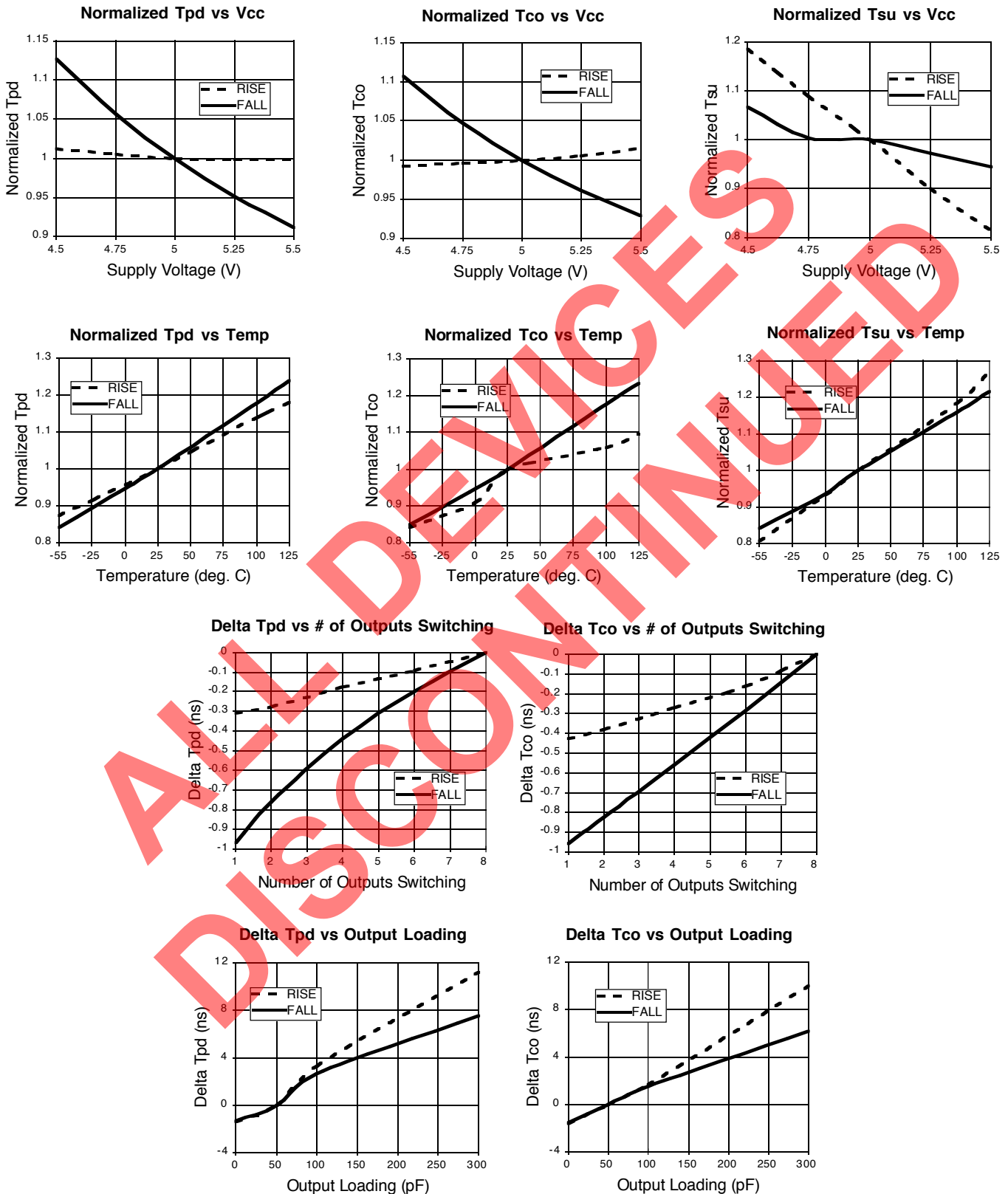
### Typical Output



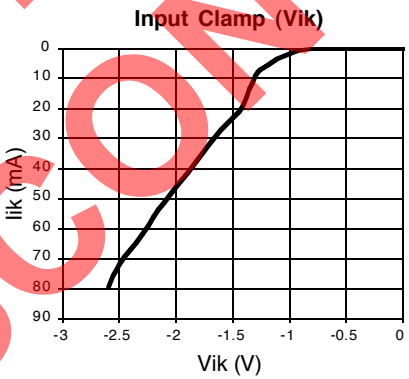
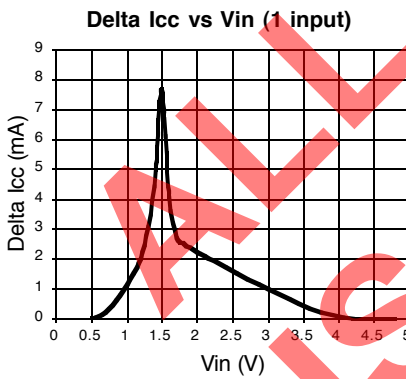
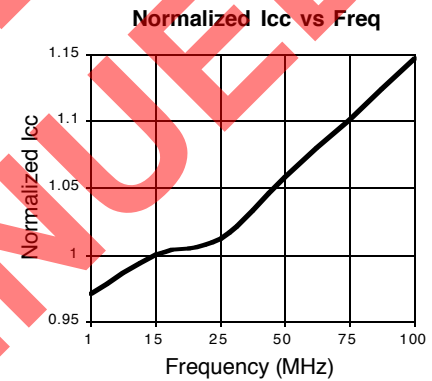
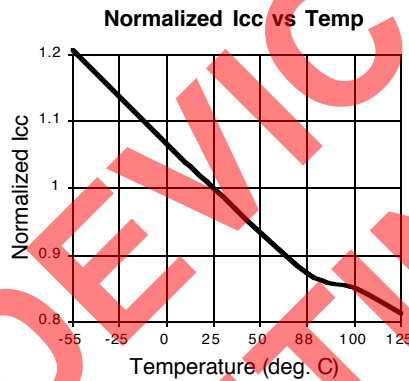
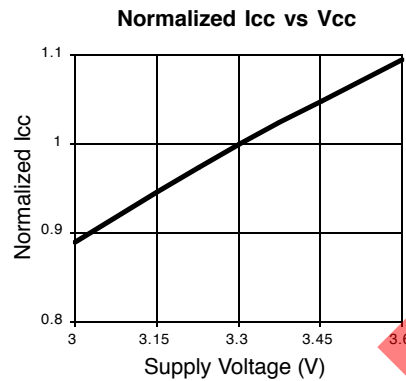
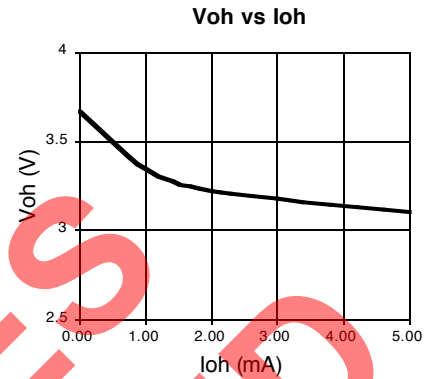
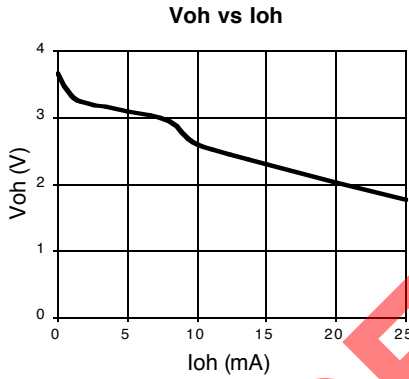
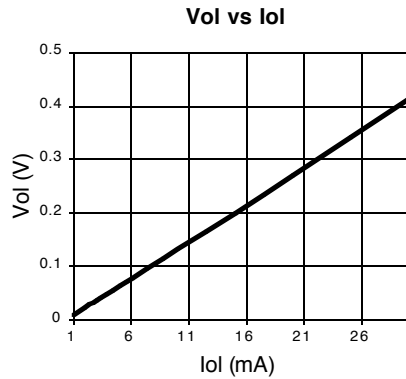
**GAL16V8D-3/-5/-7 (IND PLCC): Typical AC and DC Characteristic Diagrams**



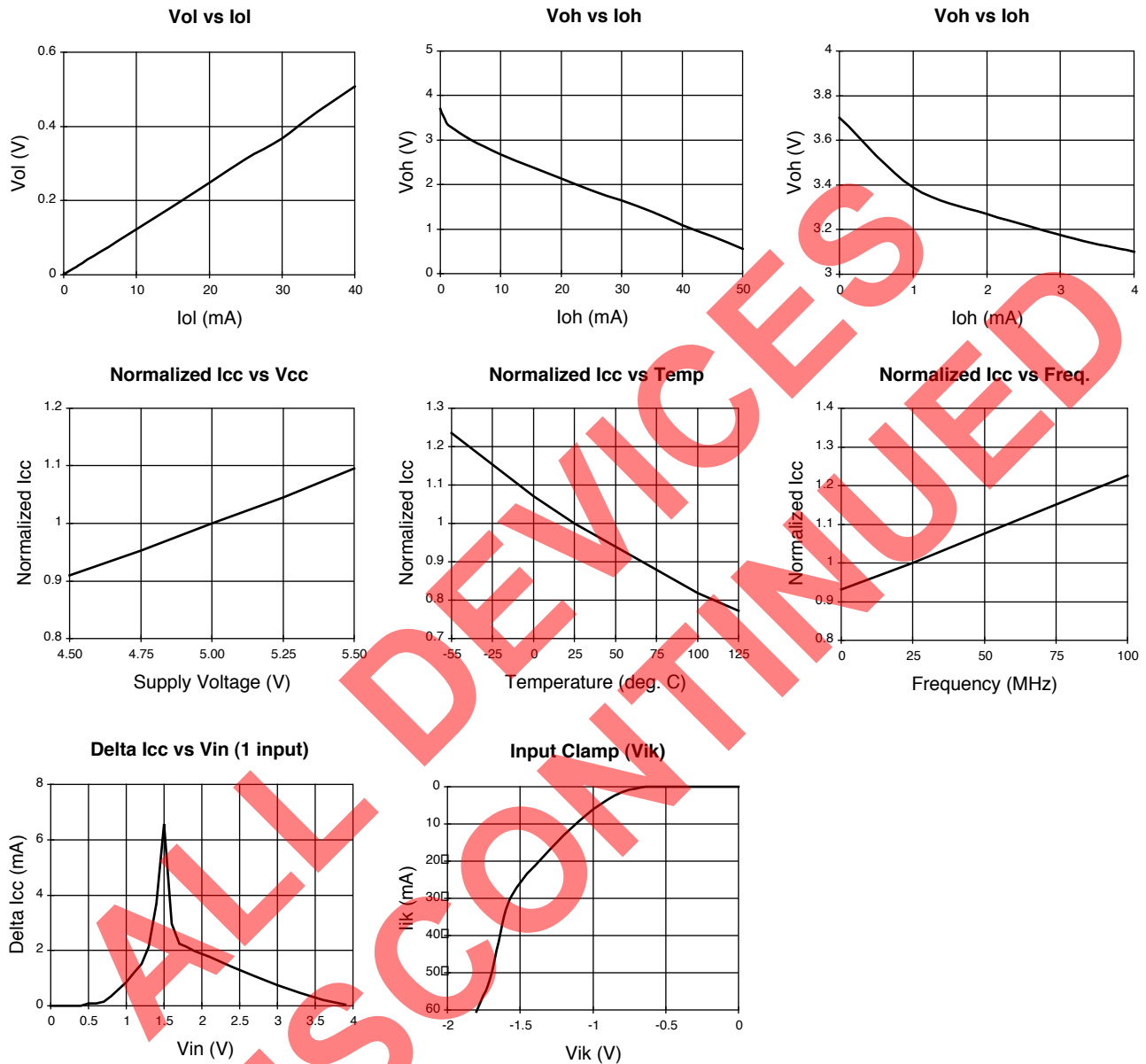
**GAL16V8D-7 (Except IND PLCC)/-10L: Typical AC and DC Characteristic Diagrams**



**GAL16V8D-7 (Except IND PLCC)/-10L: Typical AC and DC Characteristic Diagrams**



**GAL16V8D-10Q (and Slower): Typical AC and DC Characteristic Diagrams**



**Revision History**

Date	Version	Change Summary
-	16v8_10	Previous Lattice release.
August 2006	16v8_11	Updated for lead-free package options.

ALL DEVICES  
DISCONTINUED