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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	8
Number of Gates	-
Number of I/O	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LCC (J-Lead)
Supplier Device Package	20-PLCC (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/gal16v8d-20qji

Product Line	Ordering Part Number	Product Status	Reference PCN
GAL16V8D (Cont'd)	GAL16V8D-7LJ	**Discontinued**	PCN#13-10
	GAL16V8D-7LJN		
	GAL16V8D-10LJ		
	GAL16V8D-10LJN		
	GAL16V8D-15LJ		
	GAL16V8D-15LJN		
	GAL16V8D-25LJ		
	GAL16V8D-25LJN		
	GAL16V8D-7LJI		PCN#09-10
	GAL16V8D-7LJNI		
	GAL16V8D-10LJI		PCN#13-10
	GAL16V8D-10LJNI		
	GAL16V8D-15LJI		
	GAL16V8D-15LJNI		
	GAL16V8D-25LJI		
	GAL16V8D-25LJNI		
	GAL16V8D-10QJ		
	GAL16V8D-10QJN		
	GAL16V8D-15QJ		
	GAL16V8D-15QJN		
	GAL16V8D-25QJ		
	GAL16V8D-25QJN		
	GAL16V8D-20QJI		
	GAL16V8D-20QJNI		
	GAL16V8D-25QJI		
	GAL16V8D-25QJNI		
	GAL16V8D-7LS		PCN#06-07
	GAL16V8D-10LS		
	GAL16V8D-15LS		
	GAL16V8D-25LS		

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Internet: http://www.latticesemi.com

Lattice Semiconductor Corporation

Lead-Free Package Options Available!

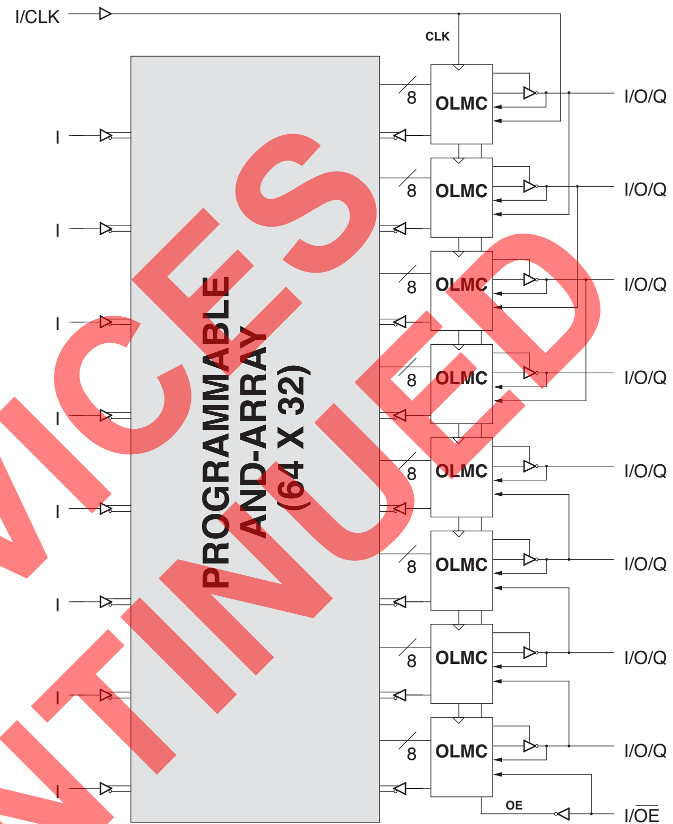
GAL16V8

High Performance E²CMOS PLD
Generic Array Logic™

Features

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 3.5 ns Maximum Propagation Delay
  - Fmax = 250 MHz
  - 3.0 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- 50% to 75% REDUCTION IN POWER FROM BIPOLAR
  - 75mA Typ Icc on Low Power Device
  - 45mA Typ Icc on Quarter Power Device
- ACTIVE PULL-UPS ON ALL PINS
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION
- LEAD-FREE PACKAGE OPTIONS

Functional Block Diagram



Description

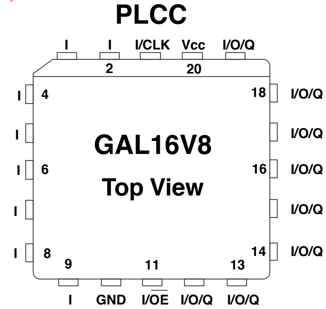
The GAL16V8, at 3.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 are the PAL architectures listed in the table of the macrocell description section. GAL16V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

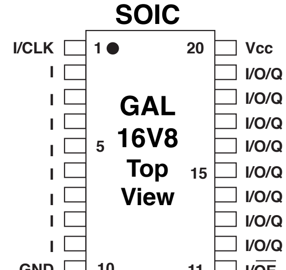
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

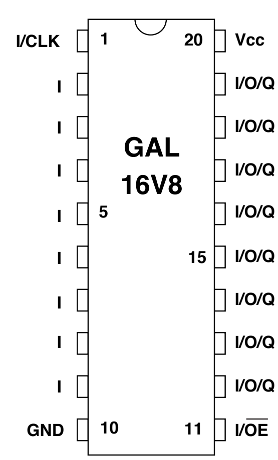
PLCC



SOIC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
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August 2006

Lead-Free Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
3.5	2.5	3.0	115	GAL16V8D-3LJN[1]	Lead-Free 20-Lead PLCC
5	3	4	115	GAL16V8D-5LJN	Lead-Free 20-Lead PLCC
7.5	7	5	115	GAL16V8D-7LPN	Lead-Free 20-Pin Plastic DIP
			115	GAL16V8D-7LJN	Lead-Free 20-Lead PLCC
10	10	7	55	GAL16V8D-10QPN	Lead-Free 20-Pin Plastic DIP
			55	GAL16V8D-10QJN	Lead-Free 20-Lead PLCC
			115	GAL16V8D-10LPN	Lead-Free 20-Pin Plastic DIP
			115	GAL16V8D-10LJN	Lead-Free 20-Lead PLCC
15	12	10	55	GAL16V8D-15QPN	Lead-Free 20-Pin Plastic DIP
			55	GAL16V8D-15QJN	Lead-Free 20-Lead PLCC
			90	GAL16V8D-15LPN	Lead-Free 20-Pin Plastic DIP
			90	GAL16V8D-15LJN	Lead-Free 20-Lead PLCC
25	15	12	55	GAL16V8D-25QPN	Lead-Free 20-Pin Plastic DIP
			55	GAL16V8D-25QJN	Lead-Free 20-Lead PLCC
			90	GAL16V8D-25LPN	Lead-Free 20-Pin Plastic DIP
			90	GAL16V8D-25LJN	Lead-Free 20-Lead PLCC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	130	GAL16V8D-7LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-7LPNI	Lead-Free 20-Pin Plastic DIP
10	10	7	130	GAL16V8D-10LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-10LPNI	Lead-Free 20-Pin Plastic DIP
15	12	10	130	GAL16V8D-15LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-15LPNI	Lead-Free 20-Pin Plastic DIP
20	13	11	65	GAL16V8D-20QJNI	Lead-Free 20-Lead PLCC
			65	GAL16V8D-20QPNI	Lead-Free 20-Pin Plastic DIP
25	15	12	65	GAL16V8D-25QJNI	Lead-Free 20-Lead PLCC
			65	GAL16V8D-25QPNI	Lead-Free 20-Pin Plastic DIP
			130	GAL16V8D-25LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-25LPNI	Lead-Free 20-Pin Plastic DIP

Part Number Description

XXXXXXXX – XX X XX X

GAL16V8D **Device Name**

Speed (ns)

L = Low Power
Q = Quarter Power **Power**

Grade Blank = Commercial
I = Industrial

Package P = Plastic DIP
PN = Lead-free Plastic DIP
J = PLCC
JN = Lead-free PLCC
S = SOIC

Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8 . The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8 can emulate. It also shows the OLMC mode under which the GAL16V8 emulates the PAL architecture.

PAL Architectures Emulated by GAL16V8	GAL16V8 Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

Registered Mode

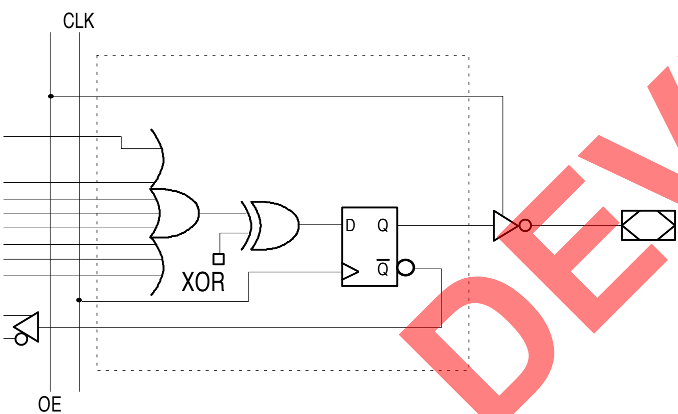
In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

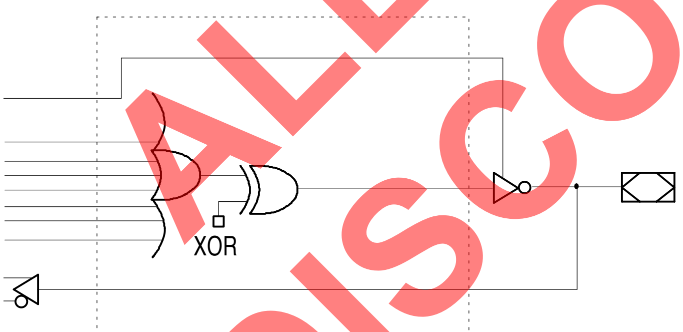
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Complex Mode

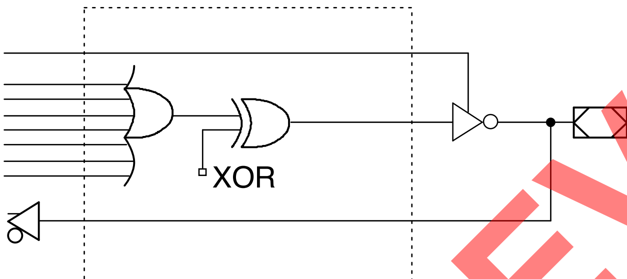
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

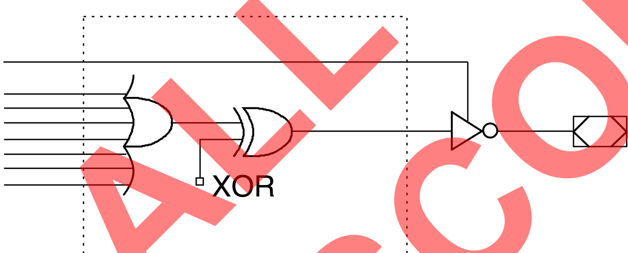
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 13 through Pin 18 are configured to this function.



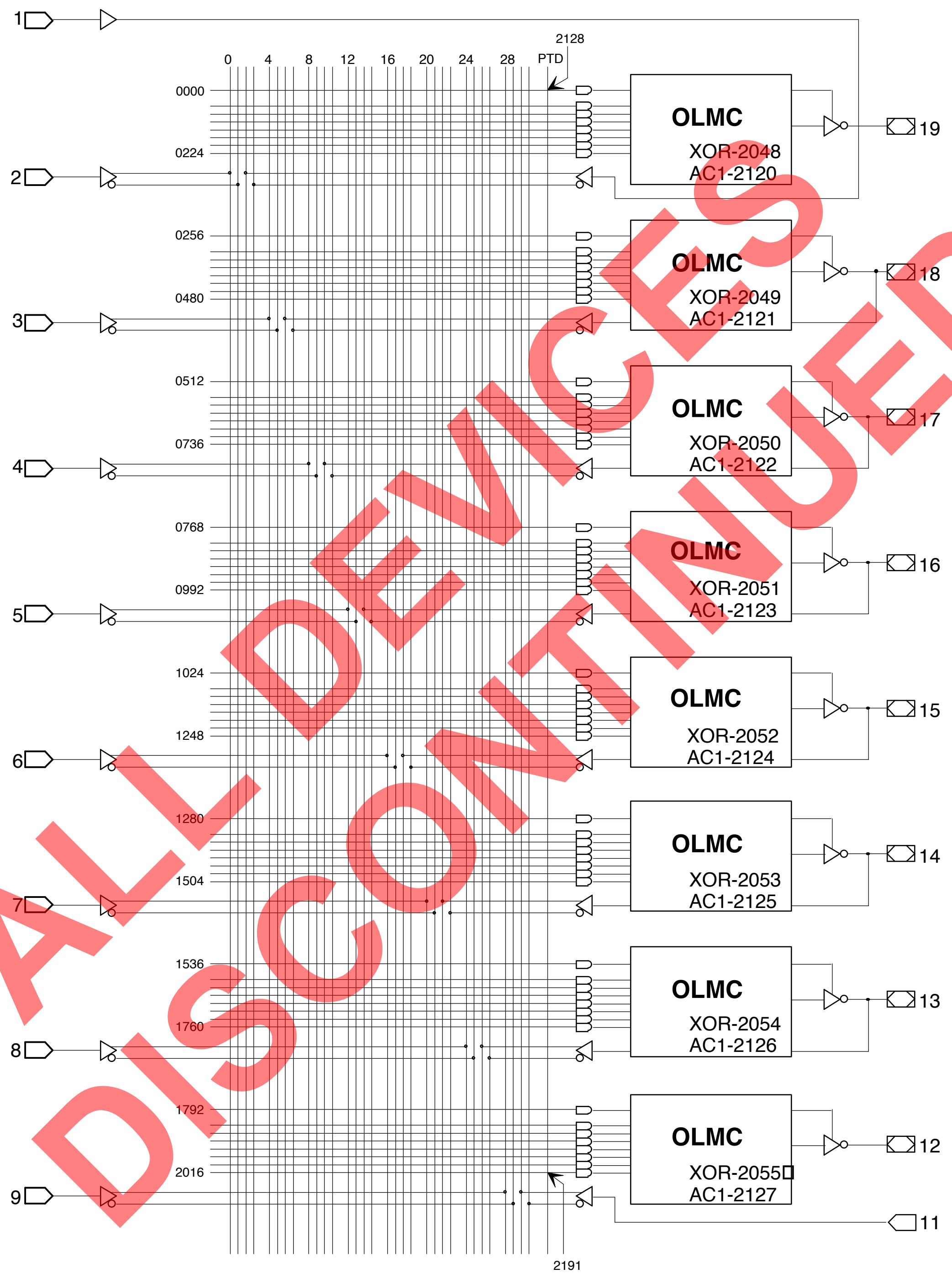
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Complex Mode Logic Diagram

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...			.... 2118, 2119	
Byte 7	Byte 6	....	Byte 1	Byte 0

M L
S S
B B

SYN-2192
AC0-2193

Simple Mode

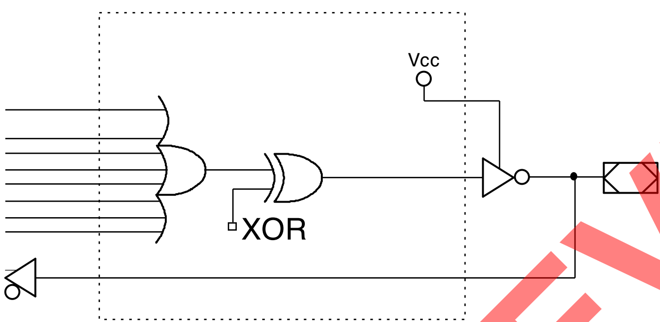
In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

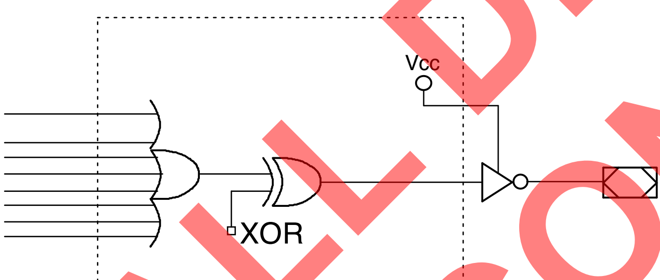
Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used as input or I/O pins, and are only available as dedicated outputs.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



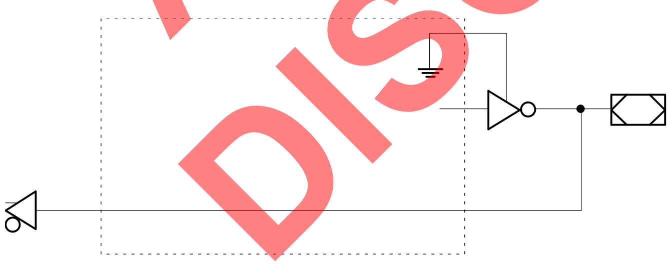
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 15 & 16 are permanently configured to this function.



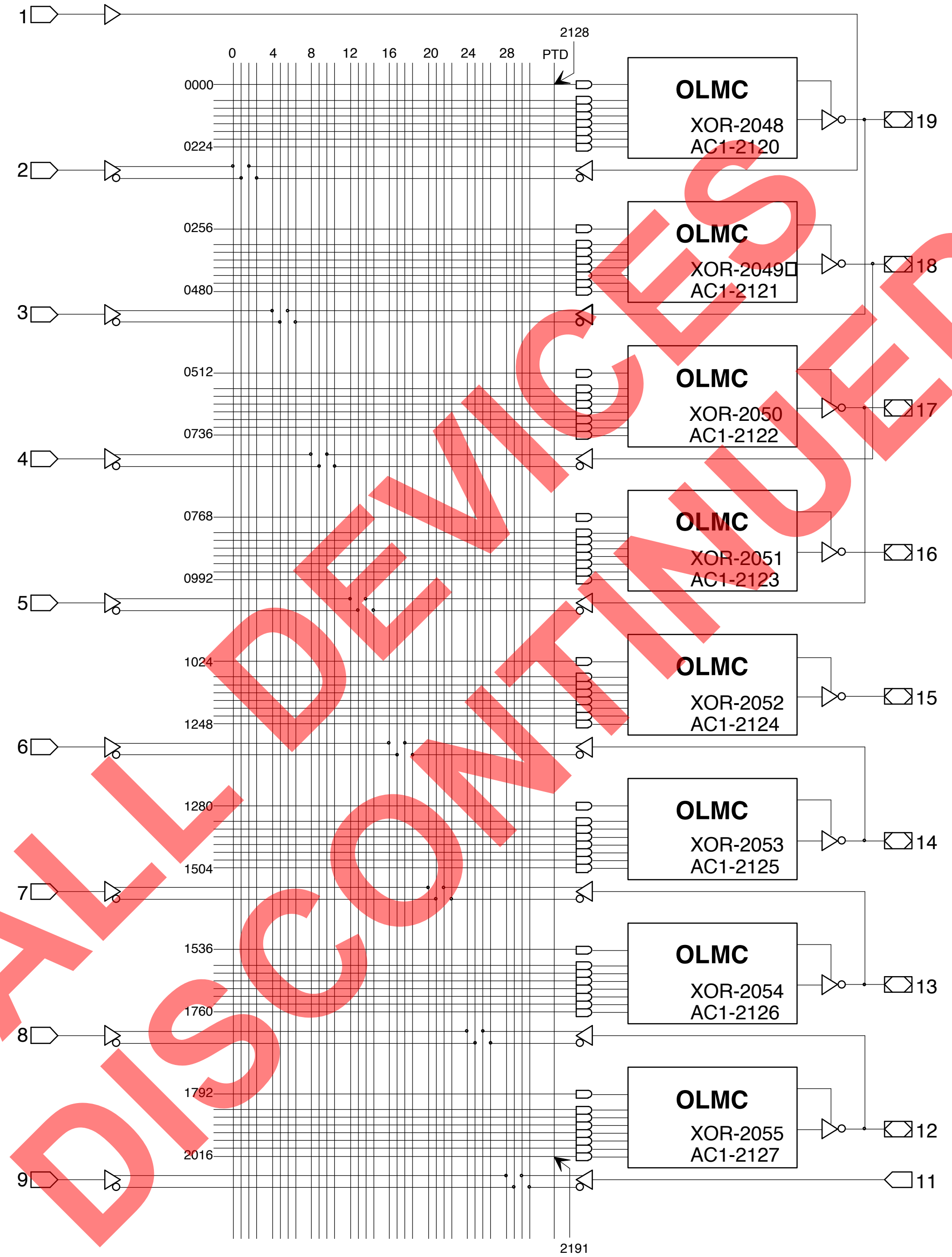
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Simple Mode Logic Diagram

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...			.... 2118, 2119
Byte 7	Byte 6	.... Byte 1	Byte 0

M S B   L S B

SYN-2192
AC0-2193

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -3 MIN.	COM -3 MAX.	COM -5 MIN.	COM -5 MAX.	COM / IND -7 MIN.	COM / IND -7 MAX.	UNITS
tpd	A	Input or I/O to Comb. Output	1	3.5	1	5	1	7.5	ns
tco	A	Clock to Output Delay	1	3	1	4	1	5	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	3	—	3	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	2.5	—	3	—	5	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	182	—	142.8	—	100	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	200	—	166	—	125	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	166	—	125	—	MHz
twh	—	Clock Pulse Duration, High	2[4]	—	3[4]	—	4	—	ns
twl	—	Clock Pulse Duration, Low	2[4]	—	3[4]	—	4	—	ns
ten	B	Input or I/O to Output Enabled	—	4.5	1	6	1	9	ns
	B	$\overline{OE}$ to Output Enabled	—	4.5	1	6	1	6	ns
tdis	C	Input or I/O to Output Disabled	—	4.5	1	5	1	9	ns
	C	$\overline{OE}$ to Output Disabled	—	4.5	1	5	1	6	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **fmax** with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section. Characterized but not 100% tested.
4) Characterized but not 100% tested.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION	COM / IND -10 MIN.	MAX.	COM / IND -15 MIN.	MAX.	IND -20 MIN.	MAX.	COM / IND -25 MIN.	MAX.	UNITS
tpd	A	Input or I/O to Comb. Output	3	10	3	15	3	20	3	25	ns
tco	A	Clock to Output Delay	2	7	2	10	2	11	2	12	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	8	—	9	—	10	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	7.5	—	12	—	13	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	66.7	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	71.4	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	50	—	41.6	—	MHz
twh	—	Clock Pulse Duration, High	6	—	8	—	10	—	12	—	ns
twl	—	Clock Pulse Duration, Low	6	—	8	—	10	—	12	—	ns
ten	B	Input or I/O to Output Enabled	1	10	—	15	—	18	—	20	ns
	B	$\overline{OE}$ to Output Enabled	1	10	—	15	—	18	—	20	ns
tdis	C	Input or I/O to Output Disabled	1	10	—	15	—	18	—	20	ns
	C	$\overline{OE}$ to Output Disabled	1	10	—	15	—	18	—	20	ns

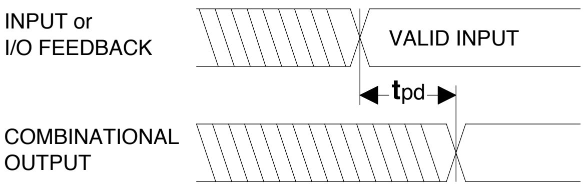
1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section. Characterized but not 100% tested.

Capacitance (T_A = 25°C, f = 1.0 MHz)

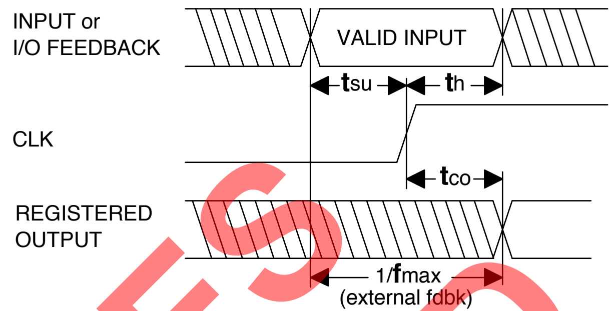
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

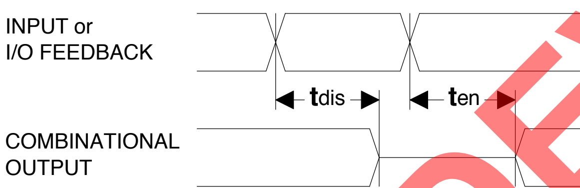
Switching Waveforms



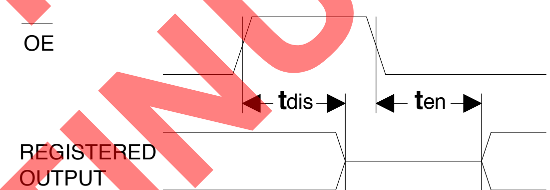
Combinatorial Output



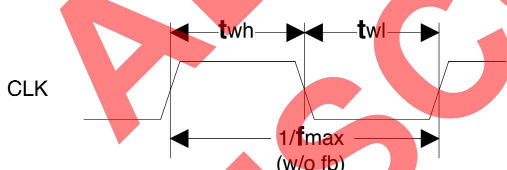
Registered Output



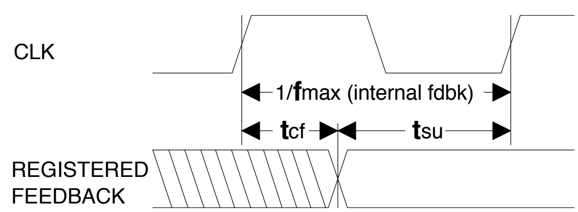
Input or I/O to Output Enable/Disable



$\overline{\text{OE}}$ to Output Enable/Disable

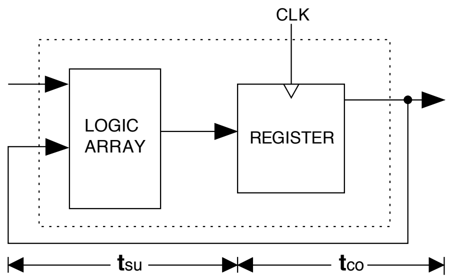


Clock Width



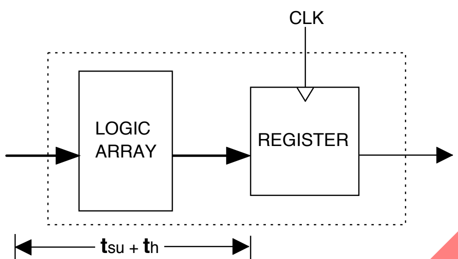
fmax with Feedback

fmax Descriptions



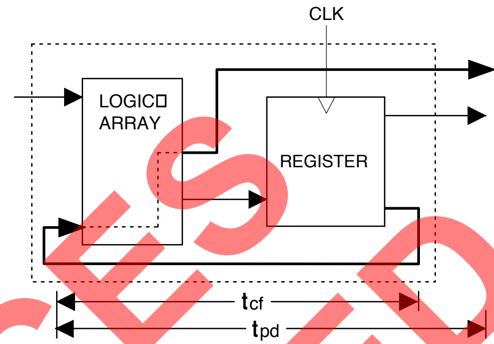
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

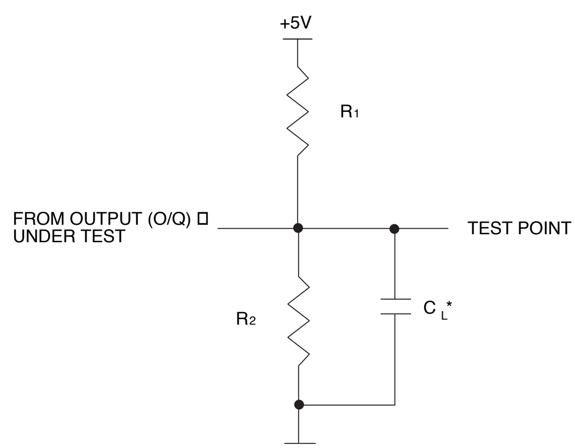
Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

Switching Test Conditions

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL16V8D-10 (and slower)	2 – 3ns 10% – 90%
	GAL16V8D-3/-5/-7	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See figure at right

Table 2-0003/16V8

3-state levels are measured 0.5V from steady-state active level.

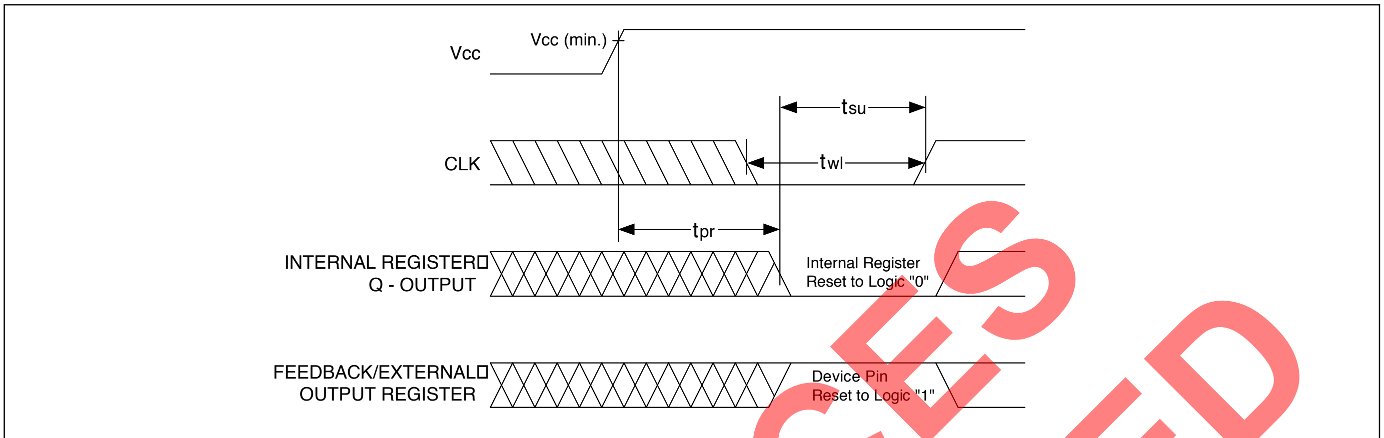


*CL INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL16V8D (except -3) Output Load Conditions (see figure above)

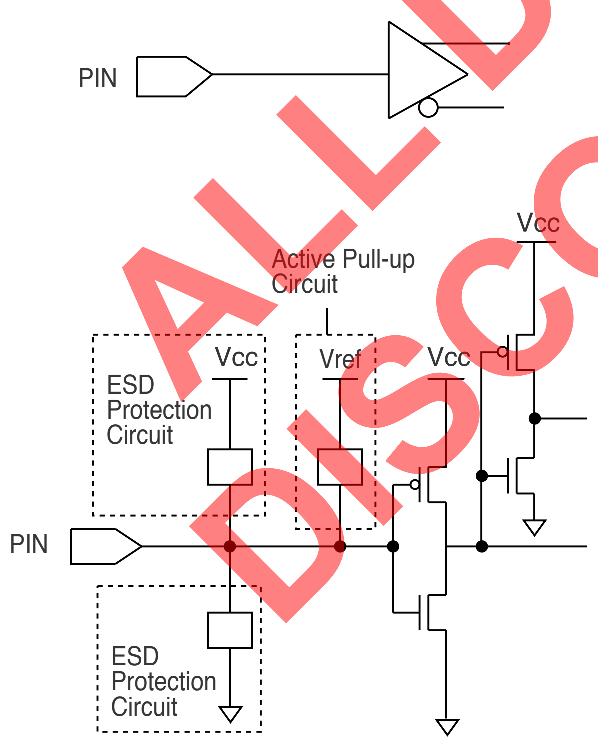
Test Condition		R1	R2	CL
A		200Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

Power-Up Reset



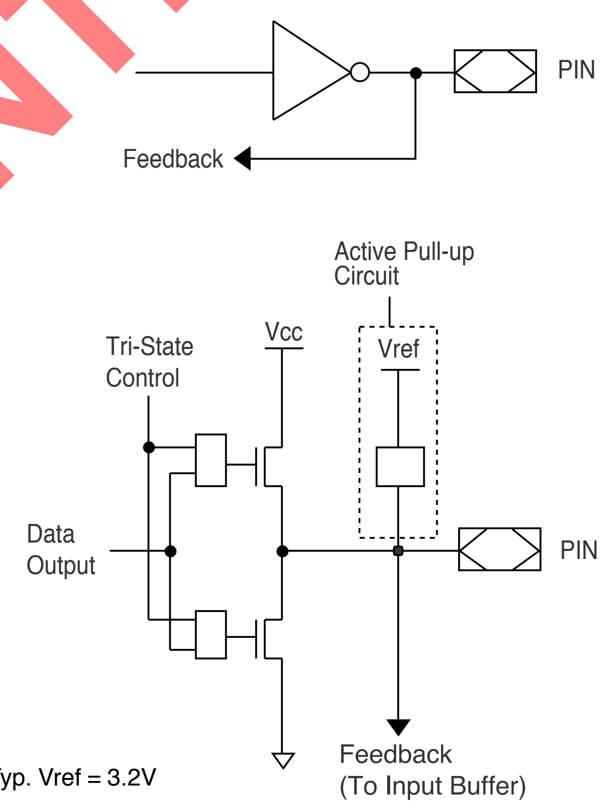
Circuitry within the GAL16V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



Typ. Vref = 3.2V

Typical Input

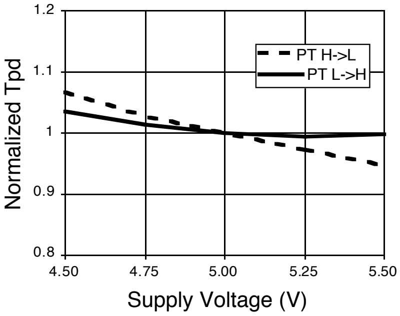


Typ. Vref = 3.2V

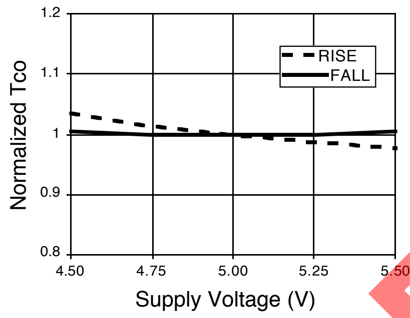
Typical Output

GAL16V8D-3/-5/-7 (IND PLCC): Typical AC and DC Characteristic Diagrams

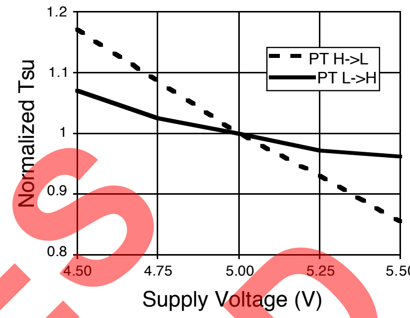
Normalized Tpd vs Vcc



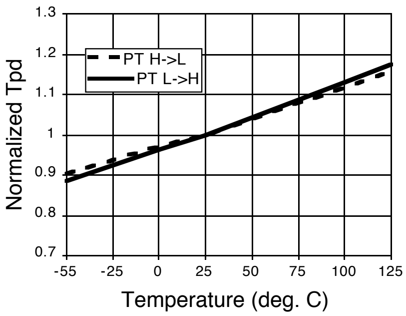
Normalized Tco vs Vcc



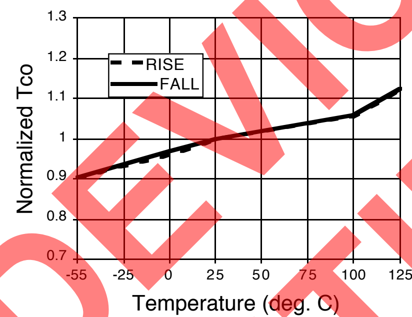
Normalized Tsu vs Vcc



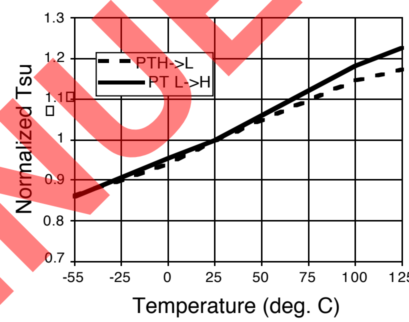
Normalized Tpd vs Temp



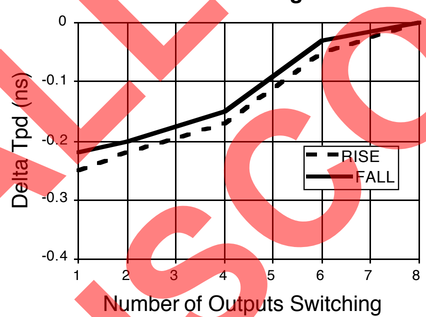
Normalized Tco vs Temp



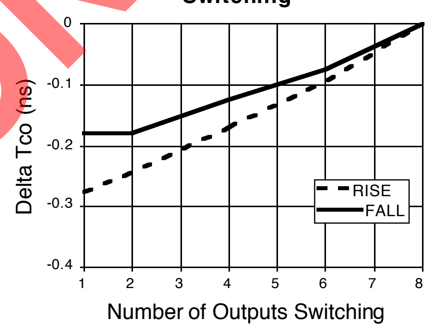
Normalized Tsu vs Temp



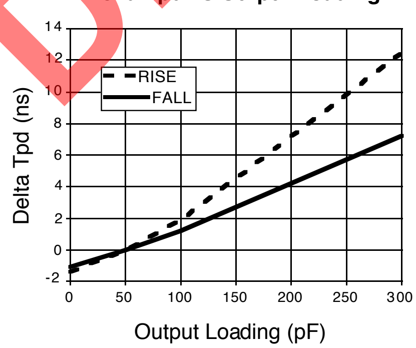
Delta Tpd vs # of Outputs Switching



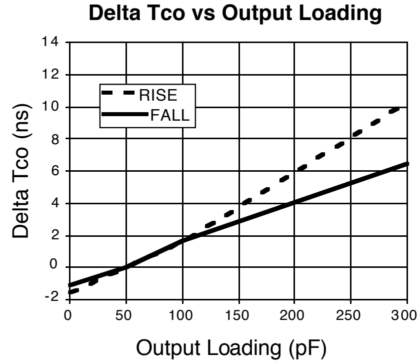
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

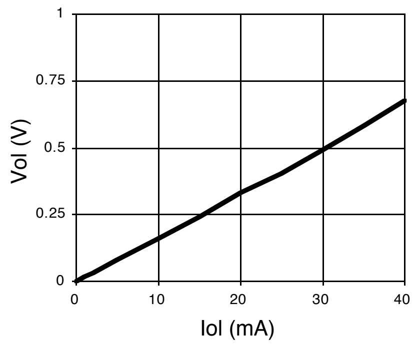


Delta Tco vs Output Loading

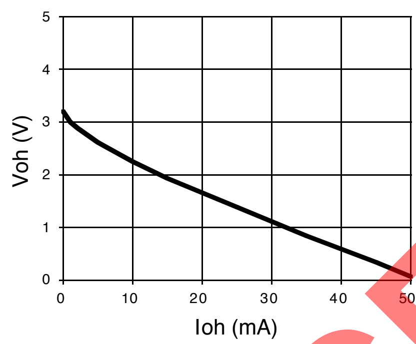


GAL16V8D-3/-5/-7 (IND PLCC): Typical AC and DC Characteristic Diagrams

Vol vs Iol

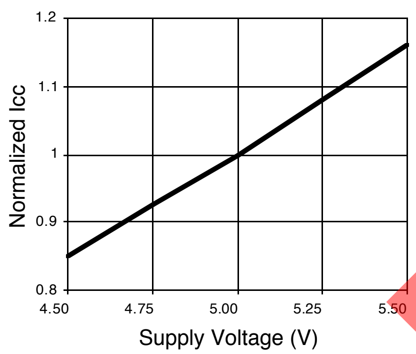


Voh vs Ioh

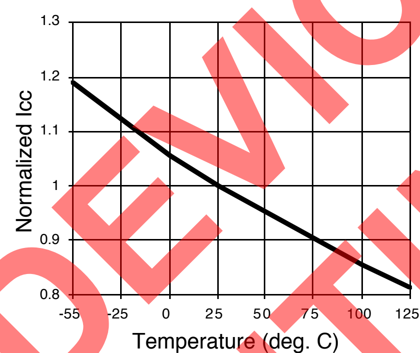


Voh vs Ioh

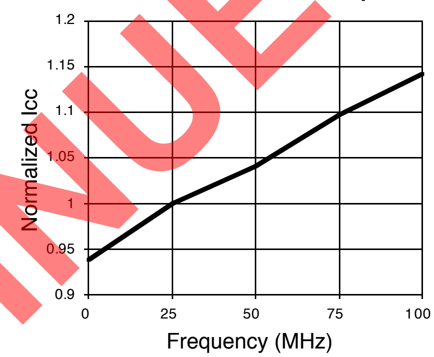
Normalized Icc vs Vcc



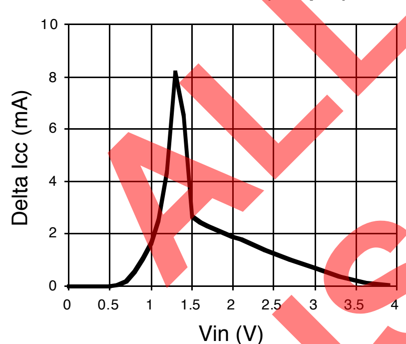
Normalized Icc vs Temp



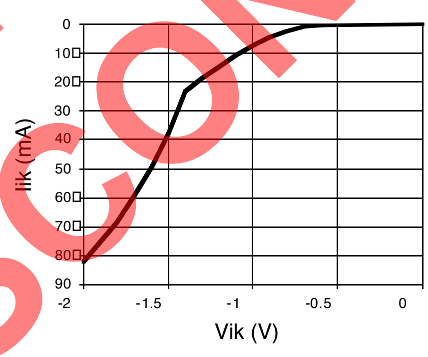
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

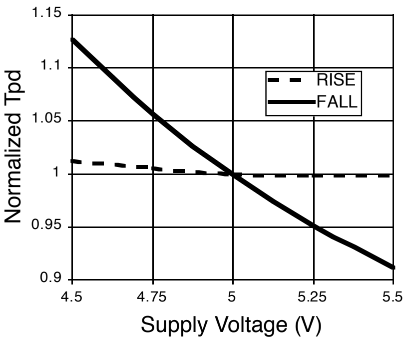


Input Clamp (Vik)

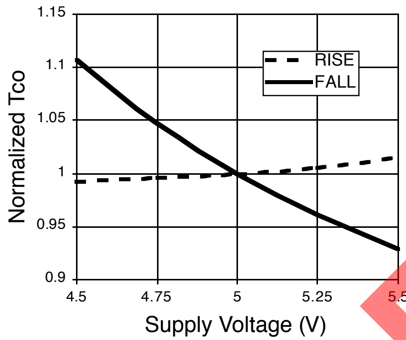


GAL16V8D-7 (Except IND PLCC)/-10L: Typical AC and DC Characteristic Diagrams

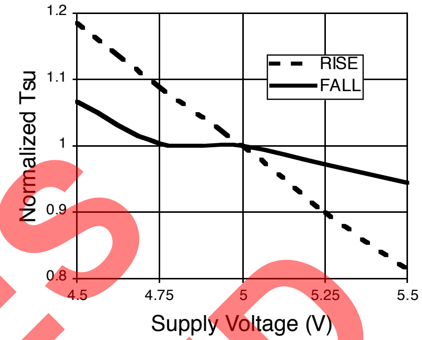
Normalized Tpd vs Vcc



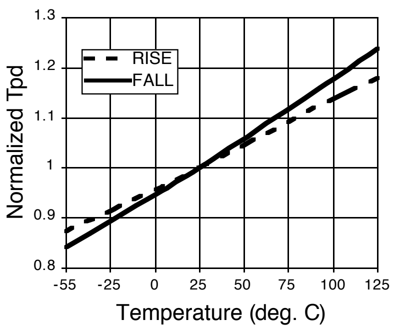
Normalized Tco vs Vcc



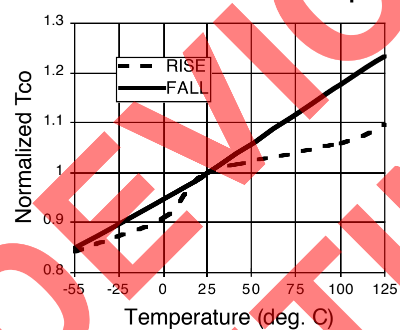
Normalized Tsu vs Vcc



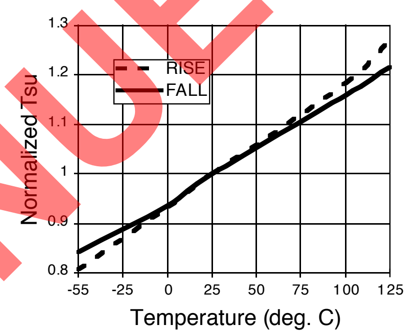
Normalized Tpd vs Temp



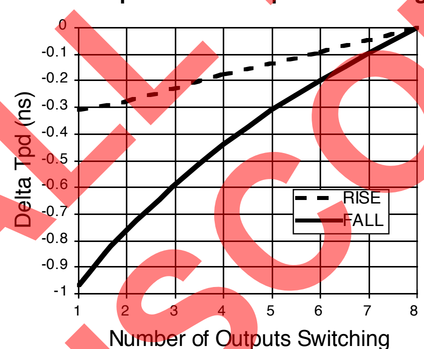
Normalized Tco vs Temp



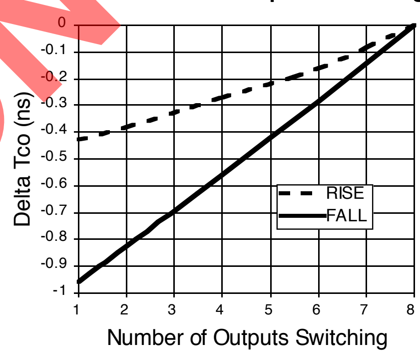
Normalized Tsu vs Temp



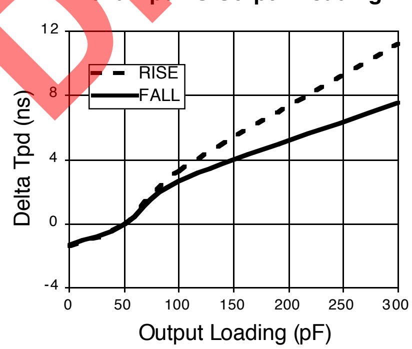
Delta Tpd vs # of Outputs Switching



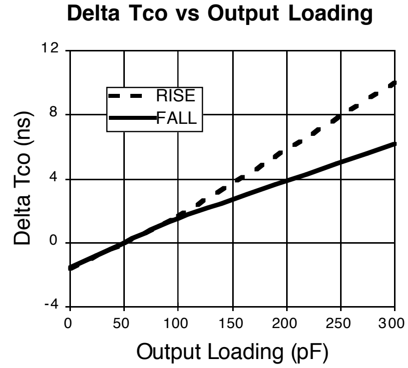
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

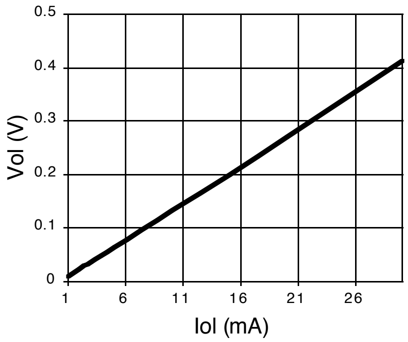


Delta Tco vs Output Loading

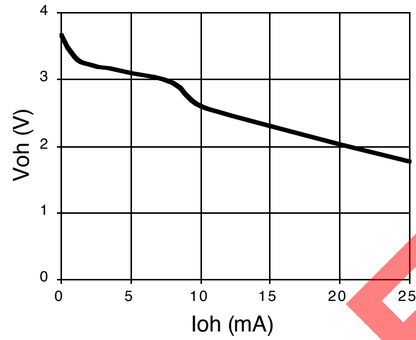


GAL16V8D-7 (Except IND PLCC)/-10L: Typical AC and DC Characteristic Diagrams

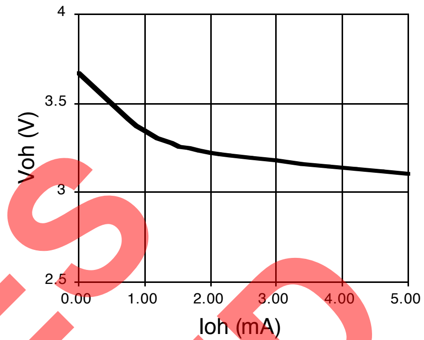
Vol vs Iol



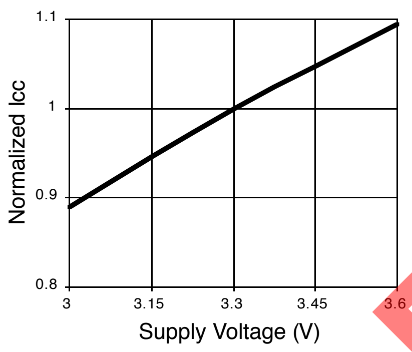
Voh vs Ioh



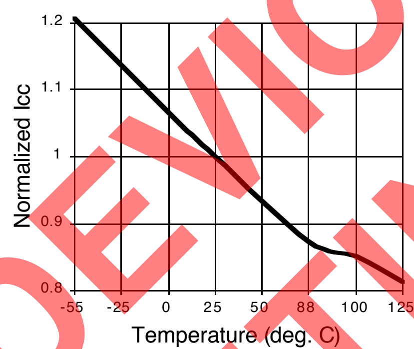
Voh vs Ioh



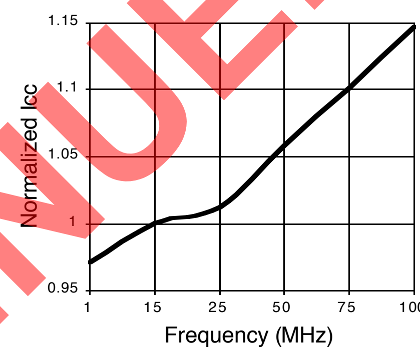
Normalized Icc vs Vcc



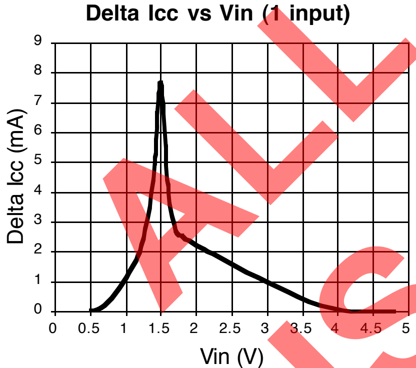
Normalized Icc vs Temp



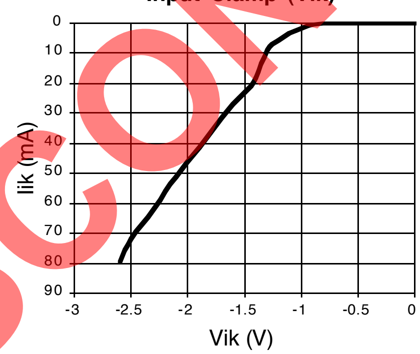
Normalized Icc vs Freq



Delta Icc vs Vin (1 input)

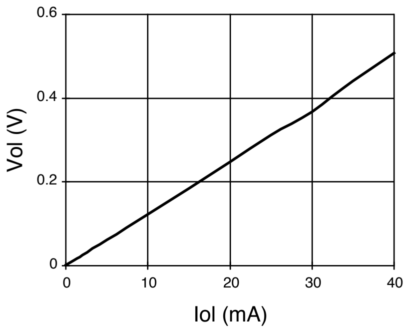


Input Clamp (Vik)

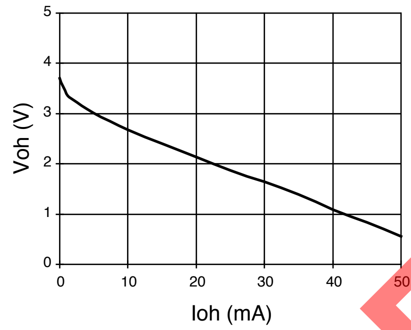


GAL16V8D-10Q (and Slower): Typical AC and DC Characteristic Diagrams

Vol vs Iol

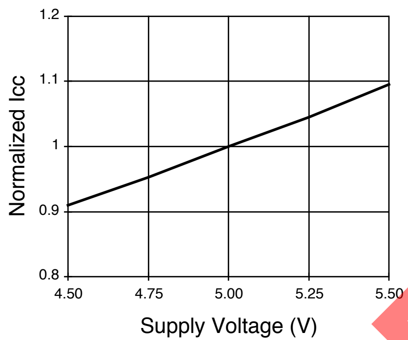


Voh vs Ioh

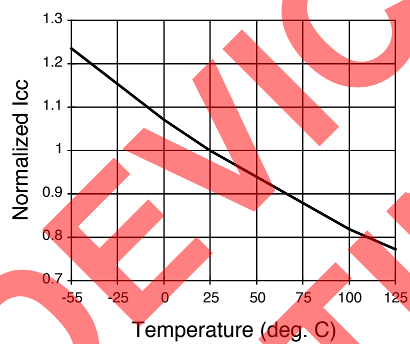


Voh vs Ioh

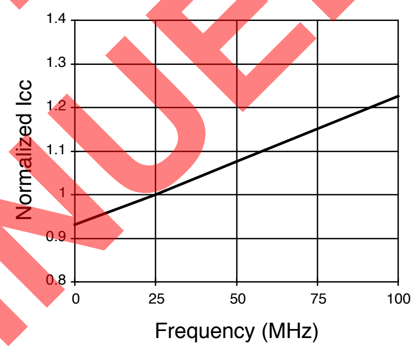
Normalized Icc vs Vcc



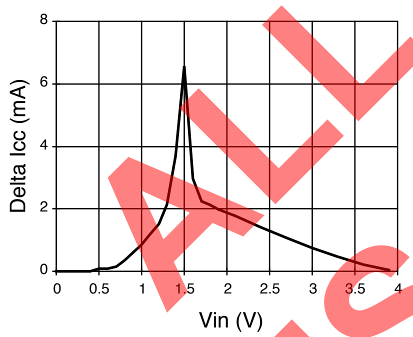
Normalized Icc vs Temp



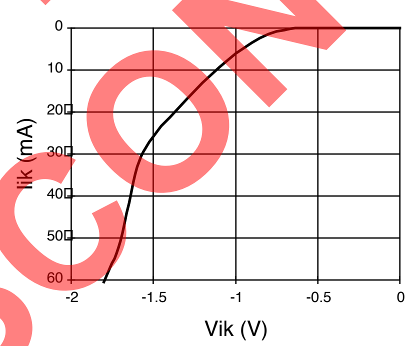
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Revision History

Date	Version	Change Summary
-	16v8_10	Previous Lattice release.
August 2006	16v8_11	Updated for lead-free package options.