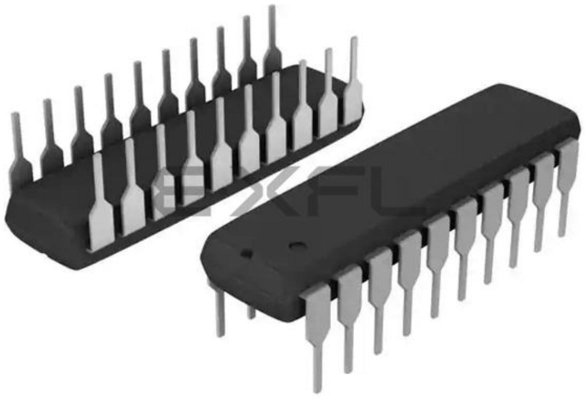


Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	25 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	8
Number of Gates	-
Number of I/O	-
Operating Temperature	0°C ~ 75°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/gal16v8d-25lp

Product Line	Ordering Part Number	Product Status	Reference PCN
GAL16V8D (Cont'd)	GAL16V8D-7LJ	Discontinued	PCN#13-10
	GAL16V8D-7LJN		
	GAL16V8D-10LJ		
	GAL16V8D-10LJN		
	GAL16V8D-15LJ		
	GAL16V8D-15LJN		
	GAL16V8D-25LJ		
	GAL16V8D-25LJN		
	GAL16V8D-7LJI		PCN#09-10
	GAL16V8D-7LJNI		
	GAL16V8D-10LJI		PCN#13-10
	GAL16V8D-10LJNI		
	GAL16V8D-15LJI		
	GAL16V8D-15LJNI		
	GAL16V8D-25LJI		
	GAL16V8D-25LJNI		
	GAL16V8D-10QJ		
	GAL16V8D-10QJN		
	GAL16V8D-15QJ		
	GAL16V8D-15QJN		
	GAL16V8D-25QJ		
	GAL16V8D-25QJN		
	GAL16V8D-20QJI		
	GAL16V8D-20QJNI		
	GAL16V8D-25QJI		
	GAL16V8D-25QJNI		
	GAL16V8D-7LS		PCN#06-07
	GAL16V8D-10LS		
	GAL16V8D-15LS		
	GAL16V8D-25LS		

Lead-Free Package Options Available!

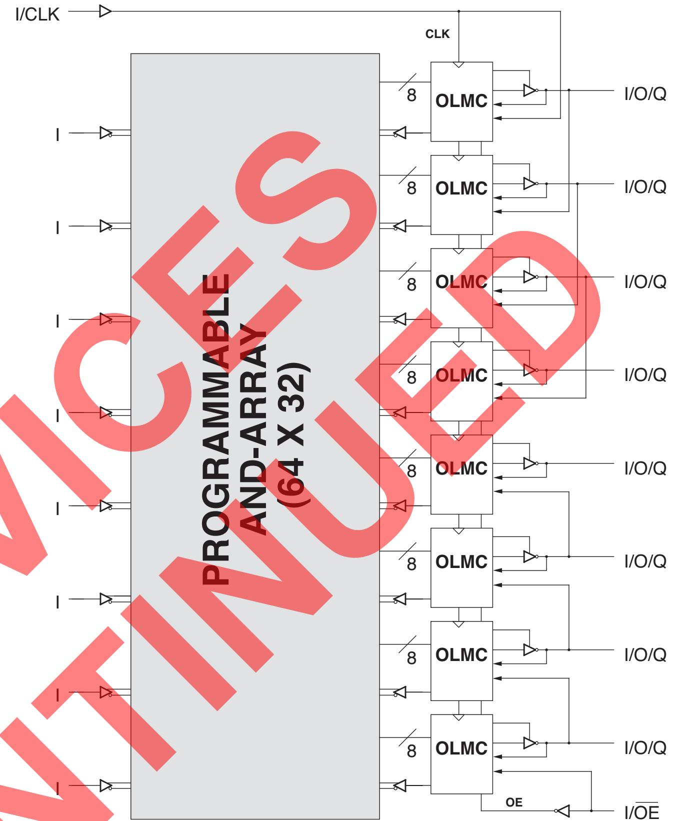
GAL16V8

High Performance E²CMOS PLD
Generic Array Logic™

Features

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 3.5 ns Maximum Propagation Delay
  - Fmax = 250 MHz
  - 3.0 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- 50% to 75% REDUCTION IN POWER FROM BIPOLAR
  - 75mA Typ Icc on Low Power Device
  - 45mA Typ Icc on Quarter Power Device
- ACTIVE PULL-UPS ON ALL PINS
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION
- LEAD-FREE PACKAGE OPTIONS

Functional Block Diagram



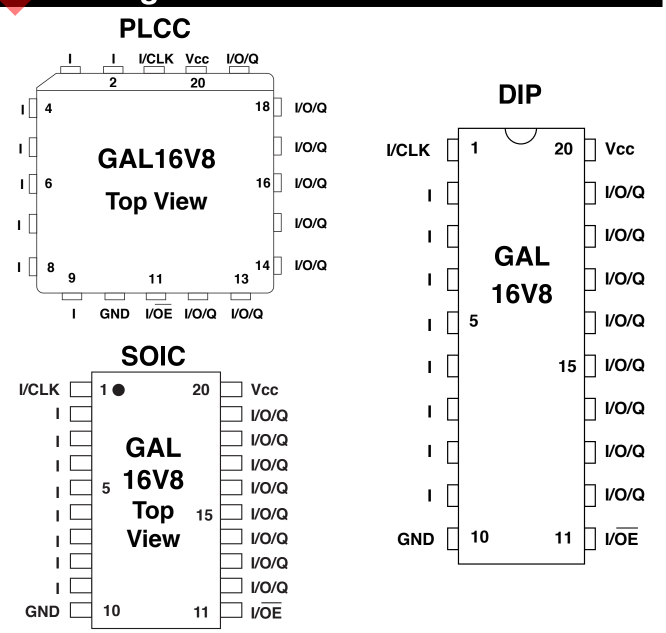
Description

The GAL16V8, at 3.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 are the PAL architectures listed in the table of the macrocell description section. GAL16V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

August 2006

GAL16V8 Ordering Information

Conventional Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
3.5	2.5	3.0	115	GAL16V8D-3LJ[1]	20-Lead PLCC
5	3	4	115	GAL16V8C-5LP[1]	20-Pin Plastic DIP
			115	GAL16V8D-5LJ	20-Lead PLCC
7.5	7	5	115	GAL16V8D-7LP	20-Pin Plastic DIP
			115	GAL16V8C-7LP[1]	20-Pin Plastic DIP
			115	GAL16V8D-7LJ	20-Lead PLCC
			115	GAL16V8D-7LS[1]	20-Pin SOIC
10	10	7	55	GAL16V8D-10QP	20-Pin Plastic DIP
			55	GAL16V8D-10QJ	20-Lead PLCC
			115	GAL16V8D-10LP	20-Pin Plastic DIP
			115	GAL16V8D-10LJ	20-Lead PLCC
			115	GAL16V8D-10LS[1]	20-Pin SOIC
15	12	10	55	GAL16V8D-15QP	20-Pin Plastic DIP
			55	GAL16V8D-15QJ	20-Lead PLCC
			90	GAL16V8D-15LP	20-Pin Plastic DIP
			90	GAL16V8D-15LJ	20-Lead PLCC
			90	GAL16V8D-15LS[1]	20-Pin SOIC
25	15	12	55	GAL16V8D-25QP	20-Pin Plastic DIP
			55	GAL16V8D-25QJ	20-Lead PLCC
			90	GAL16V8D-25LP	20-Pin Plastic DIP
			90	GAL16V8D-25LJ	20-Lead PLCC
			90	GAL16V8D-25LS[1]	20-Pin SOIC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	130	GAL16V8D-7LPI	20-Pin Plastic DIP
			130	GAL16V8D-7LJI	20-Lead PLCC
10	10	7	130	GAL16V8D-10LPI	20-Pin Plastic DIP
			130	GAL16V8D-10LJI	20-Lead PLCC
15	12	10	130	GAL16V8D-15LPI	20-Pin Plastic DIP
			130	GAL16V8D-15LJI	20-Lead PLCC
20	13	11	65	GAL16V8D-20QPI	20-Pin Plastic DIP
			65	GAL16V8D-20QJI	20-Lead PLCC
25	15	12	65	GAL16V8D-25QPI	20-Pin Plastic DIP
			65	GAL16V8D-25QJI	20-Lead PLCC
			130	GAL16V8D-25LPI	20-Pin Plastic DIP
			130	GAL16V8D-25LJI	20-Lead PLCC

Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

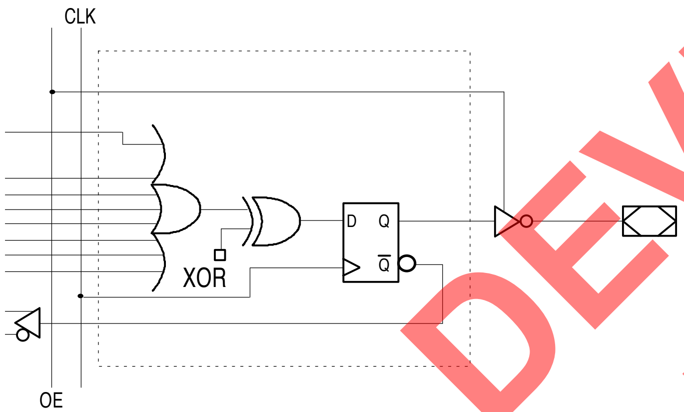
Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode.

Dedicated input or output functions can be implemented as subsets of the I/O function.

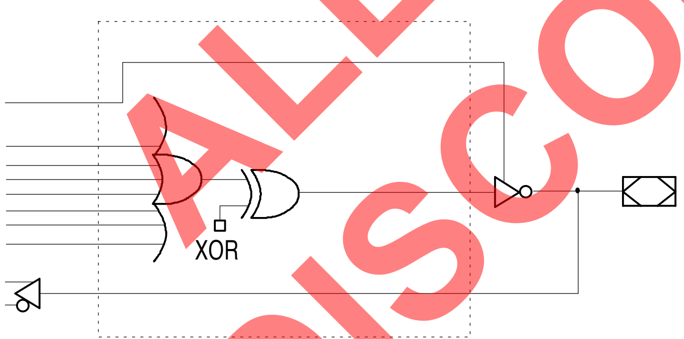
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



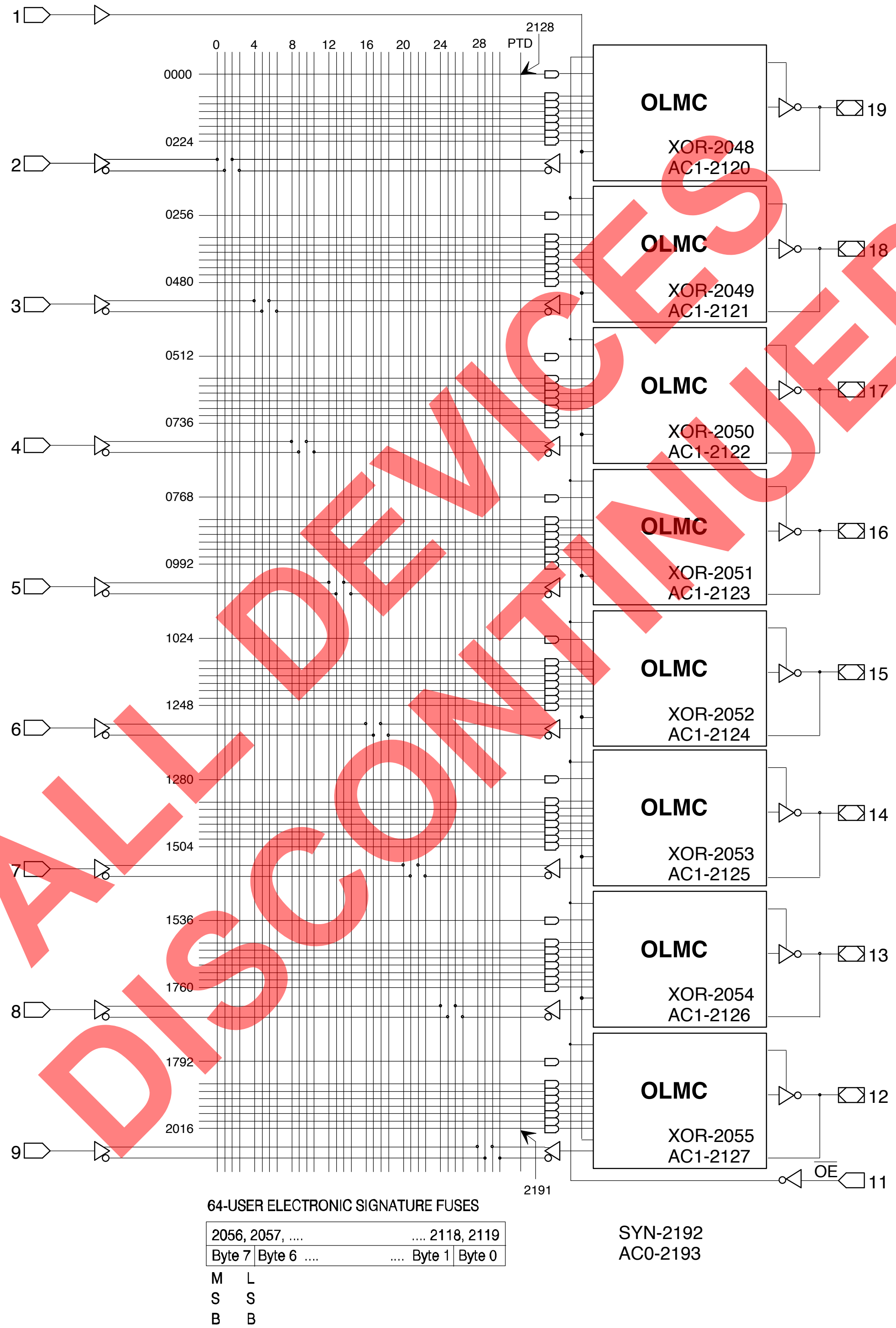
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram

DIP & PLCC Package Pinouts



Complex Mode

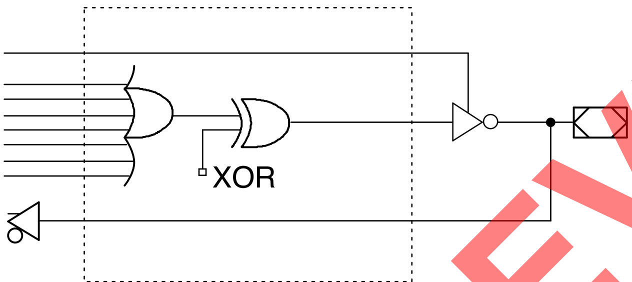
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

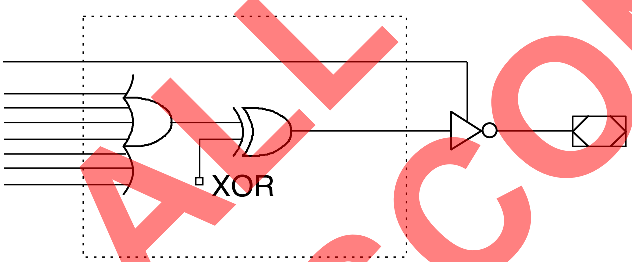
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 13 through Pin 18 are configured to this function.



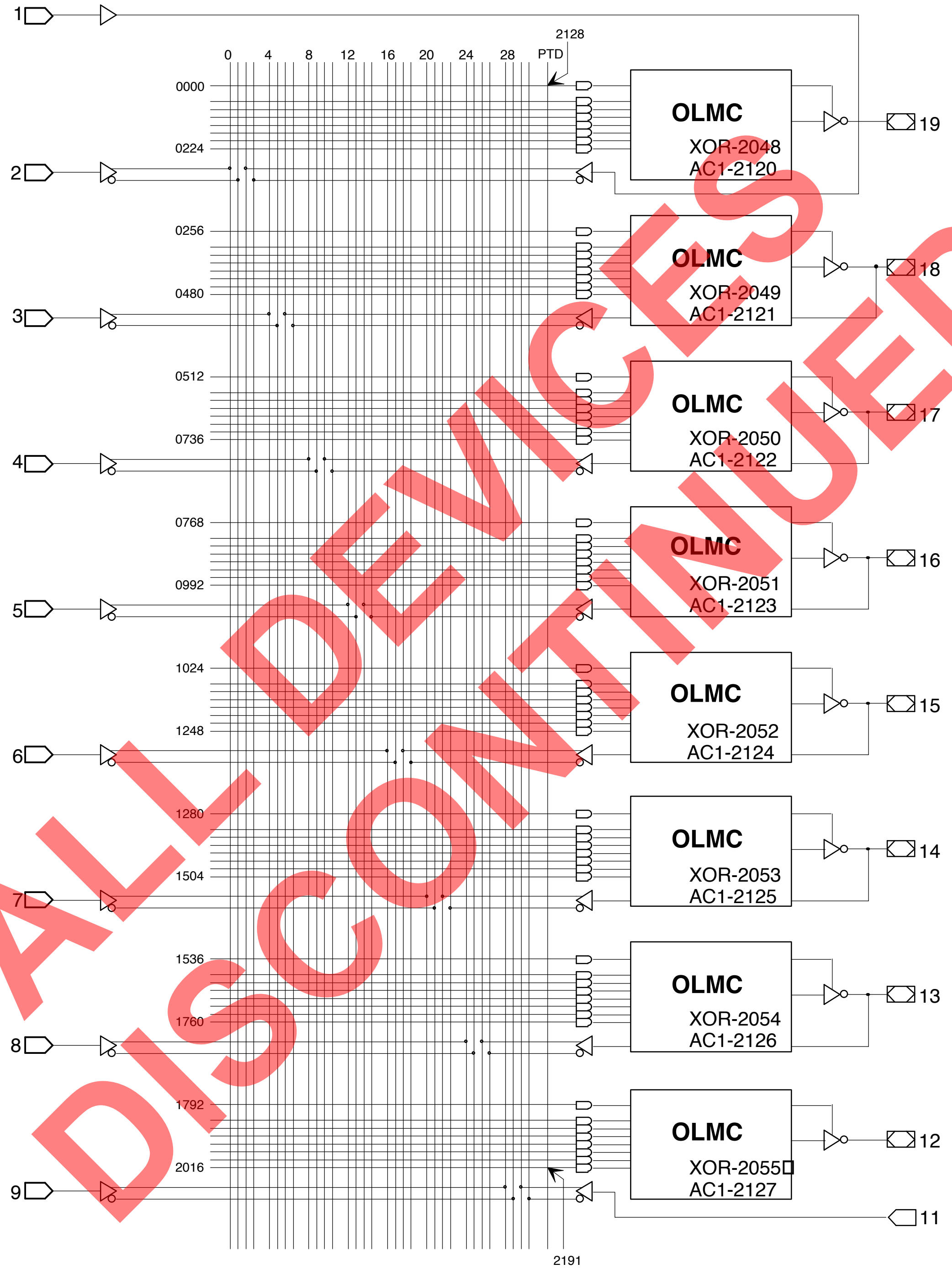
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Complex Mode Logic Diagram

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...			.... 2118, 2119
Byte 7	Byte 6	.... Byte 1	Byte 0

M L
S S
B B

SYN-2192
AC0-2193

Absolute Maximum Ratings(1)

Supply voltage V_{CC} .... –0.5 to +7V
Input voltage applied .... –2.5 to V_{CC} +1.0V
Off-state output voltage applied .... –2.5 to V_{CC} +1.0V
Storage Temperature .... –65 to 150°C
Ambient Temperature with
Power Applied .... –55 to 125°C

1.Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) .... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground .... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) .... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground .... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
VIL	Input Low Voltage		Vss – 0.5	—	0.8	V
VIH	Input High Voltage		2.0	—	Vcc+1	V
IIL[1]	Input or I/O Low Leakage Current	0V ≤ VIN ≤ VIL (MAX.)	—	—	–100	μA
IIH	Input or I/O High Leakage Current	3.5V ≤ VIN ≤ VCC	—	—	10	μA
VOL	Output Low Voltage	IOL = MAX. Vin = VIL or VIH	—	—	0.5	V
VOH	Output High Voltage	IOH = MAX. Vin = VIL or VIH	2.4	—	—	V
IOL	Low Level Output Current	L-3/-5 & -7 (Ind. PLCC)	—	—	16	mA
		L-7 (Except Ind. PLCC)/-10/-15/-25 Q-10/-15/-20/-25	—	—	24	mA
IOH	High Level Output Current		—	—	–3.2	mA
IOS[2]	Output Short Circuit Current	VCC = 5V VOUT = 0.5V T_A= 25°C	–30	—	–150	mA

COMMERCIAL

ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15MHz Outputs Open	L -3/-5/-7/-10	—	75	115	mA
			L-15/-25	—	75	90	mA
			Q-10/-15/-25	—	45	55	mA

INDUSTRIAL

ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15MHz Outputs Open	L -7/-10/-15/-25	—	75	130	mA
			Q -20/-25	—	45	65	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	COM -3		COM -5		COM / IND -7		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Comb. Output	1	3.5	1	5	1	7.5	ns
t_{co}	A	Clock to Output Delay	1	3	1	4	1	5	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	2.5	—	3	—	3	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	2.5	—	3	—	5	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
f_{max}[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	182	—	142.8	—	100	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	200	—	166	—	125	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	166	—	125	—	MHz
t_{wh}	—	Clock Pulse Duration, High	2[4]	—	3[4]	—	4	—	ns
t_{wl}	—	Clock Pulse Duration, Low	2[4]	—	3[4]	—	4	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	4.5	1	6	1	9	ns
	B	$\overline{OE}$ to Output Enabled	—	4.5	1	6	1	6	ns
t_{dis}	C	Input or I/O to Output Disabled	—	4.5	1	5	1	9	ns
	C	$\overline{OE}$ to Output Disabled	—	4.5	1	5	1	6	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section. Characterized but not 100% tested.
4) Characterized but not 100% tested.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION	COM / IND		COM / IND		IND		COM / IND		UNITS
			-10		-15		-20		-25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Comb. Output	3	10	3	15	3	20	3	25	ns
tco	A	Clock to Output Delay	2	7	2	10	2	11	2	12	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	8	—	9	—	10	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	7.5	—	12	—	13	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	66.7	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	71.4	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	50	—	41.6	—	MHz
twh	—	Clock Pulse Duration, High	6	—	8	—	10	—	12	—	ns
twl	—	Clock Pulse Duration, Low	6	—	8	—	10	—	12	—	ns
ten	B	Input or I/O to Output Enabled	1	10	—	15	—	18	—	20	ns
	B	$\overline{OE}$ to Output Enabled	1	10	—	15	—	18	—	20	ns
tdis	C	Input or I/O to Output Disabled	1	10	—	15	—	18	—	20	ns
	C	$\overline{OE}$ to Output Disabled	1	10	—	15	—	18	—	20	ns

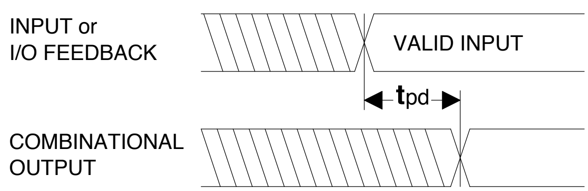
1) Refer to **Switching Test Conditions** section.
2) Calculated from **fmax** with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section. Characterized but not 100% tested.

Capacitance (T_A = 25°C, f = 1.0 MHz)

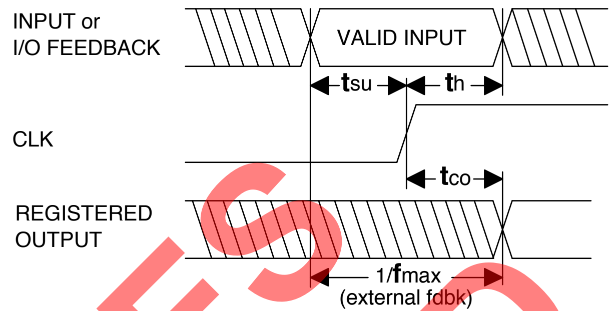
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

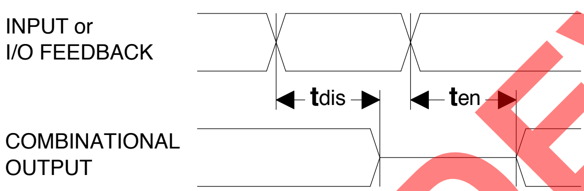
Switching Waveforms



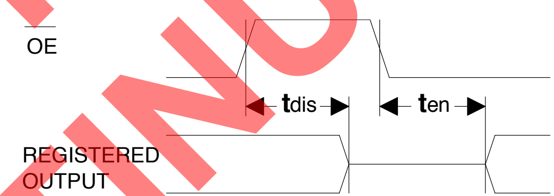
Combinatorial Output



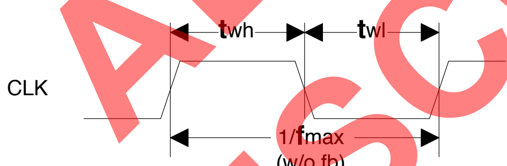
Registered Output



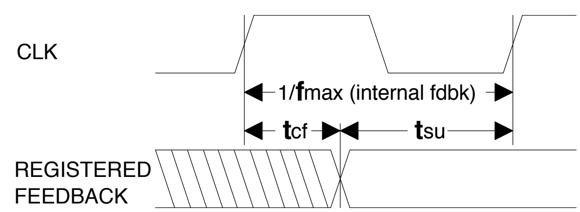
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

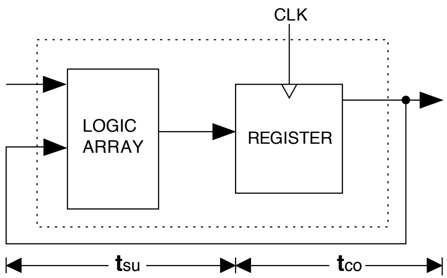


Clock Width



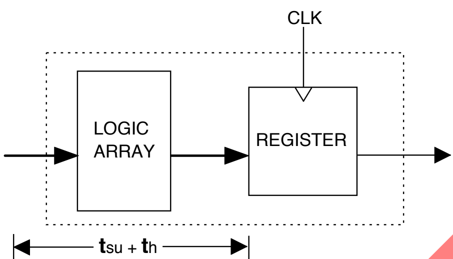
fmax with Feedback

fmax Descriptions



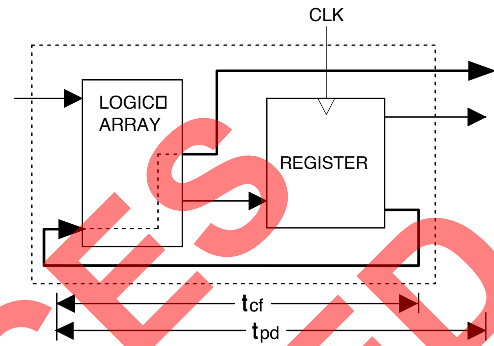
fmax with External Feedback 1/(tsu+tco)

Note: **f**max with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: **f**max with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: **t**cf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

Switching Test Conditions

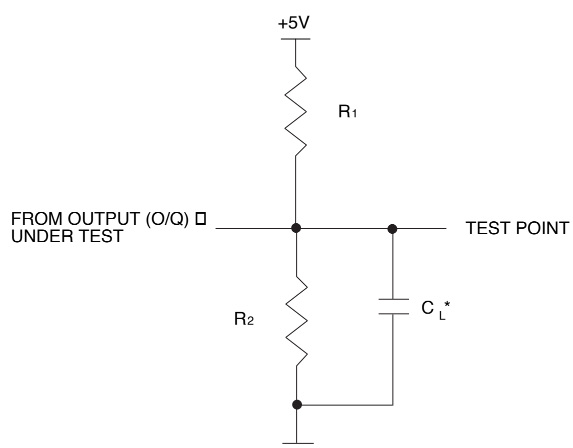
Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL16V8D-10 (and slower)	2 – 3ns 10% – 90%
	GAL16V8D-3/-5/-7	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See figure at right

3-state levels are measured 0.5V from steady-state active level.

Table 2-0003/16V8

GAL16V8D (except -3) Output Load Conditions (see figure above)

Test Condition		R_1	R_2	C_L
A		200Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

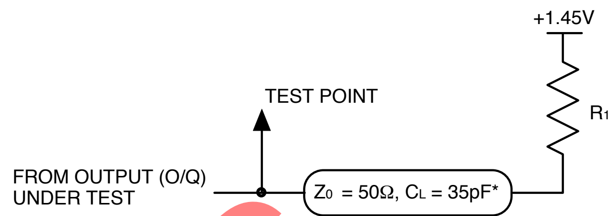


*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Switching Test Conditions (Continued)

GAL16V8D-3 Output Load Conditions (see figure at right)

Test Condition		R_1	C_L
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



*C_L includes test fixture and probe capacitance.

Electronic Signature

An electronic signature is provided in every GAL16V8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

Security Cell

A security cell is provided in the GAL16V8 devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Latch-Up Protection

GAL16V8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

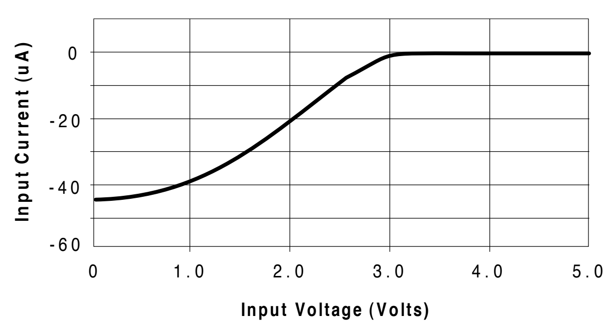
GAL16V8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

Input Buffers

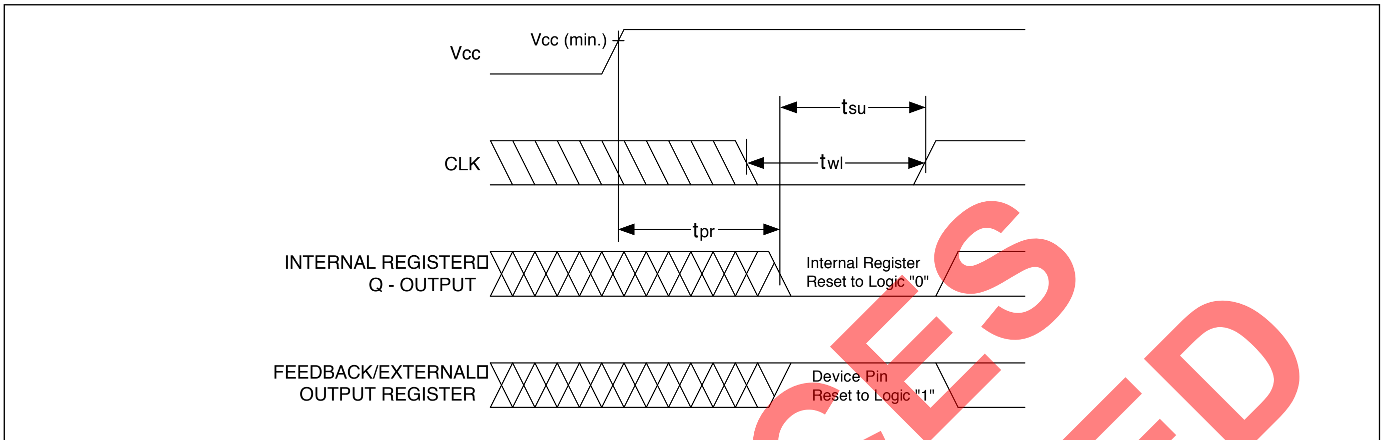
GAL16V8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL16V8 input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic

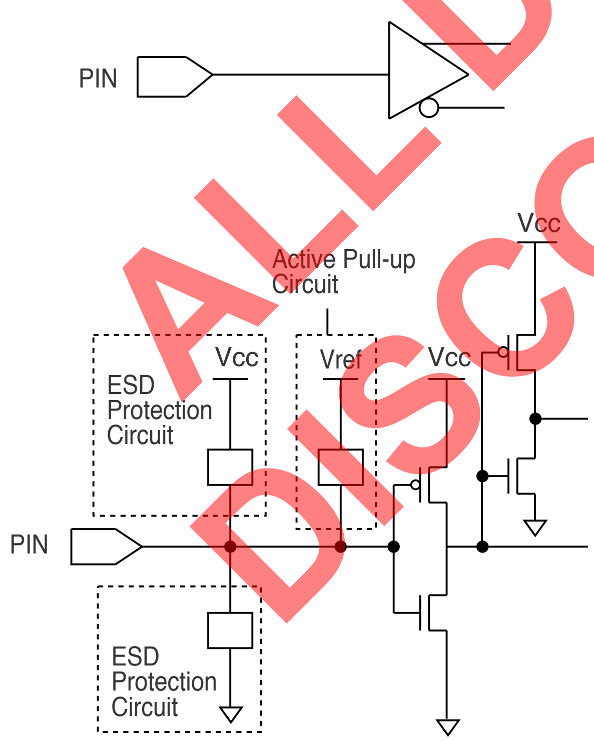


Power-Up Reset



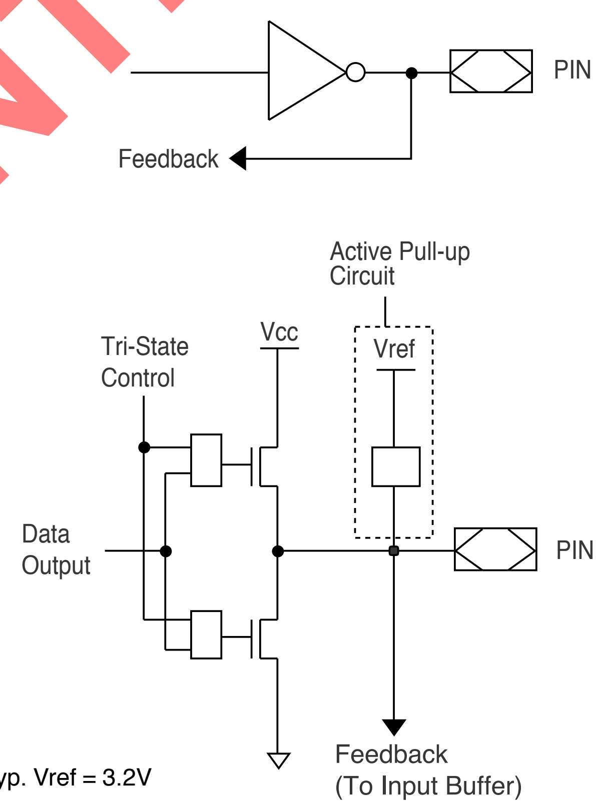
Circuitry within the GAL16V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 1μs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



Typ. Vref = 3.2V

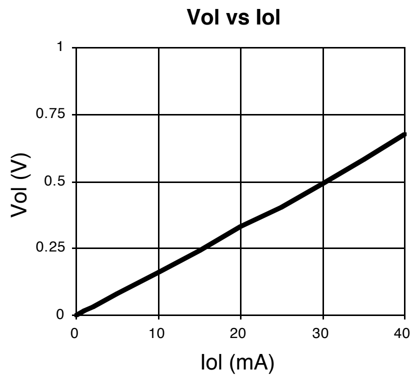
Typical Input

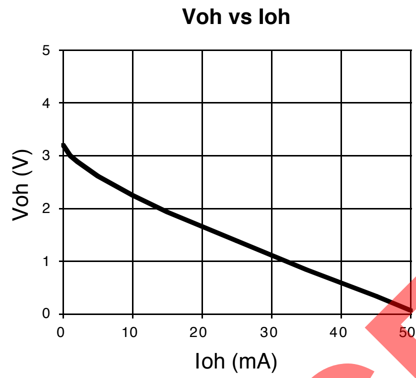


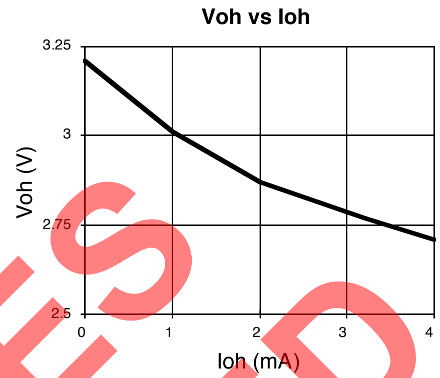
Typ. Vref = 3.2V

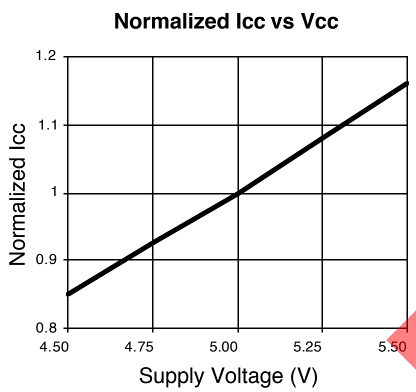
Typical Output

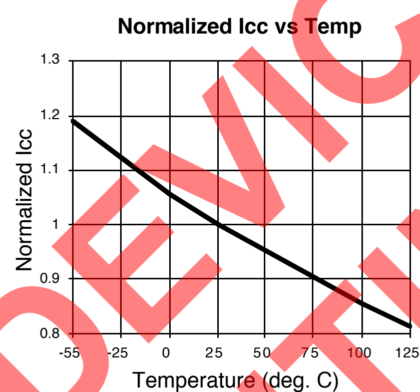
GAL16V8D-3/-5/-7 (IND PLCC): Typical AC and DC Characteristic Diagrams

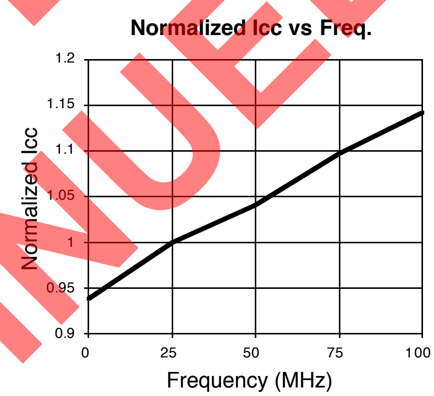


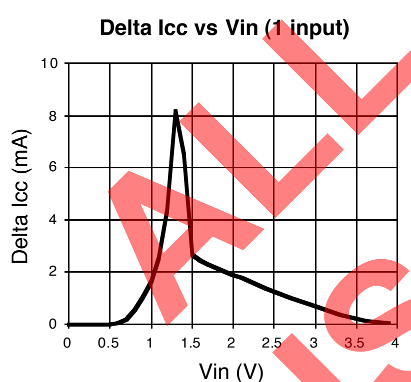


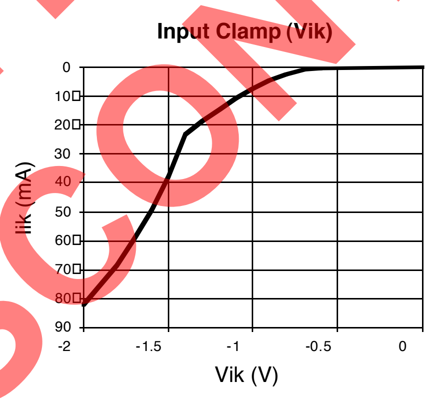






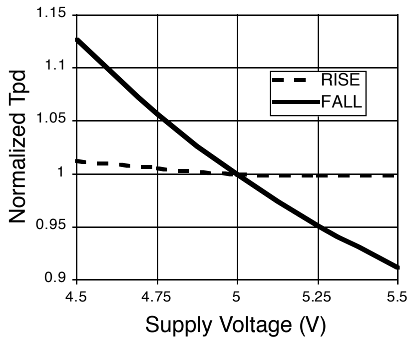




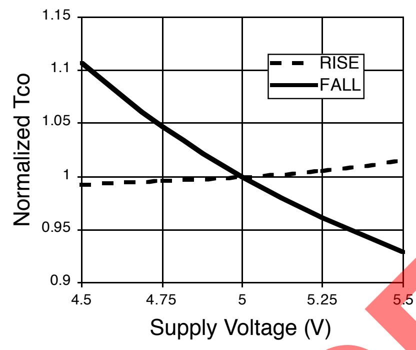


GAL16V8D-7 (Except IND PLCC)/-10L: Typical AC and DC Characteristic Diagrams

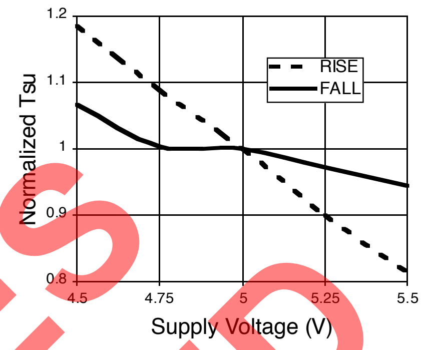
Normalized Tpd vs Vcc



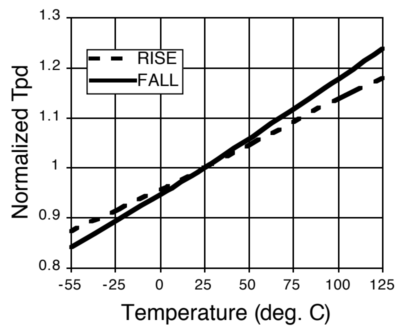
Normalized Tco vs Vcc



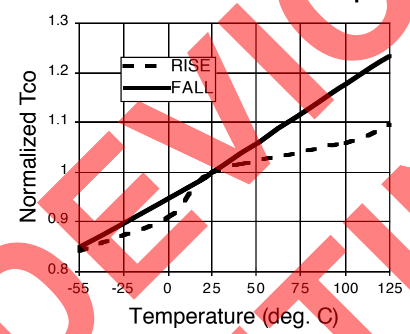
Normalized Tsu vs Vcc



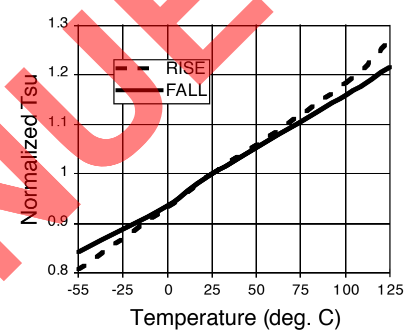
Normalized Tpd vs Temp



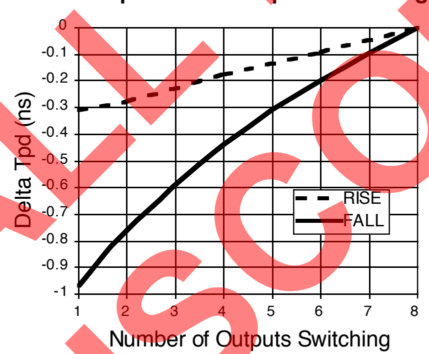
Normalized Tco vs Temp



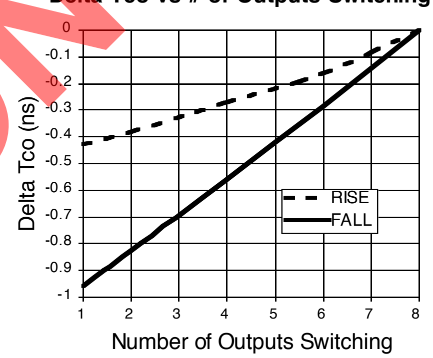
Normalized Tsu vs Temp



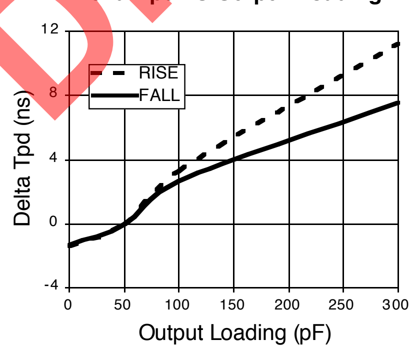
Delta Tpd vs # of Outputs Switching



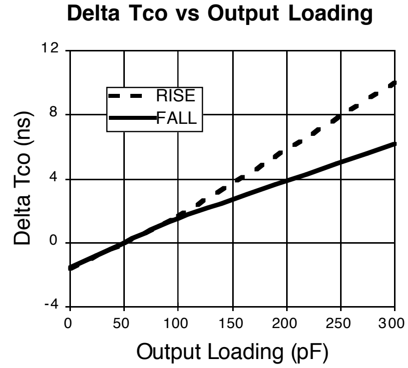
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

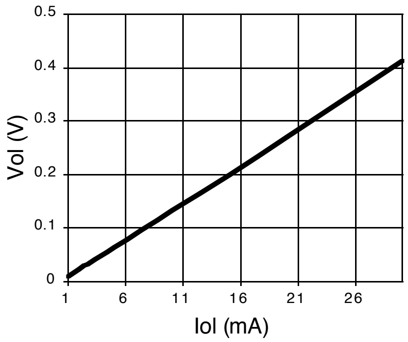


Delta Tco vs Output Loading

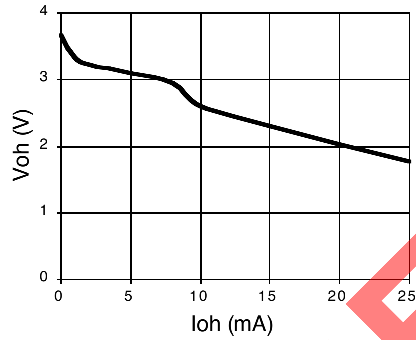


GAL16V8D-7 (Except IND PLCC)/-10L: Typical AC and DC Characteristic Diagrams

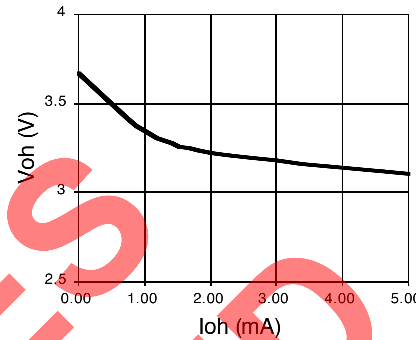
Vol vs Iol



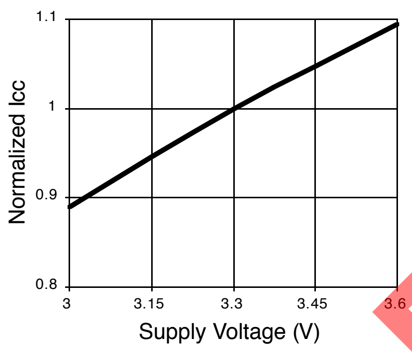
Voh vs Ioh



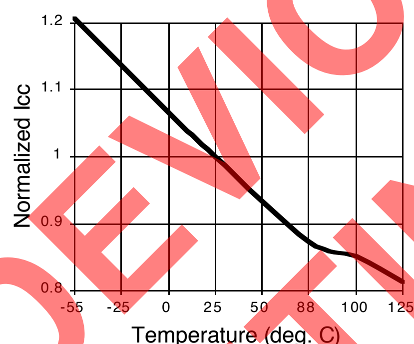
Voh vs Ioh



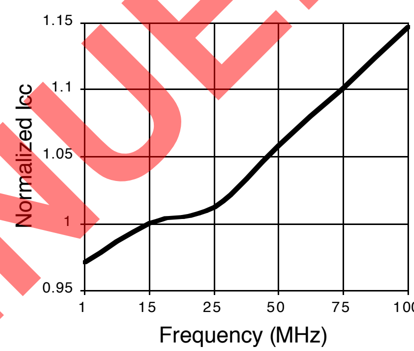
Normalized Icc vs Vcc



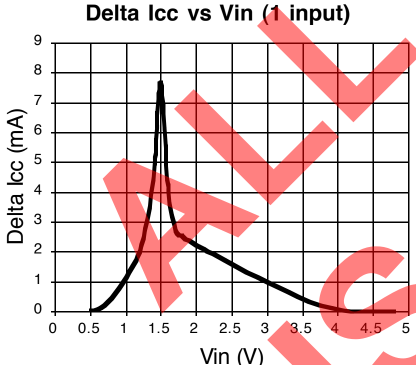
Normalized Icc vs Temp



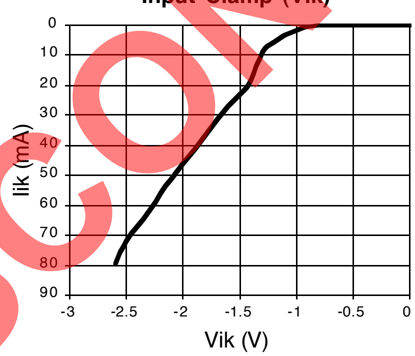
Normalized Icc vs Freq



Delta Icc vs Vin (1 input)

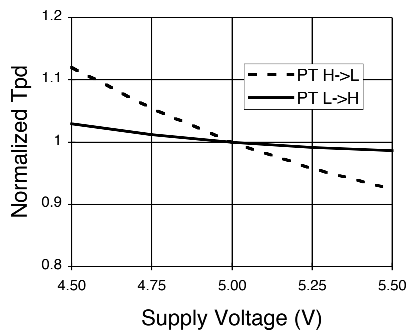


Input Clamp (Vik)

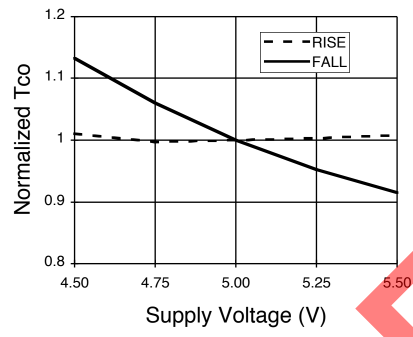


GAL16V8D-10Q (and Slower): Typical AC and DC Characteristic Diagrams

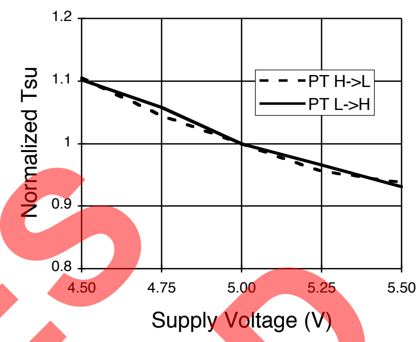
Normalized Tpd vs Vcc



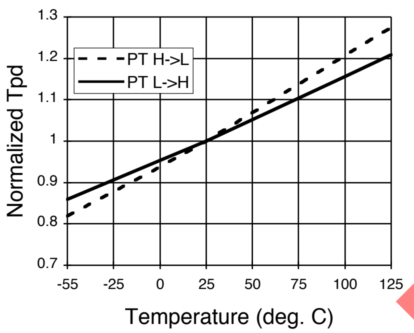
Normalized Tco vs Vcc



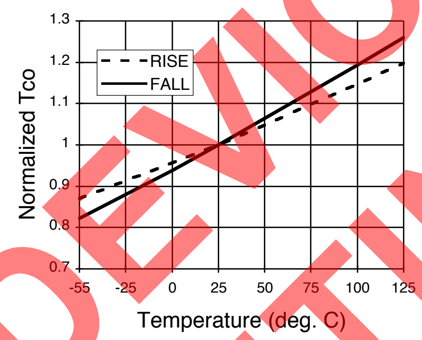
Normalized Tsu vs Vcc



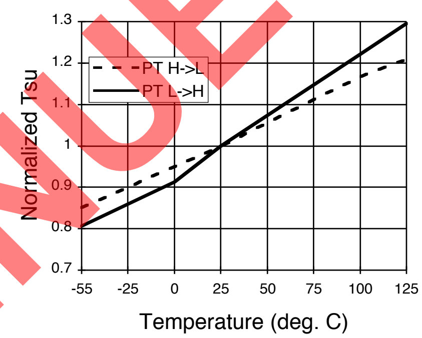
Normalized Tpd vs Temp



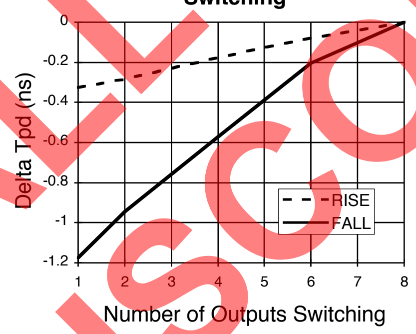
Normalized Tco vs Temp



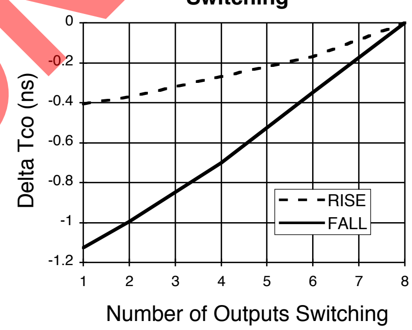
Normalized Tsu vs Temp



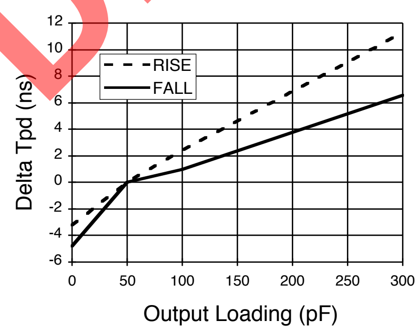
Delta Tpd vs # of Outputs Switching



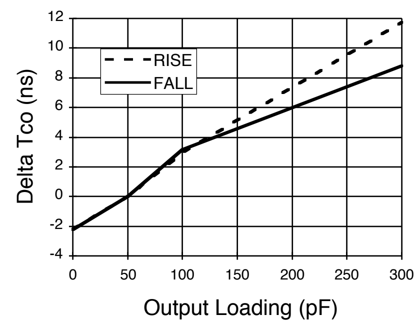
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

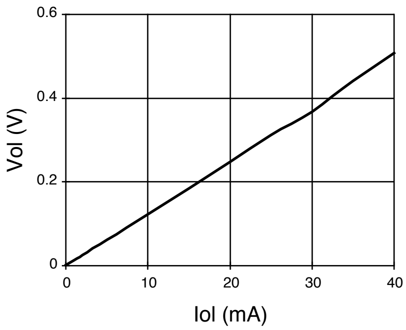


Delta Tco vs Output Loading

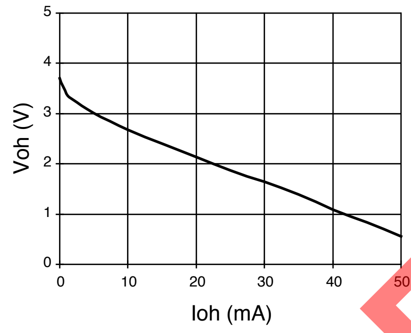


GAL16V8D-10Q (and Slower): Typical AC and DC Characteristic Diagrams

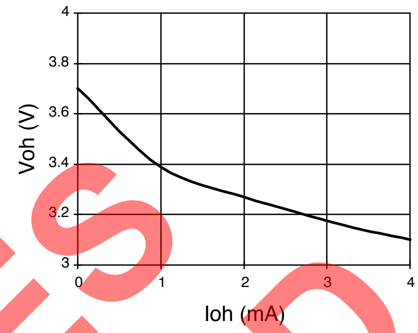
Vol vs Iol



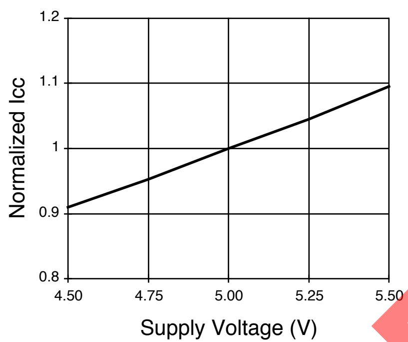
Voh vs Ioh



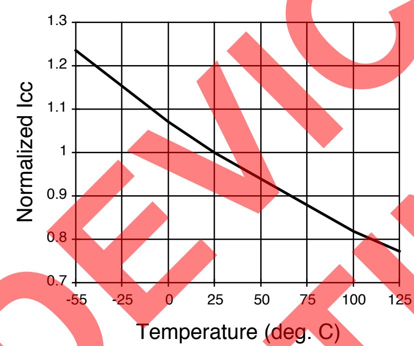
Voh vs Ioh



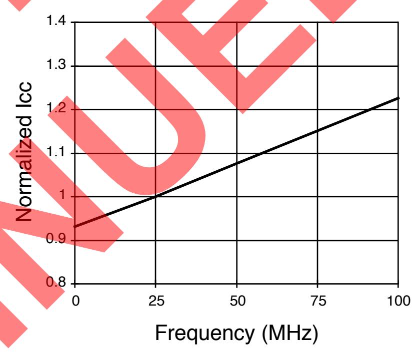
Normalized Icc vs Vcc



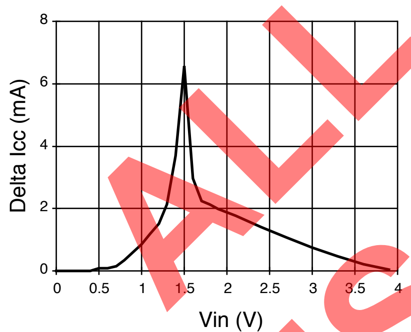
Normalized Icc vs Temp



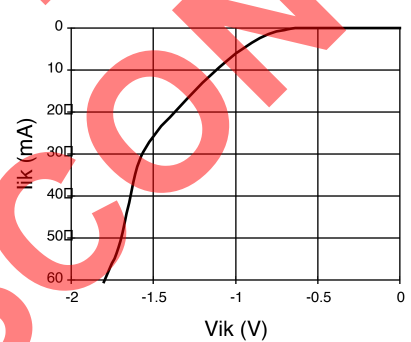
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Revision History

Date	Version	Change Summary
-	16v8_10	Previous Lattice release.
August 2006	16v8_11	Updated for lead-free package options.