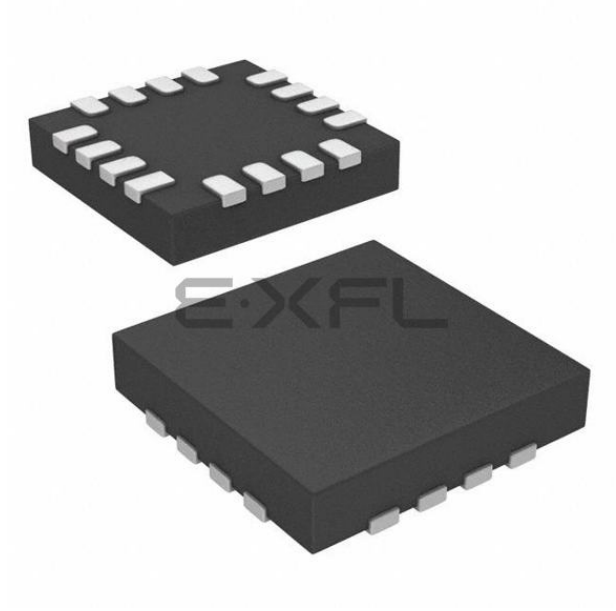

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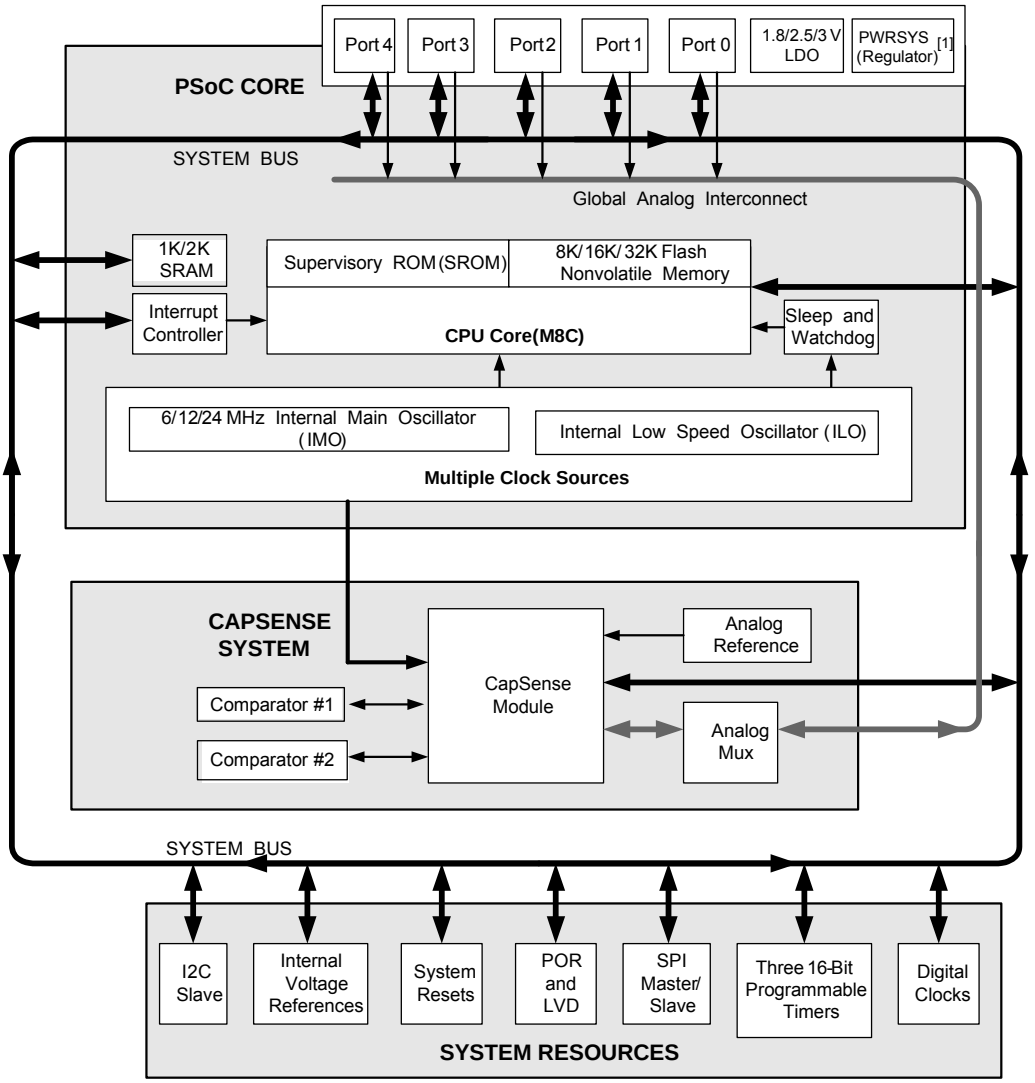
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (8kB)
Controller Series	CY8C20xx7/S
RAM Size	1K x 8
Interface	I²C, SPI
Number of I/O	14
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20237-24lkxi

Logic Block Diagram



Note
1. Internal voltage regulator for internal circuitry

PSoC® Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional MCU-based system components with one low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the "Logic Block Diagram" on page 2, consists of three main areas:

- The core
- CapSense analog system
- System resources

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20x37/47/67/S PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 34 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-million instructions per second (MIPS), 8-bit Harvard-architecture microprocessor.

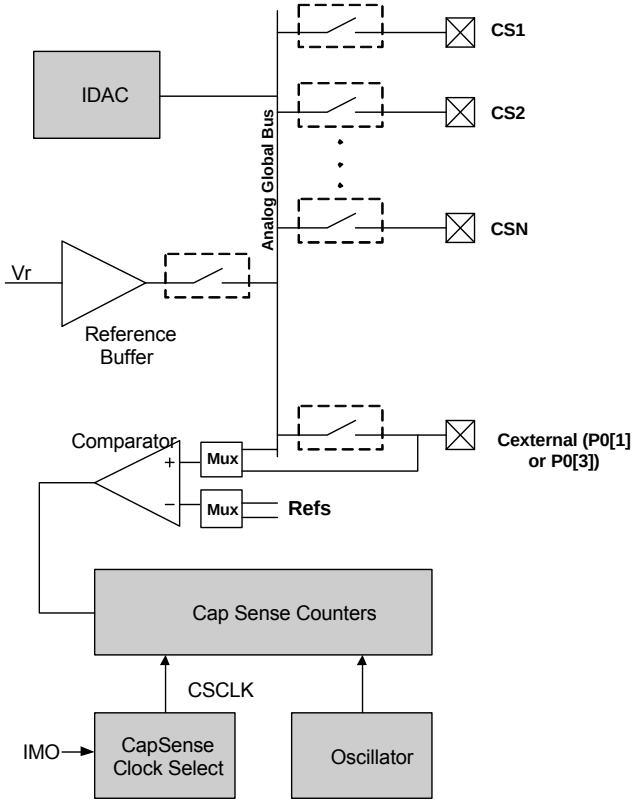
CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1 V or 1.2 V analog reference, which together support capacitive sensing of up to 31 inputs[2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple ports.

SmartSense™ Auto-tuning

SmartSense auto-tuning is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters of each sensor during run time. SmartSense auto-tuning allows engineers to go from prototyping to mass production without retuning for manufacturing variations in PCB and/or overlay material properties.

Figure 1. CapSense System Block Diagram



Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Note
2. 34 GPIOs = 31 pins for capacitive sensing+2 pins for I^2C + 1 pin for modulator capacitor.

Additional System Resources

System resources provide additional capability, such as configurable I^2C slave, SPI master/slave communication interface, three 16-bit programmable timers, various system resets supported by the M8C low voltage detection and power-on reset. The merits of each system resource are listed here:

- The I^2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I^2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I^2C enhanced slave interface appears as a 32-byte RAM buffer to the external I^2C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For more details, refer to the I2CSBUF User Module datasheet.
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20x37/47/67/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

Application Notes/Design Guides

Application notes and design guides are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/gocapsense. Select Application Notes under the Related Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. See “Development Kits” on page 31.

Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

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Pinouts

The CY8C20x37/47/67/S PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

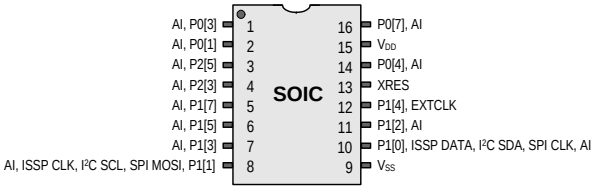
16-pin SOIC (10 Sensing Inputs)

Table 1. Pin Definitions – CY8C20237-24SXI, CY8C20247/S-24SXI [3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[3]	Integrating Input
2	I/O	I	P0[1]	Integrating Input
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P1[7]	I2C SCL, SPI SS
6	I/O	I	P1[5]	I2C SDA, SPI MISO
7	I/O	I	P1[3]	
8	I/O	I	P1[1]	ISSP CLK[4], I2C SCL, SPI MOSI
9	Power		V_{SS}	Ground connection[7]
10	I/O	I	P1[0]	ISSP DATA[4], I2C SDA, SPI CLK[5]
11	I/O	I	P1[2]	Driven Shield Output (optional)
12	I/O	I	P1[4]	Optional external clock (EXTCLK)
13	INPUT		XRES	Active high external reset with internal pull-down[6]
14	I/O	I	P0[4]	
15	Power		V_{DD}	Supply voltage
16	I/O	I	P0[7]	

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 2. CY8C20237-24SXI, CY8C20247/S-24SXI Device



Notes
3. 13 GPIOs = 10 pins for capacitive sensing+2 pins for I^2C + 1 pin for modulator capacitor.
4. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
5. Alternate SPI clock.
6. The internal pull down is 5KOhm.
7. All VSS pins should be brought out to one common GND plane.

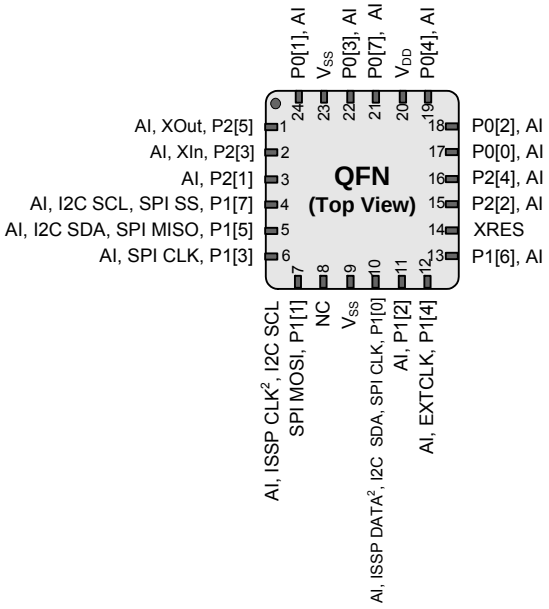
24-pin QFN (16 Sensing Inputs)[14]

Table 3. Pin Definitions – CY8C20337, CY8C20347/S [15]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I^2C SCL, SPI SS
5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[16], I^2C SCL, SPI MOSI
8			NC	No connection
9	Power		V_{SS}	Ground connection[19]
10	IOHR	I	P1[0]	ISSP DATA[16], I^2C SDA, SPI CLK[17]
11	IOHR	I	P1[2]	Driven Shield Output (optional)
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down[18]
15	I/O	I	P2[2]	Driven Shield Output (optional)
16	I/O	I	P2[4]	Driven Shield Output (optional)
17	IOH	I	P0[0]	Driven Shield Output (optional)
18	IOH	I	P0[2]	Driven Shield Output (optional)
19	IOH	I	P0[4]	
20	Power		V_{DD}	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[3]	Integrating input
23	Power		V_{SS}	Ground connection[19]
24	IOH	I	P0[1]	Integrating input
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 4. CY8C20337, CY8C20347/S Device



Notes

14. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. 19 GPIOs = 16 pins for capacitive sensing+2 pins for I^2C + 1 pin for modulator capacitor.
16. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter issues.
17. Alternate SPI clock.
18. The internal pull down is 5KOhm.
19. All VSS pins should be brought out to one common GND plane.

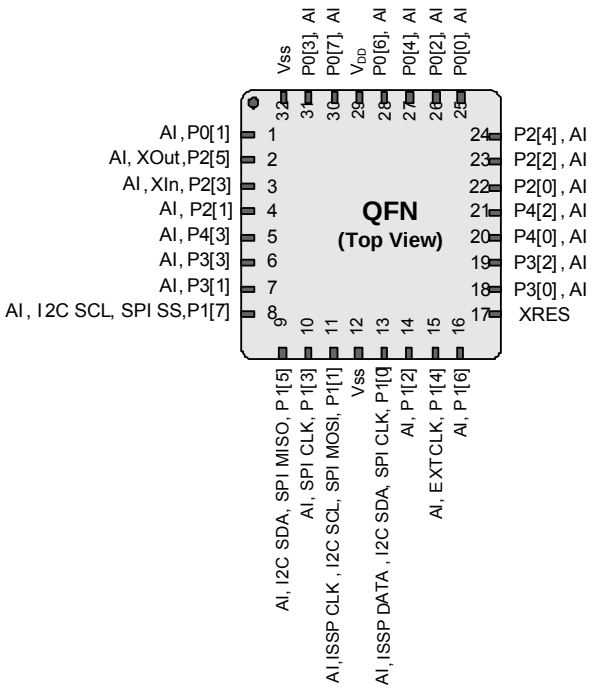
32-pin QFN (25 Sensing Inputs)[25]

Table 5. Pin Definitions – CY8C20437, CY8C20447/S, CY8C20467/S [26]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[5]	Crystal output (XOut)
3	I/O	I	P2[3]	Crystal input (XIn)
4	I/O	I	P2[1]	
5	I/O	I	P4[3]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I^2C SCL, SPI SS
9	IOHR	I	P1[5]	I^2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK[27], I^2C SCL, SPI MOSI.
12	Power		V_{SS}	Ground connection[30]
13	IOHR	I	P1[0]	ISSP DATA[27], I^2C SDA, SPI CLK[28]
14	IOHR	I	P1[2]	Driven Shield Output (optional)
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down[29]
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P4[0]	
21	I/O	I	P4[2]	
22	I/O	I	P2[0]	
23	I/O	I	P2[2]	Driven Shield Output (optional)
24	I/O	I	P2[4]	Driven Shield Output (optional)
25	IOH	I	P0[0]	Driven Shield Output (optional)
26	IOH	I	P0[2]	Driven Shield Output (optional)
27	IOH	I	P0[4]	
28	IOH	I	P0[6]	
29	Power		V_{DD}	
30	IOH	I	P0[7]	
31	IOH	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[30]
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 6. CY8C20437, CY8C20447/S, CY8C20467/S Device



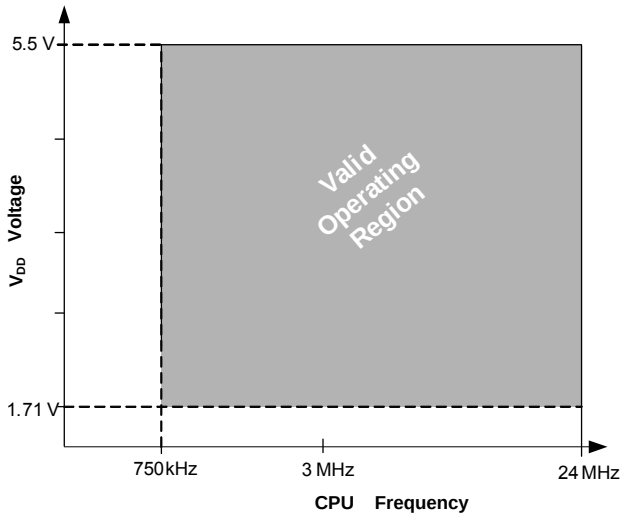
Notes

25. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
26. 28 GPIOs = 25 pins for capacitive sensing+2 pins for I^2C + 1 pin for modulator capacitor.
27. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter issues.
28. Alternate SPI clock.
29. The internal pull down is 5KOhm.
30. All VSS pins should be brought out to one common GND plane.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x37/47/67/S PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at http://www.cypress.com/psoc.

Figure 8. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	+25	+125	°C
V_{DD}	Supply voltage relative to V_{SS}	–	–0.5	–	+6.0	V
V_{IO}	DC input voltage	–	V_{SS} – 0.5	–	V_{DD} + 0.5	V
V_{IOZ}	DC voltage applied to tristate	–	V_{SS} – 0.5	–	V_{DD} + 0.5	V
I_{MIO}	Maximum current into any port pin	–	–25	–	+50	mA
ESD	Electro static discharge voltage	Human body model ESD	2000	–	–	V
LU	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature	–	–40	–	+85	°C
T_C	Commercial temperature range	–	0		70	°C
T_J	Operational die temperature	The temperature rise from ambient to junction is package specific. See the Thermal Impedances on page 30. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

DC Chip-Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 9. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD} [37, 38, 39]	Supply voltage	See Table 14 on page 17.	1.71	–	5.50	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	2.88	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.71	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.16	1.80	mA
I_{SB0} [40, 41, 42, 43]	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.1	µA
I_{SB1} [40, 41, 42, 43]	Standby current with POR, LVD and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	µA
I_{SBI2C} [40, 41, 42, 43]	Standby current with I^2C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	µA

Notes

37. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
38. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that V_{DD} falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the Technical Reference Manual. In deep sleep/standby sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected and resets the device when V_{DD} goes lower than 1.1 V at edge rates slower than 1 V/ms.
39. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.
40. Errata: When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the “Errata” on page 37.
41. Errata: When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the “Errata” on page 37.
42. Errata: If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the “Errata” on page 37.
43. Errata: Device wakes up from sleep when an analog interrupt is trigger. For more information, see the “Errata” on page 37.

Table 12. 1.71 V to 2.4 V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Low output voltage	I_{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V_{IL}	Input low voltage	–	–	–	0.30 × V_{DD}	V
V_{IH}	Input high voltage	–	0.65 × V_{DD}	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

Table 13. GPIO Current Sink and Source Specifications

Supply Voltage	Mode	Port 0/1 per I/O (max)	Port 2/3/4 per I/O (max)	Total Current Even Pins (max)	Total Current Odd Pins (max)	Units
1.71–2.4	Sink	5	5	20	30	mA
	Source	2	0.5	10[45]		mA
2.4–3.0	Sink	10	10	30	30	mA
	Source	2	0.2	10[45]		mA
3.0–5.0	Sink	25	25	60	60	mA
	Source	5	1	20[45]		mA

DC Analog Mux Bus Specifications

Table 14 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus	–	–	–	800	Ω
R_{GND}	Resistance of initialization switch to V_{SS}	–	–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V_{DD}	0.2	–	1.8	V
I_{LPC}	LPC supply current	–	–	10	80	µA
V_{OSLPC}	LPC voltage offset	–	–	2.5	30	mV

Note
45. Total current (odd + even ports)

DC I²C Specifications

Table 20 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. DC I²C Specifications[50]

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{ILI2C}	Input low level	3.1 V ≤ V_{DD} ≤ 5.5 V	–	–	0.25 × V_{DD}	V
		2.5 V ≤ V_{DD} ≤ 3.0 V	–	–	0.3 × V_{DD}	V
		1.71 V ≤ V_{DD} ≤ 2.4 V	–	–	0.3 × V_{DD}	V
V_{IHI2C}	Input high level	1.71 V ≤ V_{DD} ≤ 5.5 V	0.65 × V_{DD}	–	V_{DD} + 0.7 V[51]	V

Shield Driver DC Specifications

Table 21 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. Shield Driver DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{Ref}	Reference buffer output	1.7 V ≤ V_{DD} ≤ 5.5 V	0.942	–	1.106	V
V_{RefHi}	Reference buffer output	1.7 V ≤ V_{DD} ≤ 5.5 V	1.104	–	1.296	V

DC IDAC Specifications

Table 22 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. DC IDAC Specifications (8-bit IDAC)

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–1	–	1	LSB	–
IDAC_DNL	Integral nonlinearity	–2	–	2	LSB	–
IDAC_Current	Range = 4x	138	–	169	µA	DAC setting = 127 dec
	Range = 8x	138	–	169	µA	DAC setting = 64 dec

Table 23. DC IDAC Specifications (7-bit IDAC)

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–1	–	1	LSB	–
IDAC_DNL	Integral nonlinearity	–2	–	2	LSB	–
IDAC_Current	Range = 4x	137	–	168	µA	DAC setting = 127 dec
	Range = 8x	138	–	169	µA	DAC setting = 64 dec

Notes

50. Errata: Pull-up resistors on I2C interface cannot be connected to a supply voltage that is more than 0.7 V higher than the CY8C20xx7/S power supply. For more information see item #6 in the "Errata" on page 37.
51. Errata: For more information see item #6 in the "Errata" on page 37.

AC Programming Specifications

Figure 10. AC Waveform

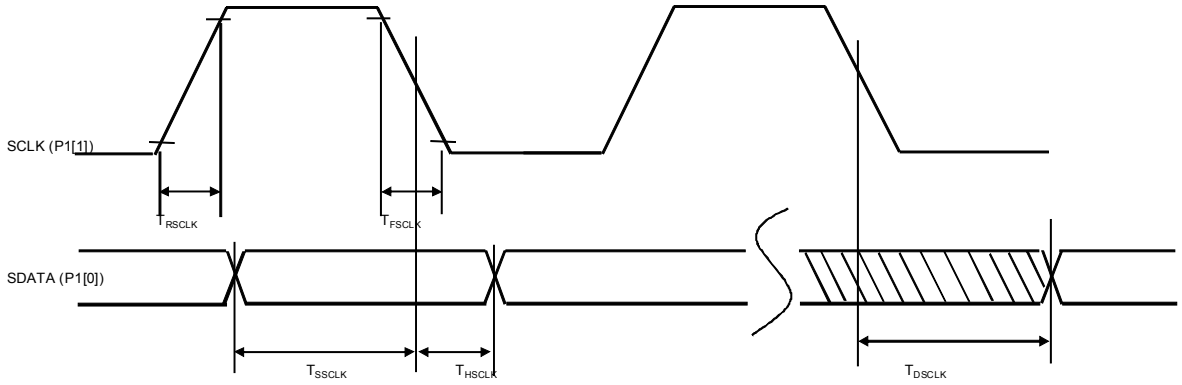


Table 28 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 28. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{RSCLK}	Rise time of SCLK	–	1	–	20	ns
t_{FSCLK}	Fall time of SCLK	–	1	–	20	ns
t_{SSCLK}	Data setup time to falling edge of SCLK	–	40	–	–	ns
t_{HSCLK}	Data hold time from falling edge of SCLK	–	40	–	–	ns
F_{SCLK}	Frequency of SCLK	–	0	–	8	MHz
t_{ERASEB}	Flash erase time (block)	–	–	–	18	ms
t_{WRITE}	Flash block write time	–	–	–	25	ms
t_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
t_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \le V_{DD} \le 3.6$	–	–	85	ns
t_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \le V_{DD} \le 3.0$	–	–	130	ns
t_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	µs
t_{XRES}	XRES pulse length	–	300	–	–	µs
$t_{VDDWAIT}$[54]	V_{DD} stable to wait-and-poll hold off	–	0.1	–	1	ms
$t_{VDDXRES}$[54]	V_{DD} stable to XRES assertion delay	–	14.27	–	–	ms
t_{POLL}	SDAT high pulse time	–	0.01	–	200	ms
t_{ACQ}[54]	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.	–	3.20	–	19.60	ms
$t_{XRESINI}$[54]	“Key window” time after an XRES event, based on 8 ILO clocks	–	98	–	615	µs

Note
54. Valid from 5 to 50 °C. See the spec, CY8C20X66, CY8C20X46, CY8C20X36, CY7C643XX, CY7C604XX, CY8CTST2XX, CY8CTMG2XX, CY8C20X67, CY8C20X47, CY8C20X37, Programming Spec for more details.

Table 31. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
t_{LOW}	SCLK low time	–	42	–	–	ns
t_{HIGH}	SCLK high time	–	42	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
t_{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Figure 14. SPI Slave Mode 0 and 2

SPI Slave, modes 0 and 2

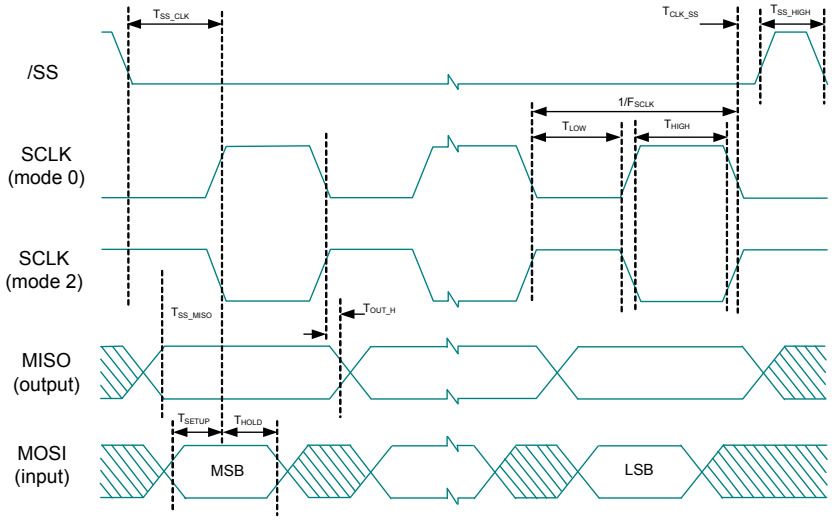
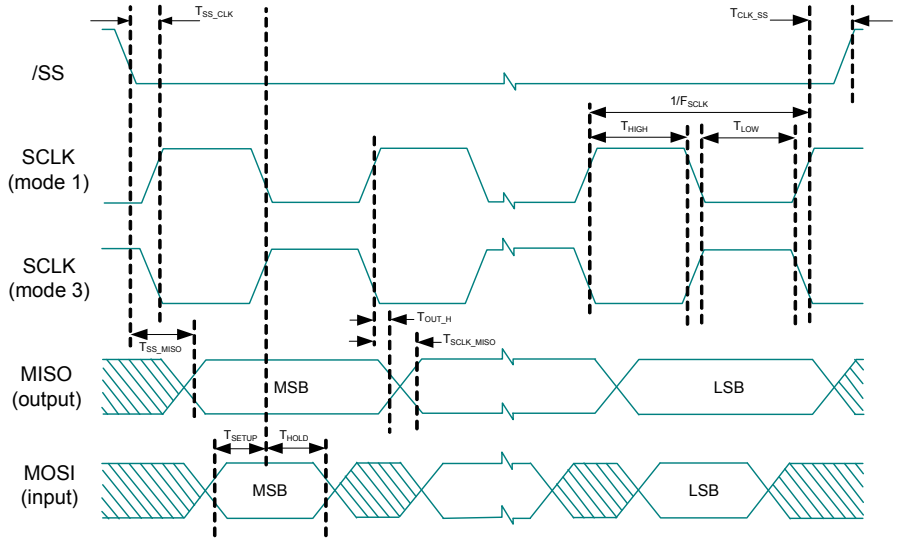


Figure 15. SPI Slave Mode 1 and 3

SPI Slave, modes 1 and 3



Thermal Impedances

Table 32. Thermal Impedances per Package

Package	Typical θ_{JA} [57]
16-pin SOIC	95 °C/W
16-pin QFN	33 °C/W
24-pin QFN[58]	21 °C/W
32-pin QFN[58]	20 °C/W
48-pin QFN[58]	18 °C/W
30-ball WLCSP	54 °C/W

Capacitance on Crystal Pins

Table 33. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-Pin QFN	3.2 pF
48-Pin QFN	3.3 pF

Solder Reflow Peak Temperature

Table 34 shows the solder reflow temperature limits that must not be exceeded.

Table 34. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
16-pin SOIC	260 °C	30 seconds
16-pin QFN	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
30-ball WLCSP	260 °C	30 seconds

Notes
57. $T_J = T_A + \text{Power} \times \theta_{JA}$.
58. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

Third Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation > Evaluation Boards.

Ordering Information

Table 35 lists the CY8C20x37/47/67/S PSoC devices' key package features and ordering codes.

Table 35. PSoC Device Key Features and Ordering Information

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	CapSense Sensors	Digital I/O Pins	Analog Inputs [59]	XRES Pin	ADC
CY8C20237-24SXI	16-pin SOIC	8 K	1 K	10	13	13	Yes	Yes
CY8C20247S-24SXI	16-pin SOIC	16 K	2 K	10	13	13	Yes	Yes
CY8C20237-24LKXI	16-pin QFN	8 K	1 K	10	13	13	Yes	Yes
CY8C20237-24LKXIT	16-pin QFN (Tape and Reel)	8 K	1 K	10	13	13	Yes	Yes
CY8C20247S-24LKXI	16-pin QFN	16 K	2 K	10	13	13	Yes	Yes
CY8C20247S-24LKXIT	16-pin QFN (Tape and Reel)	16 K	2 K	10	13	13	Yes	Yes
CY8C20337-24LQXI	24-pin QFN	8 K	1 K	16	19	19	Yes	Yes
CY8C20337-24LQXIT	24-pin QFN (Tape and Reel)	8 K	1 K	16	19	19	Yes	Yes
CY8C20347-24LQXI	24-pin QFN	16 K	2 K	16	19	19	Yes	Yes
CY8C20347-24LQXIT	24-pin QFN (Tape and Reel)	16 K	2 K	16	19	19	Yes	Yes
CY8C20347S-24LQXI	24-pin QFN	16 K	2 K	16	19	19	Yes	Yes
CY8C20347S-24LQXIT	24-pin QFN (Tape and Reel)	16 K	2 K	16	19	19	Yes	Yes
CY8C20437-24LQXI	32-pin QFN	8 K	1 K	25	28	28	Yes	Yes
CY8C20437-24LQXIT	32-pin QFN (Tape and Reel)	8 K	1 K	25	28	28	Yes	Yes
CY8C20447-24LQXI	32-pin QFN	16 K	2 K	25	28	28	Yes	Yes
CY8C20447-24LQXIT	32-pin QFN (Tape and Reel)	16 K	2 K	25	28	28	Yes	Yes
CY8C20447S-24LQXI	32-pin QFN	16 K	2 K	25	28	28	Yes	Yes
CY8C20447S-24LQXIT	32-pin QFN (Tape and Reel)	16 K	2 K	25	28	28	Yes	Yes
CY8C20467-24LQXI	32-pin QFN	32 K	2 K	25	28	28	Yes	Yes
CY8C20467-24LQXIT	32-pin QFN (Tape and Reel)	32 K	2 K	25	28	28	Yes	Yes
CY8C20467S-24LQXI	32-pin QFN	32 K	2 K	25	28	28	Yes	Yes
CY8C20467S-24LQXIT	32-pin QFN (Tape and Reel)	32 K	2 K	25	28	28	Yes	Yes
CY8C20637-24LQXI	48-pin QFN	8 K	1 K	31	34	34	Yes	Yes
CY8C20637-24LQXIT	48-pin QFN (Tape and Reel)	8 K	1 K	31	34	34	Yes	Yes
CY8C20647-24LQXI	48-pin QFN	16 K	2 K	31	34	34	Yes	Yes
CY8C20647-24LQXIT	48-pin QFN (Tape and Reel)	16 K	2 K	31	34	34	Yes	Yes
CY8C20647S-24LQXI	48-pin QFN	16 K	2 K	31	34	34	Yes	Yes
CY8C20647S-24LQXIT	48-pin QFN (Tape and Reel)	16 K	2 K	31	34	34	Yes	Yes
CY8C20667-24LQXI	48-pin QFN	32 K	2 K	31	34	34	Yes	Yes
CY8C20667-24LQXIT	48-pin QFN (Tape and Reel)	32 K	2 K	31	34	34	Yes	Yes
CY8C20667S-24LQXI	48-pin QFN	32 K	2 K	31	34	34	Yes	Yes
CY8C20667S-24LQXIT	48-pin QFN (Tape and Reel)	32 K	2 K	31	34	34	Yes	Yes

Note
59. Dual-function Digital I/O Pins also connect to the common analog mux.

Acronyms

The following table lists the acronyms that are used in this document.

Table 36. Acronyms Used in this Document

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
ESD	electrostatic discharge
FSR	full scale range
GPIO	general purpose input/output
I^2C	inter-integrated circuit
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
ISSP	in-system serial programming
LCD	liquid crystal display
LDO	low dropout (regulator)
LED	light-emitting diode
LPC	low power comparator
LSB	least-significant bit
LVD	low voltage detect
MCU	micro-controller unit
MIPS	million instructions per second
MISO	master in slave out
MOSI	master out slave in
MSB	most-significant bit
OCD	on-chip debug
PCB	printed circuit board
POR	power on reset
PSRR	power supply rejection ratio
PWRSYS	power system
PSoC	programmable system-on-chip
QFN	quad flat no-lead
SCLK	serial I^2C clock
SDA	serial I^2C data
SDATA	serial ISSP data
SOIC	small outline integrated circuit
SPI	serial peripheral interface
SRAM	static random access memory
SS	slave select
USB	universal serial bus
WLCSP	wafer level chip scale package

Reference Documents

- *Technical reference manual for CY20xx7 devices*
- *In-system Serial Programming (ISSP) protocol for 20xx7*
- *Host Sourced Serial Programming for 20xx7 devices*

Document Conventions

Units of Measure

Table 37 lists all the abbreviations used to measure the PSoC devices.

Table 37. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibel
kHz	kilohertz
ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Errata

This section describes the errata for the CY8C20xx7/S family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY8C20xx7/S Qualification Status

Product Status: Production released.

CY8C20xx7/S Errata Summary

The following Errata items apply to the CY8C20xx7/S datasheet 001-69257.

1. DoubleTimer0 ISR

■Problem Definition

When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

■Parameters Affected

No datasheet parameters are affected.

■Trigger Condition(S)

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

■Scope of Impact

The ISR may be executed twice.

■Workaround

In the ISR, firmware should clear the one-shot bit with a statement such as “`and reg[B0h], FDh`”

■Fix Status

Will not be fixed

■Changes

None

2. Missed GPIO Interrupt

■Problem Definition

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

■Parameters Affected

No datasheet parameters are affected.

■Trigger Condition(S)

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

■Scope of Impact

The GPIO interrupt service routine will not be run.

■Workaround

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt.

Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0.

Alternatively, the ISR’s for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

■Fix Status

Will not be fixed

■Changes

None

5. Wake-up from Sleep with Hardware I2C Address match on Pins P1[0], P1[1]

■Problem Definition

I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL, to wake-up from sleep using I2C hardware address match event.

■Parameters Affected

$t_{HD;DAT}$ increased to 20 ns from 0 ns

■Trigger Condition(S)

This is an issue only when all these three conditions are met:

1) P1.0 and P1.1 are used as I2C pins,

2) Wakeup from sleep with hardware address match feature is enabled, and

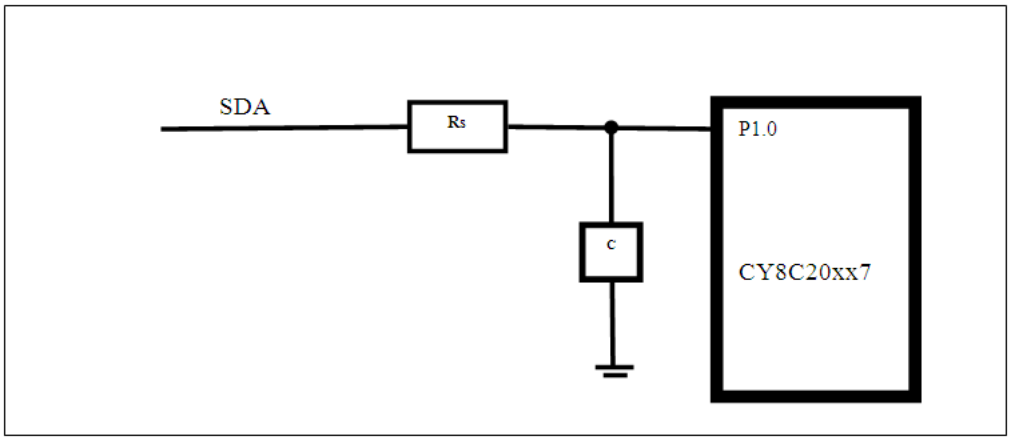
3) I2C master does not provide 20 ns hold time on SDA with respect to falling edge of SCL.

■Scope of Impact

These trigger conditions cause the device to never wake-up from sleep based on I2C address match event.

■Workaround

For a design that meets all of the trigger conditions, the following suggested circuit has to be implemented as a work-around. The R and C values proposed are 100 ohm and 200 pF respectively.



■Fix Status

Will not be fixed

■Changes

None

Document History Page

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3276782	DST	06/27/2011	New silicon and document
*A	3327230	DST	07/28/2011	Changed 48-pin dimensions to 6 × 6 × 0.6 mm QFN Updated pins name in Table 3 on page 9 and removed USB column and updated dimensions for 48-pin parts in Table 35 on page 33 Updated Figure 20 on page 29 Removed ICE and Debugger sections. Removed CY3215 Development Kit and CY3280-20x66 UCC sections. Updated Ordering Information.
*B	3403111	YVA	10/12/2011	Moved status from Advance to Preliminary. Updated Ordering Information Removed the row named “48-Pin (6 × 6 mm) QFN (OCD)”. Changed all 48-pin ordering code column from CY8C20XXX-24LTxx to CY8C20XXX-24LQxx. Updated 16-pin SOIC and 16-pin QFN package drawings.
*C	3473317	DST	12/23/2011	Updated Features. Updated Pinouts (Removed PSoC in captions of Figure 2, Figure 3, Figure 4, Figure 6, and Figure 7). Updated DC Chip-Level Specifications under Electrical Specifications (Updated typical value of I_{DD24} parameter from 3.32 mA to 2.88 mA, updated typical value of I_{DD12} parameter from 1.86 mA to 1.71 mA, updated typical value of I_{DD6} parameter from 1.13 mA to 1.16 mA, updated maximum value of I_{SB0} parameter from 0.50 µA to 1.1 µA, added I_{SBI2C} parameter and its details). Updated DC GPIO Specifications under Electrical Specifications (Added the parameters namely $V_{ILLVT3.3}$, $V_{IHLVT3.3}$, $V_{ILLVT5.5}$, $V_{IHLVT5.5}$ and their details in Table 10, added the parameters namely $V_{ILLVT2.5}$, $V_{IHLVT2.5}$ and their details in Table 11). Added the following sections namely DC I2C Specifications, Shield Driver DC Specifications, and DC IDAC Specifications under Electrical Specifications. Updated AC Chip-Level Specifications (Added the parameter namely t_{JIT_IMO} and its details). Updated Ordering Information (updated Table 35).
*D	3510277	YVA/DST	02/16/2012	Added CY8C20x37/37S/47/47S/67/67S part numbers and changed title to “1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders” Updated Features. Modified comparator blocks in Logic Block Diagram. Replaced SmartSense with SmartSense auto-tuning. Added CY8C20xx7S part numbers in Pin Definitions. Added footnote for Table 20. Updated Table 21 and Table 22 and added Table 23. Updated F_{32K1} min value. Updated data hold time min values. Updated CY8C206x7 part information in Table “Emulation and Programming Accessories”. Updated Ordering Information.
*E	3539259	DST	03/01/2012	Changed Datasheet status from Preliminary to Final. Updated all Pinouts to include Driven Shield Output (optional) information. Updated Min value for V_{LPC} Table 15. Updated Offset and Input range in Table 16.

Document History Page *(continued)*

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*K	4248645	DST	01/16/2014	Updated Pinouts: Updated 32-pin QFN (25 Sensing Inputs)[25]: Updated Figure 6. Updated Packaging Information: spec 001-09116 – Changed revision from *H to *I.
*L	4404150	SLAN	06/10/2014	Updated Pinouts: Updated 16-pin SOIC (10 Sensing Inputs): Updated Table 1: Added Note 6 and referred the same note in description of XRES pin. Updated 16-pin QFN (10 Sensing Inputs)[8]: Updated Table 2: Added Note 12 and referred the same note in description of XRES pin. Updated 24-pin QFN (16 Sensing Inputs)[14]: Updated Table 3: Added Note 18 and referred the same note in description of XRES pin. Updated 30-ball WLCSP (24 Sensing Inputs): Updated Table 4: Added Note 21 and referred the same note in description of XRES pin. Updated 32-pin QFN (25 Sensing Inputs)[25]: Updated Table 5: Added Note 29 and referred the same note in description of XRES pin. Updated 48-pin QFN (31 Sensing Inputs)[31]: Updated Table 6: Added Note 35 and referred the same note in description of XRES pin. Updated Electrical Specifications: Updated DC GPIO Specifications: Updated Table 10: Updated minimum and maximum values of V_{IH} parameter. Updated Table 11: Updated minimum and maximum values of V_{IH} parameter. Updated AC Chip-Level Specifications: Updated Table 24: Removed minimum and maximum values of “ILO untrimmed frequency”. Updated Packaging Information: spec 001-09116 – Changed revision from *I to *J. Completing Sunset Review.
*M	4825924	SLAN	07/07/2015	Added the footnote “All VSS pins should be brought out to one common GND plane” in pinout tables (Table 1 through Table 6). Updated Packaging Information: spec 001-13937 – Changed revision from *E to *F. Updated to new template.
*N	5068999	ARVI	12/31/2015	Updated hyperlink of “Technical Reference Manual” in all instances across the document. Updated PSoC® Functional Overview: Updated Additional System Resources: Updated description. Updated Development Tool Selection: Removed “Accessories (Emulation and Programming)”. Removed “Build a PSoC Emulator into Your Board”.