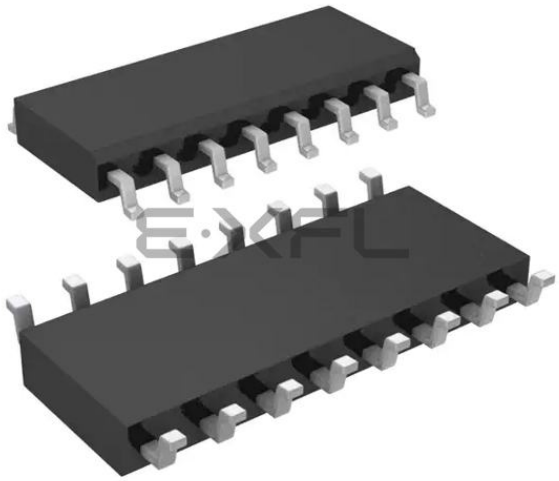

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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

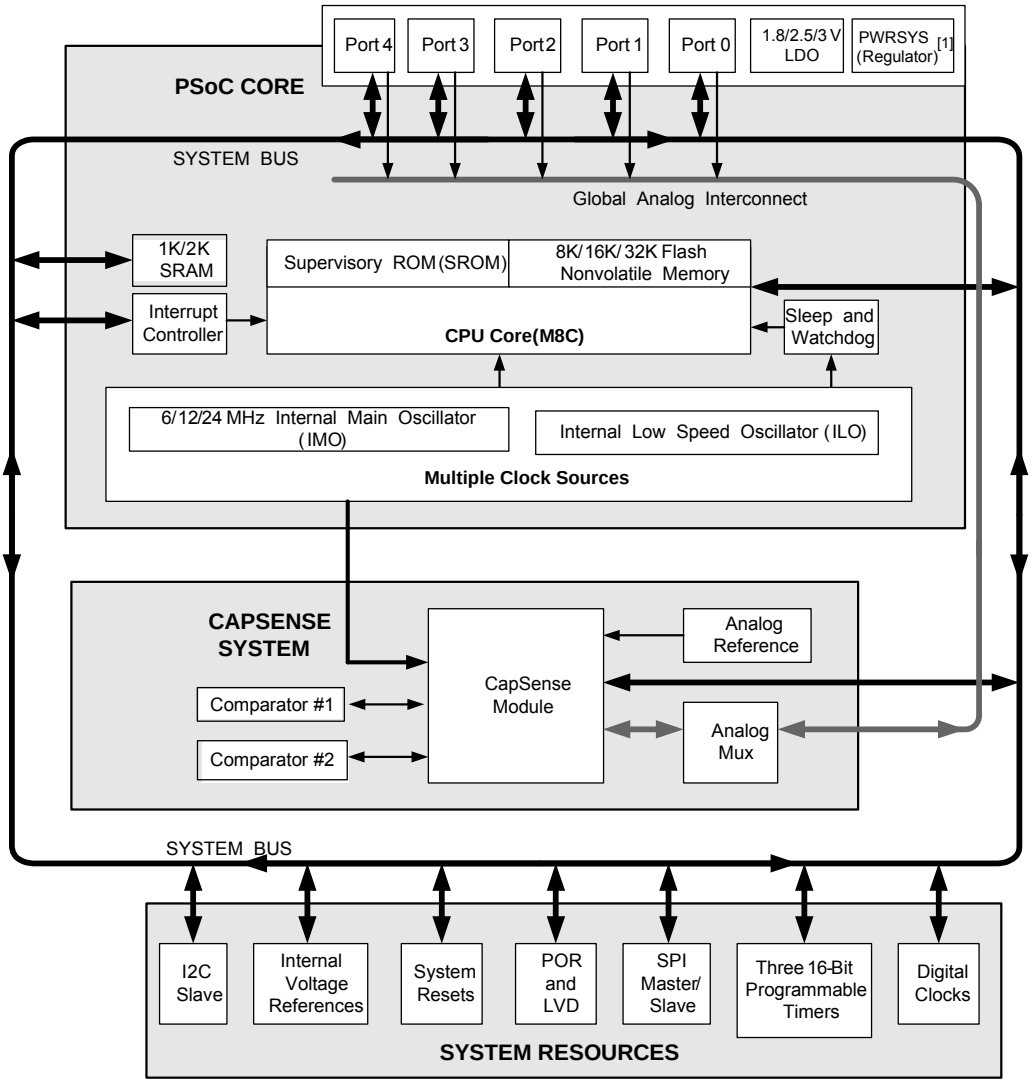
Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Obsolete |
| Applications | Capacitive Sensing |
| Core Processor | M8C |
| Program Memory Type | FLASH (8kB) |
| Controller Series | CY8C20xx7/S |
| RAM Size | 1K x 8 |
| Interface | I²C, SPI |
| Number of I/O | 14 |
| Voltage - Supply | 1.71V ~ 5.5V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 16-SOIC (0.154", 3.90mm Width) |
| Supplier Device Package | 16-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20237-24sxi |

## Logic Block Diagram




**Note**
1. Internal voltage regulator for internal circuitry

## Contents

## PSoC® Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional MCU-based system components with one low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the "Logic Block Diagram" on page 2, consists of three main areas:

- The core
- CapSense analog system
- System resources

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20x37/47/67/S PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 34 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

### PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-million instructions per second (MIPS), 8-bit Harvard-architecture microprocessor.

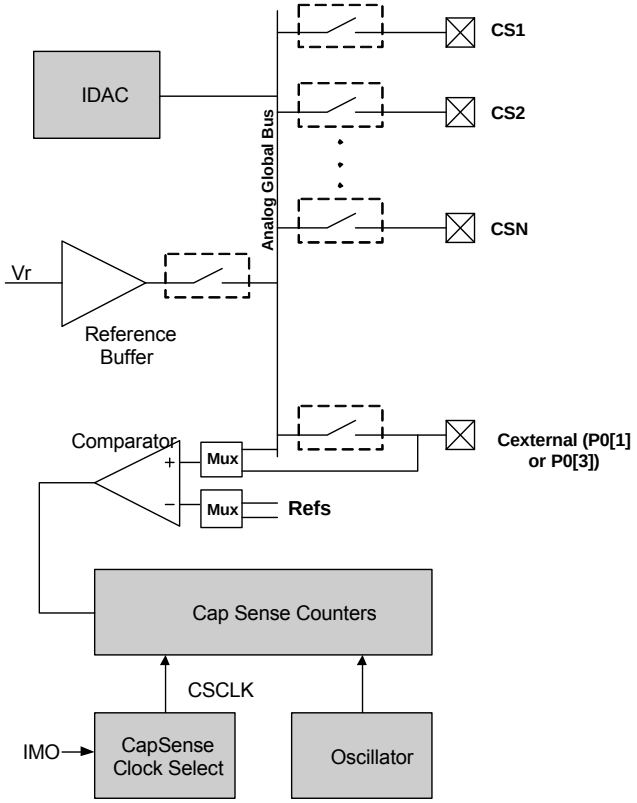
### CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1 V or 1.2 V analog reference, which together support capacitive sensing of up to 31 inputs[2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple ports.

*SmartSense™ Auto-tuning*

SmartSense auto-tuning is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters of each sensor during run time. SmartSense auto-tuning allows engineers to go from prototyping to mass production without retuning for manufacturing variations in PCB and/or overlay material properties.

**Figure 1. CapSense System Block Diagram**




*Analog Multiplexer System*

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

**Note**
2. 34 GPIOs = 31 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.

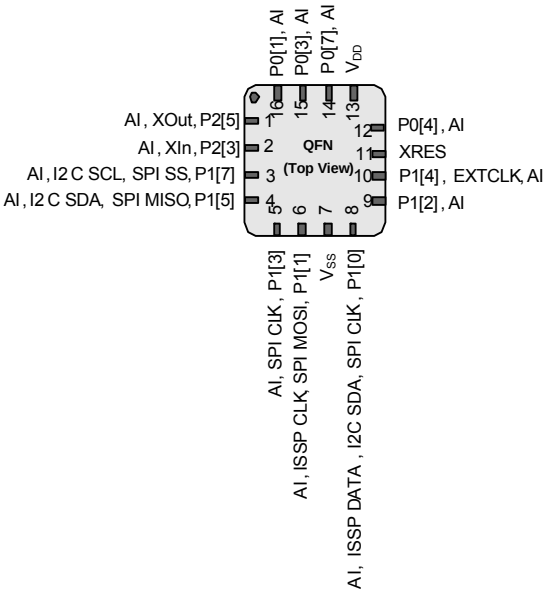
## 16-pin QFN (10 Sensing Inputs)[8]

**Table 2. Pin Definitions – CY8C20237, CY8C20247/S** [9]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | Crystal output (XOut) |
| 2 | I/O | I | P2[3] | Crystal input (XIn) |
| 3 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| 4 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| 5 | IOHR | I | P1[3] | SPI CLK |
| 6 | IOHR | I | P1[1] | ISSP CLK[10], $I^2C$ SCL, SPI MOSI |
| 7 | Power | | $V_{SS}$ | Ground connection[13] |
| 8 | IOHR | I | P1[0] | ISSP DATA[10], $I^2C$ SDA, SPI CLK[11] |
| 9 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 10 | IOHR | I | P1[4] | Optional external clock (EXTCLK) |
| 11 | Input | | XRES | Active high external reset with internal pull-down[12] |
| 12 | IOH | I | P0[4] | |
| 13 | Power | | $V_{DD}$ | Supply voltage |
| 14 | IOH | I | P0[7] | |
| 15 | IOH | I | P0[3] | Integrating input |
| 16 | IOH | I | P0[1] | Integrating input |

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 3. CY8C20237, CY8C20247/S Device**




**Notes**
8. No center pad.
9. 13 GPIOs = 10 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
10. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
11. Alternate SPI clock.
12. The internal pull down is 5KOhm.
13. All VSS pins should be brought out to one common GND plane.

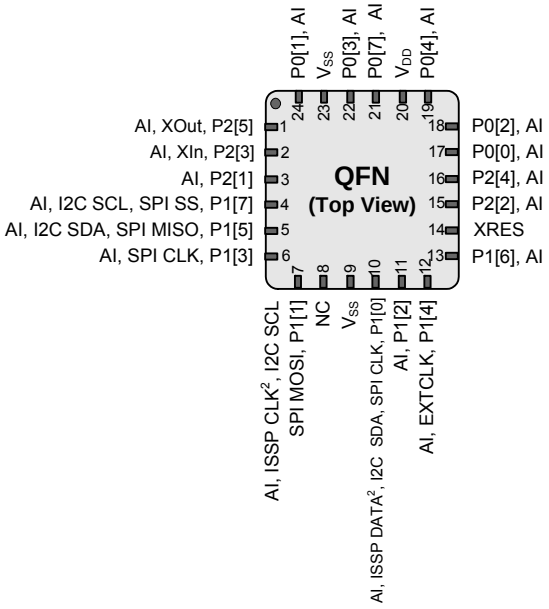
## 24-pin QFN (16 Sensing Inputs)[14]

**Table 3. Pin Definitions – CY8C20337, CY8C20347/S** [15]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | Crystal output (XOut) |
| 2 | I/O | I | P2[3] | Crystal input (XIn) |
| 3 | I/O | I | P2[1] | |
| 4 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| 5 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| 6 | IOHR | I | P1[3] | SPI CLK |
| 7 | IOHR | I | P1[1] | ISSP CLK[16], $I^2C$ SCL, SPI MOSI |
| 8 | | | NC | No connection |
| 9 | Power | | $V_{SS}$ | Ground connection[19] |
| 10 | IOHR | I | P1[0] | ISSP DATA[16], $I^2C$ SDA, SPI CLK[17] |
| 11 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 12 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 13 | IOHR | I | P1[6] | |
| 14 | Input | | XRES | Active high external reset with internal pull-down[18] |
| 15 | I/O | I | P2[2] | Driven Shield Output (optional) |
| 16 | I/O | I | P2[4] | Driven Shield Output (optional) |
| 17 | IOH | I | P0[0] | Driven Shield Output (optional) |
| 18 | IOH | I | P0[2] | Driven Shield Output (optional) |
| 19 | IOH | I | P0[4] | |
| 20 | Power | | $V_{DD}$ | Supply voltage |
| 21 | IOH | I | P0[7] | |
| 22 | IOH | I | P0[3] | Integrating input |
| 23 | Power | | $V_{SS}$ | Ground connection[19] |
| 24 | IOH | I | P0[1] | Integrating input |
| CP | Power | | $V_{SS}$ | Center pad must be connected to ground |

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 4. CY8C20337, CY8C20347/S Device**




**Notes**

14. The center pad (CP) on the QFN package must be connected to ground ($V_{SS}$) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. 19 GPIOs = 16 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
16. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
17. Alternate SPI clock.
18. The internal pull down is 5KOhm.
19. All VSS pins should be brought out to one common GND plane.

### 30-ball WLCSP (24 Sensing Inputs)

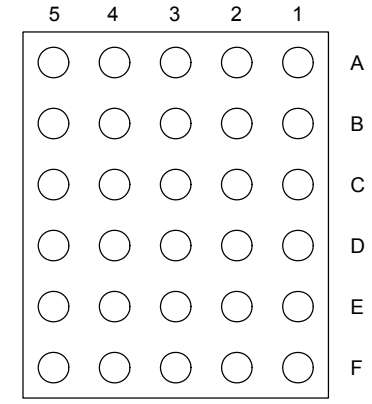
**Table 4. Pin Definitions – CY8C20767, CY8C20747 30-ball Part Pinout (WLCSP)** [20]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| A1 | IOH | I | P0[2] | Driven Shield Output (optional) |
| A2 | IOH | I | P0[6] | |
| A3 | Power | | $V_{DD}$ | Supply voltage |
| A4 | IOH | I | P0[1] | Integrating Input |
| A5 | I/O | I | P2[7] | |
| B1 | I/O | I | P4[2] | |
| B2 | IOH | I | P0[0] | Driven Shield Output (optional) |
| B3 | IOH | I | P0[4] | |
| B4 | IOH | I | P0[3] | Integrating Input |
| B5 | I/O | I | P2[5] | Crystal Output (Xout) |
| C1 | I/O | I | P2[2] | Driven Shield Output (optional) |
| C2 | I/O | I | P2[4] | Driven Shield Output (optional) |
| C3 | I/O | I | P0[7] | |
| C4 | IOH | I | P3[2] | |
| C5 | I/O | I | P2[3] | Crystal Input (Xin) |
| D1 | I/O | I | P2[0] | |
| D2 | I/O | I | P3[0] | |
| D3 | I/O | I | P3[1] | |
| D4 | I/O | I | P3[3] | |
| D5 | I/O | I | P2[1] | |
| E1 | Input | | XRES | Active high external reset with internal pull-down[21] |
| E2 | IOHR | I | P1[6] | |
| E3 | IOHR | I | P1[4] | Optional external clock input (EXT CLK) |
| E4 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| E5 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| F1 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| F2 | IOHR | I | P1[0] | ISSP DATA[22], $I^2C$ SDA, SPI CLK[23] |
| F3 | Power | | $V_{SS}$ | Supply ground[24] |
| F4 | IOHR | I | P1[1] | ISSP CLK[22], $I^2C$ SCL, SPI MOSI |
| F5 | IOHR | I | P1[3] | SPI CLK |

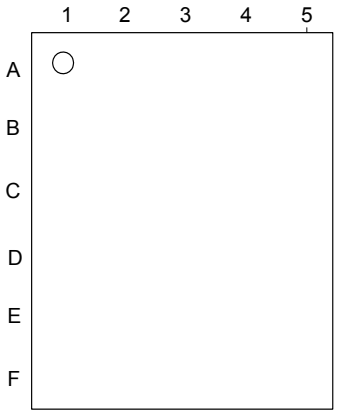
**LEGEND:** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

**Figure 5. CY8C20767, CY8C20747 30-ball WLCSP**

**Bottom View**




**Top View**




**Notes**

20. 27 GPIOs = 24 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
21. The internal pull down is 5KOhm.
22. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
23. Alternate SPI clock.
24. All VSS pins should be brought out to one common GND plane.

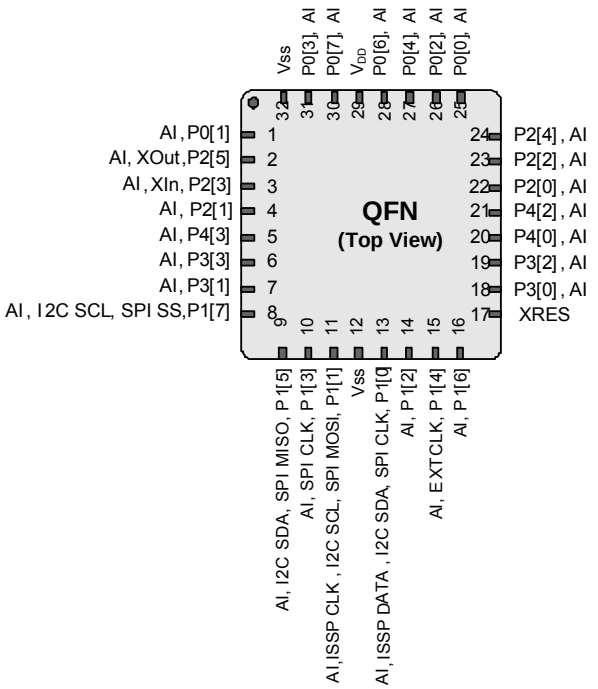
## 32-pin QFN (25 Sensing Inputs)[25]

**Table 5. Pin Definitions – CY8C20437, CY8C20447/S, CY8C20467/S** [26]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IOH | I | P0[1] | Integrating input |
| 2 | I/O | I | P2[5] | Crystal output (XOut) |
| 3 | I/O | I | P2[3] | Crystal input (XIn) |
| 4 | I/O | I | P2[1] | |
| 5 | I/O | I | P4[3] | |
| 6 | I/O | I | P3[3] | |
| 7 | I/O | I | P3[1] | |
| 8 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| 9 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| 10 | IOHR | I | P1[3] | SPI CLK. |
| 11 | IOHR | I | P1[1] | ISSP CLK[27], $I^2C$ SCL, SPI MOSI. |
| 12 | Power | | $V_{SS}$ | Ground connection[30] |
| 13 | IOHR | I | P1[0] | ISSP DATA[27], $I^2C$ SDA, SPI CLK[28] |
| 14 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 15 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 16 | IOHR | I | P1[6] | |
| 17 | Input | | XRES | Active high external reset with internal pull-down[29] |
| 18 | I/O | I | P3[0] | |
| 19 | I/O | I | P3[2] | |
| 20 | I/O | I | P4[0] | |
| 21 | I/O | I | P4[2] | |
| 22 | I/O | I | P2[0] | |
| 23 | I/O | I | P2[2] | Driven Shield Output (optional) |
| 24 | I/O | I | P2[4] | Driven Shield Output (optional) |
| 25 | IOH | I | P0[0] | Driven Shield Output (optional) |
| 26 | IOH | I | P0[2] | Driven Shield Output (optional) |
| 27 | IOH | I | P0[4] | |
| 28 | IOH | I | P0[6] | |
| 29 | Power | | $V_{DD}$ | |
| 30 | IOH | I | P0[7] | |
| 31 | IOH | I | P0[3] | Integrating input |
| 32 | Power | | $V_{SS}$ | Ground connection[30] |
| CP | Power | | $V_{SS}$ | Center pad must be connected to ground |

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 6. CY8C20437, CY8C20447/S, CY8C20467/S Device**




**Notes**

25. The center pad (CP) on the QFN package must be connected to ground ($V_{SS}$) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
26. 28 GPIOs = 25 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
27. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
28. Alternate SPI clock.
29. The internal pull down is 5KOhm.
30. All VSS pins should be brought out to one common GND plane.

## DC Chip-Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 9. DC Chip-Level Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ [37, 38, 39] | Supply voltage | See Table 14 on page 17. | 1.71 | – | 5.50 | V |
| $I_{DD24}$ | Supply current, IMO = 24 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 2.88 | 4.00 | mA |
| $I_{DD12}$ | Supply current, IMO = 12 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 1.71 | 2.60 | mA |
| $I_{DD6}$ | Supply current, IMO = 6 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current | – | 1.16 | 1.80 | mA |
| $I_{SB0}$ [40, 41, 42, 43] | Deep sleep current | $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off | – | 0.10 | 1.1 | µA |
| $I_{SB1}$ [40, 41, 42, 43] | Standby current with POR, LVD and sleep timer | $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off | – | 1.07 | 1.50 | µA |
| $I_{SBI2C}$ [40, 41, 42, 43] | Standby current with $I^2C$ enabled | Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz | – | 1.64 | – | µA |

**Notes**

37. When $V_{DD}$ remains in the range from 1.71 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the $SR_{POWER\_UP}$ parameter.
38. If powering down in standby sleep mode, to properly detect and recover from a $V_{DD}$ brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that $V_{DD}$ falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of $V_{DD}$ is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the Technical Reference Manual. In deep sleep/standby sleep mode, additional low power voltage monitoring circuitry allows $V_{DD}$ brown out conditions to be detected and resets the device when $V_{DD}$ goes lower than 1.1 V at edge rates slower than 1 V/ms.
39. For proper CapSense block functionality, if the drop in $V_{DD}$ exceeds 5% of the base $V_{DD}$, the rate at which $V_{DD}$ drops should not exceed 200 mV/s. Base $V_{DD}$ can be between 1.8 V and 5.5 V.
40. Errata: When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the “Errata” on page 37.
41. Errata: When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the “Errata” on page 37.
42. Errata: If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the “Errata” on page 37.
43. Errata: Device wakes up from sleep when an analog interrupt is trigger. For more information, see the “Errata” on page 37.

**Table 11. 2.4 V to 3.0 V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| $V_{OH1}$ | High output voltage Port 2 or 3 pins | $I_{OH}$ < 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.20 | – | – | V |
| $V_{OH2}$ | High output voltage Port 2 or 3 Pins | $I_{OH}$ = 0.2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.40 | – | – | V |
| $V_{OH3}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | $I_{OH}$ < 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.20 | – | – | V |
| $V_{OH4}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | $I_{OH}$ = 2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.50 | – | – | V |
| $V_{OH5A}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | $I_{OH}$ < 10 µA, $V_{DD}$ > 2.4 V, maximum of 20 mA source current in all I/Os | 1.50 | 1.80 | 2.10 | V |
| $V_{OH6A}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | $I_{OH}$ = 1 mA, $V_{DD}$ > 2.4 V, maximum of 20 mA source current in all I/Os | 1.20 | – | – | V |
| $V_{OL}$ | Low output voltage | $I_{OL}$ = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| $V_{IL}$ | Input low voltage | – | – | – | 0.72 | V |
| $V_{IH}$ | Input high voltage | – | $V_{DD}$ × 0.65 | – | $V_{DD}$ + 0.7 | V |
| $V_H$ | Input hysteresis voltage | – | – | 80 | – | mV |
| $I_{IL}$ | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| $C_{PIN}$ | Capacitive load on pins | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |
| $V_{ILLVT2.5}$ | Input Low Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 0.7 | V | – | |
| $V_{IHLVT2.5}$ | Input High Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 1.2 | | – | V |

**Table 12. 1.71 V to 2.4 V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| $V_{OH1}$ | High output voltage Port 2 or 3 pins | $I_{OH}$ = 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH2}$ | High output voltage Port 2 or 3 pins | $I_{OH}$ = 0.5 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.50 | – | – | V |
| $V_{OH3}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | $I_{OH}$ = 100 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH4}$ | High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | $I_{OH}$ = 2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.50 | – | – | V |

## DC I²C Specifications

Table 20 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ $T_A$ ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 20. DC I²C Specifications**[50]

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{ILI2C}$ | Input low level | 3.1 V ≤ $V_{DD}$ ≤ 5.5 V | – | – | 0.25 × $V_{DD}$ | V |
| | | 2.5 V ≤ $V_{DD}$ ≤ 3.0 V | – | – | 0.3 × $V_{DD}$ | V |
| | | 1.71 V ≤ $V_{DD}$ ≤ 2.4 V | – | – | 0.3 × $V_{DD}$ | V |
| $V_{IHI2C}$ | Input high level | 1.71 V ≤ $V_{DD}$ ≤ 5.5 V | 0.65 × $V_{DD}$ | – | $V_{DD}$ + 0.7 V[51] | V |

## Shield Driver DC Specifications

Table 21 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ $T_A$ ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 21. Shield Driver DC Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{Ref}$ | Reference buffer output | 1.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.942 | – | 1.106 | V |
| $V_{RefHi}$ | Reference buffer output | 1.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.104 | – | 1.296 | V |

## DC IDAC Specifications

Table 22 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 22. DC IDAC Specifications (8-bit IDAC)**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| IDAC_DNL | Differential nonlinearity | –1 | – | 1 | LSB | – |
| IDAC_DNL | Integral nonlinearity | –2 | – | 2 | LSB | – |
| IDAC_Current | Range = 4x | 138 | – | 169 | µA | DAC setting = 127 dec |
| | Range = 8x | 138 | – | 169 | µA | DAC setting = 64 dec |

**Table 23. DC IDAC Specifications (7-bit IDAC)**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| IDAC_DNL | Differential nonlinearity | –1 | – | 1 | LSB | – |
| IDAC_DNL | Integral nonlinearity | –2 | – | 2 | LSB | – |
| IDAC_Current | Range = 4x | 137 | – | 168 | µA | DAC setting = 127 dec |
| | Range = 8x | 138 | – | 169 | µA | DAC setting = 64 dec |

**Notes**

50. Errata: Pull-up resistors on I2C interface cannot be connected to a supply voltage that is more than 0.7 V higher than the CY8C20xx7/S power supply. For more information see item #6 in the "Errata" on page 37.
51. Errata: For more information see item #6 in the "Errata" on page 37.

## AC Programming Specifications

**Figure 10. AC Waveform**

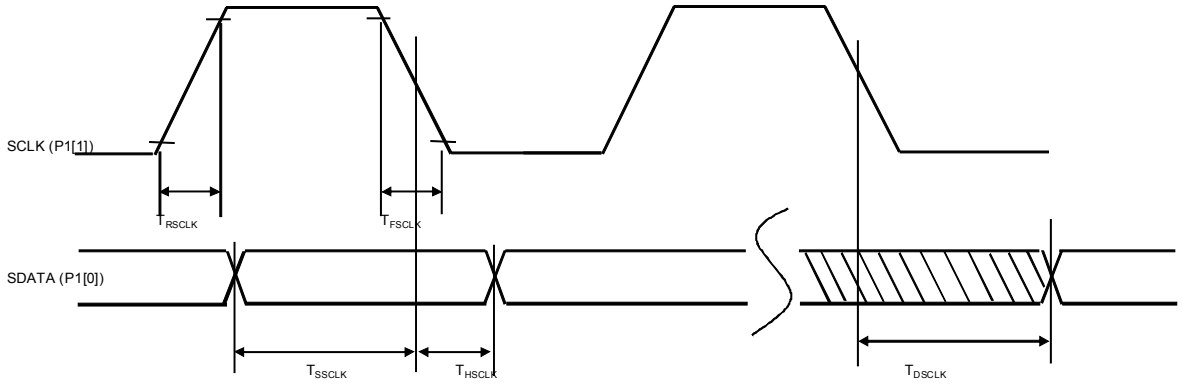



Table 28 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 28. AC Programming Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{RSCLK}$ | Rise time of SCLK | – | 1 | – | 20 | ns |
| $t_{FSCLK}$ | Fall time of SCLK | – | 1 | – | 20 | ns |
| $t_{SSCLK}$ | Data setup time to falling edge of SCLK | – | 40 | – | – | ns |
| $t_{HSCLK}$ | Data hold time from falling edge of SCLK | – | 40 | – | – | ns |
| $F_{SCLK}$ | Frequency of SCLK | – | 0 | – | 8 | MHz |
| $t_{ERASEB}$ | Flash erase time (block) | – | – | – | 18 | ms |
| $t_{WRITE}$ | Flash block write time | – | – | – | 25 | ms |
| $t_{DSCLK}$ | Data out delay from falling edge of SCLK | $3.6 < V_{DD}$ | – | – | 60 | ns |
| $t_{DSCLK3}$ | Data out delay from falling edge of SCLK | $3.0 \le V_{DD} \le 3.6$ | – | – | 85 | ns |
| $t_{DSCLK2}$ | Data out delay from falling edge of SCLK | $1.71 \le V_{DD} \le 3.0$ | – | – | 130 | ns |
| $t_{XRST3}$ | External reset pulse width after power-up | Required to enter programming mode when coming out of sleep | 300 | – | – | µs |
| $t_{XRES}$ | XRES pulse length | – | 300 | – | – | µs |
| $t_{VDDWAIT}$[54] | $V_{DD}$ stable to wait-and-poll hold off | – | 0.1 | – | 1 | ms |
| $t_{VDDXRES}$[54] | $V_{DD}$ stable to XRES assertion delay | – | 14.27 | – | – | ms |
| $t_{POLL}$ | SDAT high pulse time | – | 0.01 | – | 200 | ms |
| $t_{ACQ}$[54] | “Key window” time after a $V_{DD}$ ramp acquire event, based on 256 ILO clocks. | – | 3.20 | – | 19.60 | ms |
| $t_{XRESINI}$[54] | “Key window” time after an XRES event, based on 8 ILO clocks | – | 98 | – | 615 | µs |

**Note**
54. Valid from 5 to 50 °C. See the spec, CY8C20X66, CY8C20X46, CY8C20X36, CY7C643XX, CY7C604XX, CY8CTST2XX, CY8CTMG2XX, CY8C20X67, CY8C20X47, CY8C20X37, Programming Spec for more details.

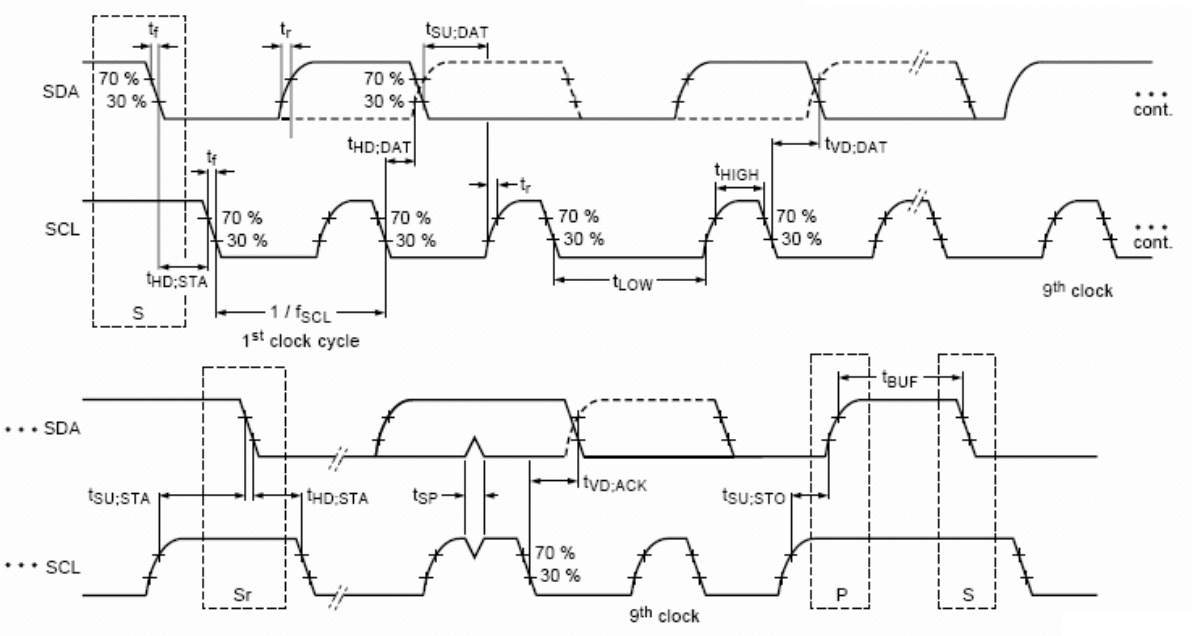
## AC I²C Specifications

Table 29 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 29. AC Characteristics of the I²C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0 | – | 0.6 | – | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | – | 1.3 | – | µs |
| $t_{HIGH}$ | HIGH Period of the SCL clock | 4.0 | – | 0.6 | – | µs |
| $t_{SU;STA}$ | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | µs |
| $t_{HD;DAT}$[55] | Data hold time | 20 | 3.45 | 20 | 0.90 | µs |
| $t_{SU;DAT}$ | Data setup time | 250 | – | 100[56] | – | ns |
| $t_{SU;STO}$ | Setup time for STOP condition | 4.0 | – | 0.6 | – | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | µs |
| $t_{SP}$ | Pulse width of spikes are suppressed by the input filter | – | – | 0 | 50 | ns |

**Figure 11. Definition for Timing for Fast/Standard Mode on the I²C Bus**




**Notes**

55. Errata: To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. For more information see item #5 in the "Errata" on page 37.
56. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

## Packaging Information

This section illustrates the packaging specifications for the CY8C20x37/47/67 PSoC device, along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

**Figure 16. 16-pin (150 Mil) SOIC**

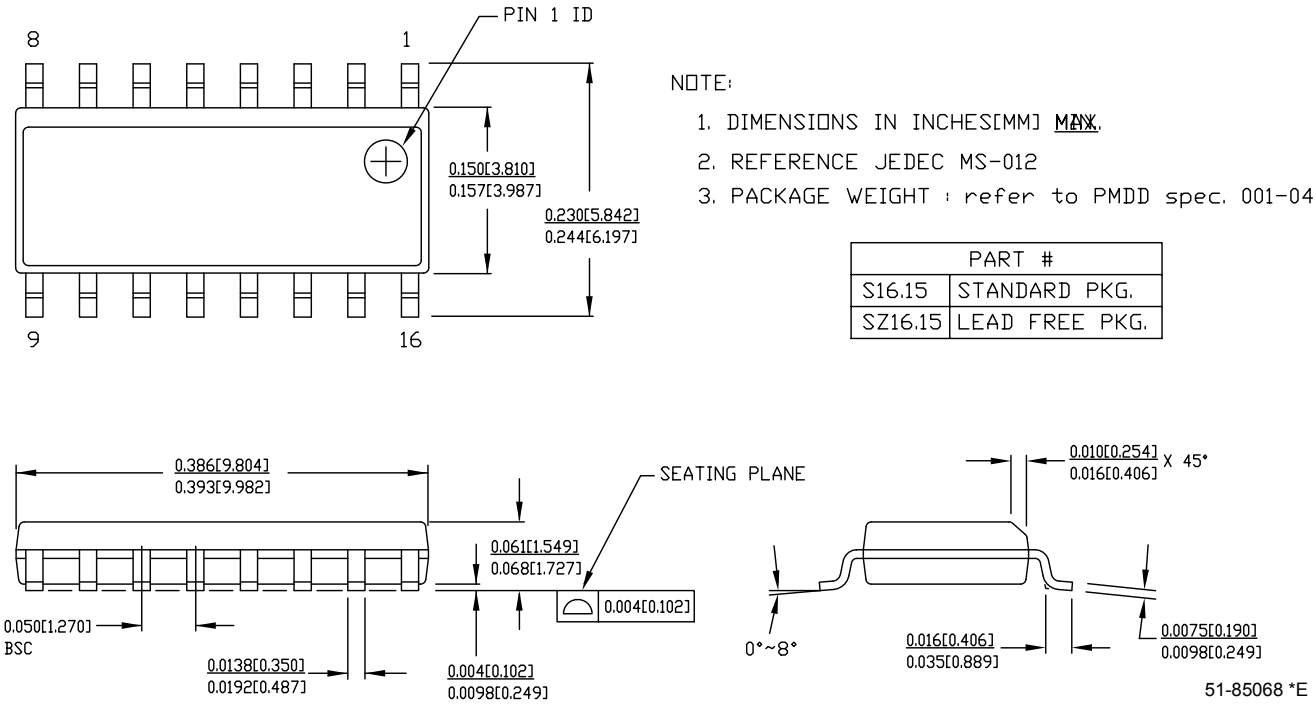
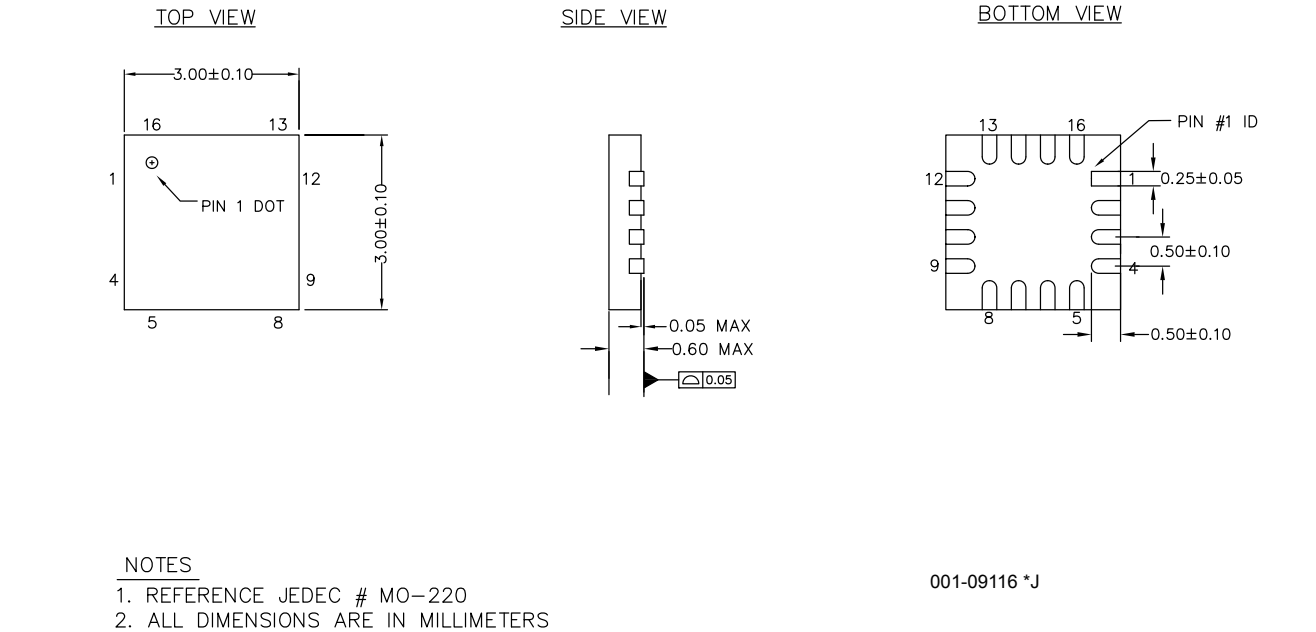



**Figure 17. 16-pin Chip-On-Lead (3 × 3 × 0.6 mm) (Sawn) Package Outline, 001-09116**



## Thermal Impedances

**Table 32. Thermal Impedances per Package**

| Package | Typical $\theta_{JA}$ [57] |
|---|---|
| 16-pin SOIC | 95 °C/W |
| 16-pin QFN | 33 °C/W |
| 24-pin QFN[58] | 21 °C/W |
| 32-pin QFN[58] | 20 °C/W |
| 48-pin QFN[58] | 18 °C/W |
| 30-ball WLCSP | 54 °C/W |

## Capacitance on Crystal Pins

**Table 33. Typical Package Capacitance on Crystal Pins**

| Package | Package Capacitance |
|---|---|
| 32-Pin QFN | 3.2 pF |
| 48-Pin QFN | 3.3 pF |

## Solder Reflow Peak Temperature

Table 34 shows the solder reflow temperature limits that must not be exceeded.

**Table 34. Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature ($T_C$) | Maximum Time above $T_C$ – 5 °C |
|---|---|---|
| 16-pin SOIC | 260 °C | 30 seconds |
| 16-pin QFN | 260 °C | 30 seconds |
| 24-pin QFN | 260 °C | 30 seconds |
| 32-pin QFN | 260 °C | 30 seconds |
| 48-pin QFN | 260 °C | 30 seconds |
| 30-ball WLCSP | 260 °C | 30 seconds |

**Notes**
57. $T_J = T_A + \text{Power} \times \theta_{JA}$.
58. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

## Development Tool Selection

### Software

*PSoC Designer™*

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, in-system programming support, and built-in support for third-party assemblers and C compilers. PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler.

*PSoC Designer Software Subsystems*

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

**Assemblers.** The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*PSoC Programmer*

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube in-circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at http://www.cypress.com/psocprogrammer.

### Development Kits

All development kits are sold at the Cypress Online Store.

### Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

*CY3210-MiniProg1*

The CY3210-MiniProg1 kit allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- 28-pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

*CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

## Acronyms

The following table lists the acronyms that are used in this document.

**Table 36. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CMOS | complementary metal oxide semiconductor |
| CPU | central processing unit |
| DAC | digital-to-analog converter |
| DC | direct current |
| ESD | electrostatic discharge |
| FSR | full scale range |
| GPIO | general purpose input/output |
| $I^2C$ | inter-integrated circuit |
| ICE | in-circuit emulator |
| ILO | internal low speed oscillator |
| IMO | internal main oscillator |
| I/O | input/output |
| ISSP | in-system serial programming |
| LCD | liquid crystal display |
| LDO | low dropout (regulator) |
| LED | light-emitting diode |
| LPC | low power comparator |
| LSB | least-significant bit |
| LVD | low voltage detect |
| MCU | micro-controller unit |
| MIPS | million instructions per second |
| MISO | master in slave out |
| MOSI | master out slave in |
| MSB | most-significant bit |
| OCD | on-chip debug |
| PCB | printed circuit board |
| POR | power on reset |
| PSRR | power supply rejection ratio |
| PWRSYS | power system |
| PSoC | programmable system-on-chip |
| QFN | quad flat no-lead |
| SCLK | serial $I^2C$ clock |
| SDA | serial $I^2C$ data |
| SDATA | serial ISSP data |
| SOIC | small outline integrated circuit |
| SPI | serial peripheral interface |
| SRAM | static random access memory |
| SS | slave select |
| USB | universal serial bus |
| WLCSP | wafer level chip scale package |

## Reference Documents

- *Technical reference manual for CY20xx7 devices*
- *In-system Serial Programming (ISSP) protocol for 20xx7*
- *Host Sourced Serial Programming for 20xx7 devices*

## Document Conventions

### Units of Measure

Table 37 lists all the abbreviations used to measure the PSoC devices.

**Table 37. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| dB | decibel |
| kHz | kilohertz |
| ksps | kilo samples per second |
| kΩ | kilohm |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

### 3. Missed Interrupt During Transition to Sleep

**■Problem Definition**

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

**■Parameters Affected**

No datasheet parameters are affected.

**■Trigger Condition(S)**

Triggered by enabling sleep mode just prior to an interrupt.

**■Scope of Impact**

The relevant interrupt service routine will not be run.

**■Workaround**

None.

**■Fix Status**

Will not be fixed

**■Changes**

None

### 4. Wakeup from sleep with analog interrupt

**■Problem Definition**

Device wakes up from sleep when an analog interrupt is trigger

**■Parameters Affected**

No datasheet parameters are affected.

**■Trigger Condition(S)**

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

**■Scope of Impact**

Device unexpectedly wakes up from sleep

**■Workaround**

Disable the analog interrupt before entering sleep and turn it back on upon wake-up.

**■Fix Status**

Will not be fixed

**■Changes**

None

## Document History Page *(continued)*

| Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors<br>Document Number: 001-69257 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *F | 3645807 | DST/BVI | 07/03/2012 | Updated $F_{SCLK}$ parameter in the Table 31, “SPI Slave AC Specifications,” on page 26<br>Changed $t_{OUT\_HIGH}$ to $t_{OUT\_H}$ in Table 30, “SPI Master AC Specifications,” on page 25<br>Updated Features section, “Programmable pin configurations” bullet:<br>■ Included the following sub-bullet point - 5 mA source current on port 0 and 1 and 1 mA on port 2,3 and 4<br>■ Changed the bullet point “High sink current of 25 mA for each GPIO” to “High sink current of 25 mA for each GPIO. Total 120 mA maximum sink current per chip”<br>■ Added “QuietZone™ Controller” bullet and updated “Low power CapSense® block with SmartSense™ auto-tuning” bullet.<br>Updated package diagrams 001-13937 to *D and 001-57280 to *C revisions. |
| *G | 3800055 | DST | 11/23/2012 | Changed document title.<br>Part named changed from CY8C20xx7 to CY8C20xx7/S<br>Table 20: Update to VIHI2C to match Item #6 in K2 Si Errata document (001-75370)<br>Updated package diagrams:<br>51-85068 to *E<br>001-09116 to *G<br>001-13937 to *E<br>001-42168 to *E<br>001-57280 to *E |
| *H | 3881332 | SRLI | 02/04/2013 | Updated Features:<br>Added Note “Please contact your nearest sales office for additional details.” and referred the same note in “24 Sensing Inputs – 30-pin WLCSP”. |
| *I | 3993458 | DST | 05/07/2013 | Updated Electrical Specifications (Updated DC GPIO Specifications (Updated heading of third column as “Port 0/1 per I/O (max)” for Table 13)).<br><br>Updated Packaging Information:<br>spec 001-09116 – Changed revision from *G to *H (Figure 17).<br><br>Added Errata. |
| *J | 4081796 | DST | 07/31/2013 | Added Errata footnotes (Note 40, 41, 42, 43, 44).<br><br>Updated already existing footnotes (Note 50, 51, 55) as Errata footnotes.<br><br>Updated Electrical Specifications:<br>Updated DC Chip-Level Specifications:<br>Added Note 40, 41, 42, 43 and referred the same notes in $I_{SB0}$, $I_{SB1}$, $I_{SBI2C}$ parameters.<br>Updated DC GPIO Specifications:<br>Added Note 44 and referred the same note in description of $V_{ILLVT3.3}$ parameter in Table 10.<br>Updated DC I2C Specifications:<br>Updated Note 50, 51 referred in Table 20.<br>Updated AC I2C Specifications:<br>Updated Note 55 referred in Table 29.<br><br>Updated to new template. |

## Document History Page *(continued)*

| Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors<br>Document Number: 001-69257 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *O | 5122184 | JFMD | 02/02/2016 | Updated Features:<br>Removed Note “Please contact your nearest sales office for additional details.” and its reference.<br>Updated Ordering Information:<br>Updated Table 35:<br>Updated part numbers. |

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