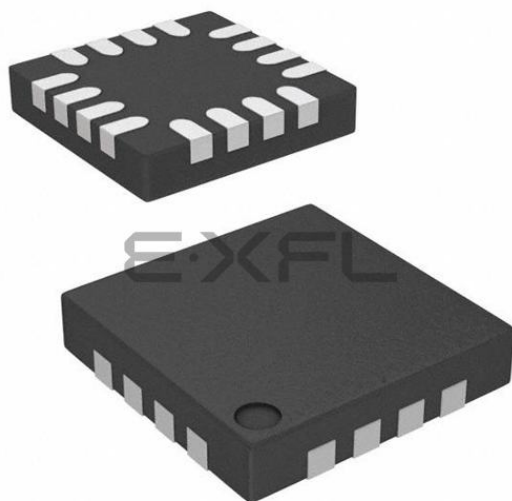




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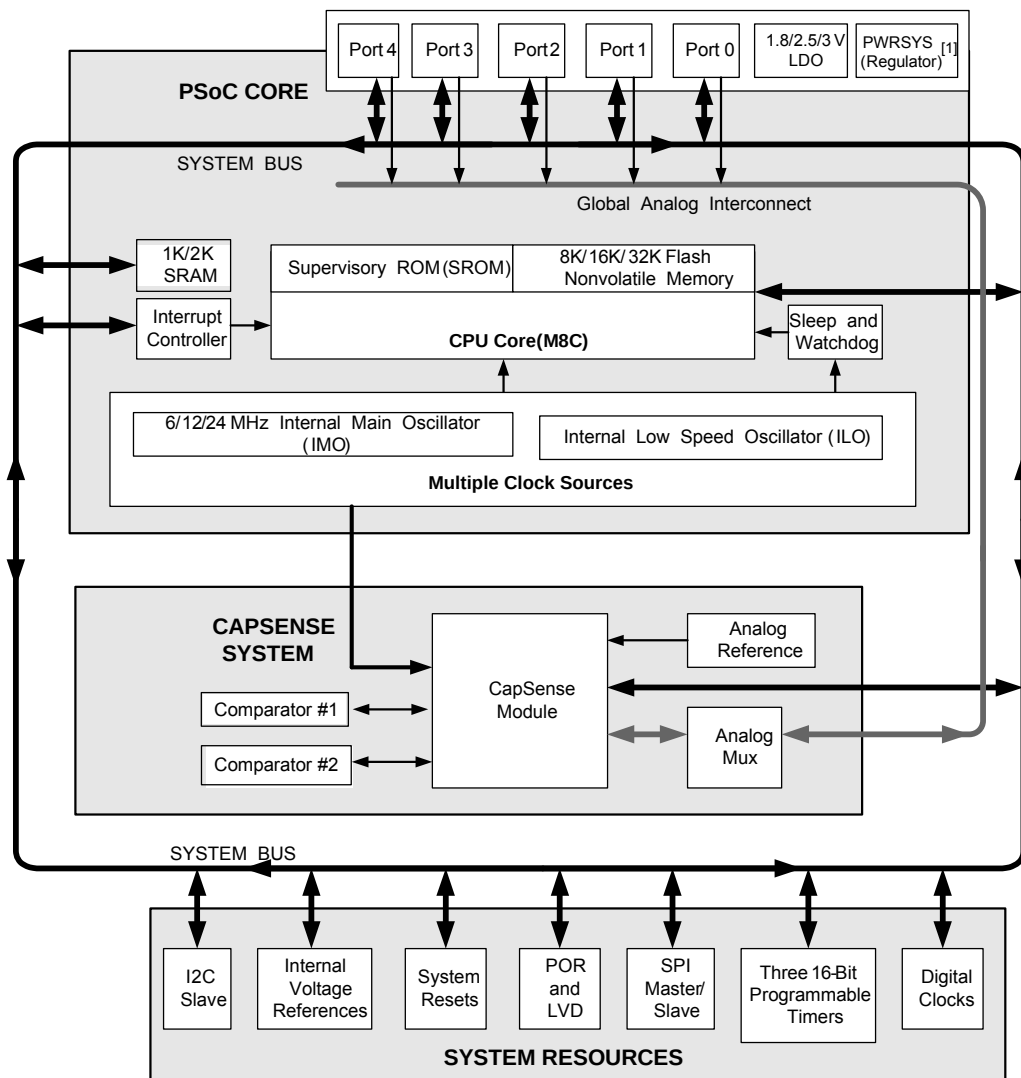
What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details

Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY8C20xx7/S
RAM Size	2K x 8
Interface	I ² C, SPI
Number of I/O	13
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20247-24lkxit

Logic Block Diagram



Note

1. Internal voltage regulator for internal circuitry

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Additional System Resources

System resources provide additional capability, such as configurable I²C slave, SPI master/slave communication interface, three 16-bit programmable timers, various system resets supported by the M8C low voltage detection and power-on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I²C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I²C enhanced slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For more details, refer to the [I2CSBUF User Module datasheet](#).
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for the CY8C20x37/47/67/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

Application Notes/Design Guides

Application notes and design guides are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/gocapsense. Select Application Notes under the Related Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. See “[Development Kits](#)” on page 31.

Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

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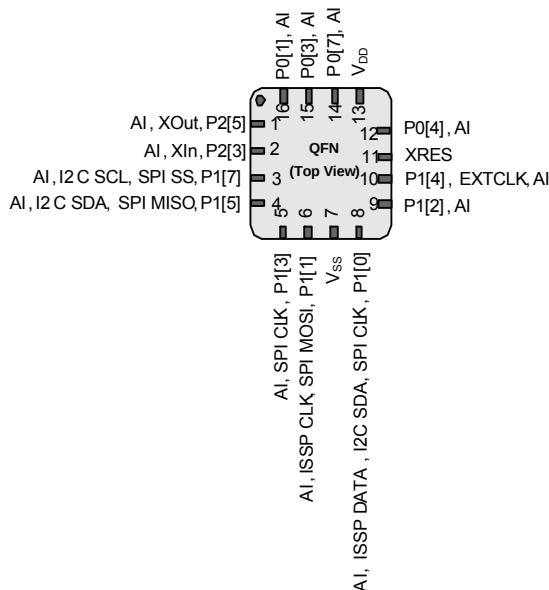
Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, create a technical support case or call technical support at 1-800-541-4736.

16-pin QFN (10 Sensing Inputs)^[8]
Table 2. Pin Definitions – CY8C20237, CY8C20247/S^[9]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I ² C SCL, SPI SS
4	IOHR	I	P1[5]	I ² C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK ^[10] , I ² C SCL, SPI MOSI
7	Power		V _{SS}	Ground connection ^[13]
8	IOHR	I	P1[0]	ISSP DATA ^[10] , I ² C SDA, SPI CLK ^[11]
9	IOHR	I	P1[2]	Driven Shield Output (optional)
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down ^[12]
12	IOH	I	P0[4]	
13	Power		V _{DD}	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 3. CY8C20237, CY8C20247/S Device

Notes

8. No center pad.
9. 13 GPIOs = 10 pins for capacitive sensing+2 pins for I²C + 1 pin for modulator capacitor.
10. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I²C bus. Use alternate pins if you encounter issues.
11. Alternate SPI clock.
12. The internal pull down is 5KOhm.
13. All VSS pins should be brought out to one common GND plane.

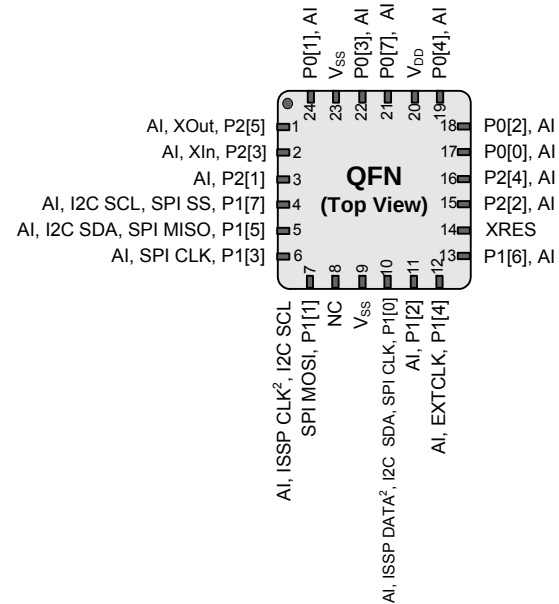
24-pin QFN (16 Sensing Inputs)^[14]
Table 3. Pin Definitions – CY8C20337, CY8C20347/S^[15]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I ² C SCL, SPI SS
5	IOHR	I	P1[5]	I ² C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK ^[16] , I ² C SCL, SPI MOSI
8			NC	No connection
9	Power		V _{SS}	Ground connection ^[19]
10	IOHR	I	P1[0]	ISSP DATA ^[16] , I ² C SDA, SPI CLK ^[17]
11	IOHR	I	P1[2]	Driven Shield Output (optional)
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down ^[18]
15	I/O	I	P2[2]	Driven Shield Output (optional)
16	I/O	I	P2[4]	Driven Shield Output (optional)
17	IOH	I	P0[0]	Driven Shield Output (optional)
18	IOH	I	P0[2]	Driven Shield Output (optional)
19	IOH	I	P0[4]	
20	Power		V _{DD}	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[3]	Integrating input
23	Power		V _{SS}	Ground connection ^[19]
24	IOH	I	P0[1]	Integrating input
CP	Power		V _{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

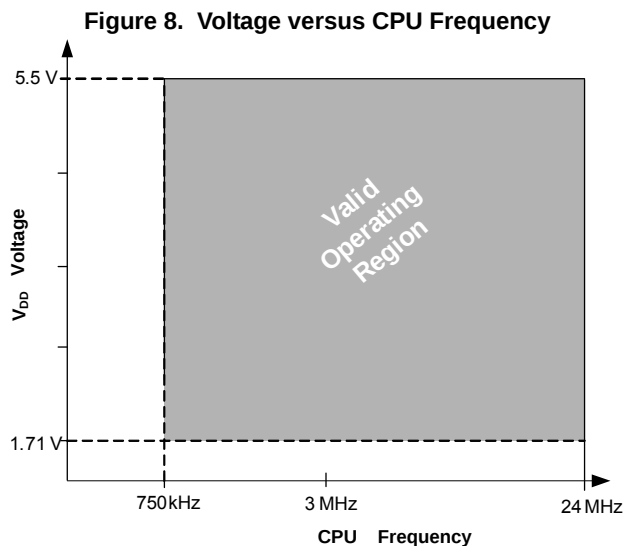
Notes

14. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. 19 GPIOs = 16 pins for capacitive sensing+2 pins for I²C + 1 pin for modulator capacitor.
16. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I²C bus. Use alternate pins if you encounter issues.
17. Alternate SPI clock.
18. The internal pull down is 5KOhm.
19. All VSS pins should be brought out to one common GND plane.

Figure 4. CY8C20337, CY8C20347/S Device


Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x37/47/67/S PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at <http://www.cypress.com/psoc>.



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	-55	+25	+125	°C
V _{DD}	Supply voltage relative to V _{SS}	—	-0.5	—	+6.0	V
V _{IO}	DC input voltage	—	V _{SS} - 0.5	—	V _{DD} + 0.5	V
V _{IOZ}	DC voltage applied to tristate	—	V _{SS} - 0.5	—	V _{DD} + 0.5	V
I _{MIO}	Maximum current into any port pin	—	-25	—	+50	mA
ESD	Electro static discharge voltage	Human body model ESD	2000	—	—	V
LU	Latch up current	In accordance with JESD78 standard	—	—	200	mA

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T _A	Ambient temperature	—	-40	—	+85	°C
T _C	Commercial temperature range	—	0	—	70	°C
T _J	Operational die temperature	The temperature rise from ambient to junction is package specific. See the Thermal Impedances on page 30 . The user must limit the power consumption to comply with this requirement.	-40	—	+100	°C

Table 11. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V _{OH1}	High output voltage Port 2 or 3 pins	I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH2}	High output voltage Port 2 or 3 Pins	I _{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.40	–	–	V
V _{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.50	–	–	V
V _{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I _{OH} < 10 μA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V _{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I _{OH} = 1 mA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V _{OL}	Low output voltage	I _{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V _{IL}	Input low voltage	–	–	–	0.72	V
V _{IH}	Input high voltage	–	V _{DD} × 0.65	–	V _{DD} + 0.7	V
V _H	Input hysteresis voltage	–	–	80	–	mV
I _{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C _{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
V _{ILLVT2.5}	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	V	–	
V _{IHLVT2.5}	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2		–	V

Table 12. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V _{OH1}	High output voltage Port 2 or 3 pins	I _{OH} = 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH2}	High output voltage Port 2 or 3 pins	I _{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.50	–	–	V
V _{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I _{OH} = 100 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH4}	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.50	–	–	V

Comparator User Module Electrical Specifications

Table 16 lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$.

Table 16. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset	–	Valid from 0.2 V to 1.5 V	–	2.5	30	mV
Current	–	Average DC current, 50 mV overdrive	–	20	80	μA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range	–	–	0.2		1.5	V

ADC Electrical Specifications

Table 17. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	V_{REFADC}	V
C_{IIN}	Input capacitance	–	–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	$1/(500\text{fF} \times \text{data clock})$	$1/(400\text{fF} \times \text{data clock})$	$1/(300\text{fF} \times \text{data clock})$	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications on page 21 for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = $0.001/(2^{\text{Resolution}}/\text{Data Clock})$	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = $0.001/(2^{\text{resolution}}/\text{data clock})$	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8, 9, or 10 bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR ($V_{DD} > 3.0\text{ V}$)	–	24	–	dB
		PSRR ($V_{DD} < 3.0\text{ V}$)	–	30	–	dB

DC POR and LVD Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{POR0}	1.66 V selected in PSoC Designer	V _{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V _{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	V
V _{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	V
V _{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	V
V _{LVD0}	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V _{LVD1}	2.71 V selected in PSoC Designer		2.64 ^[46]	2.71	2.78	V
V _{LVD2}	2.92 V selected in PSoC Designer		2.85 ^[47]	2.92	2.99	V
V _{LVD3}	3.02 V selected in PSoC Designer		2.95 ^[48]	3.02	3.09	V
V _{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	V
V _{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	V
V _{LVD6}	1.80 V selected in PSoC Designer		1.75 ^[49]	1.80	1.84	V
V _{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	V

DC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{DDIWRITE}	Supply voltage for flash write operations	–	1.71	–	5.25	V
I _{DDP}	Supply current during programming or verify	–	–	5	25	mA
V _{ILP}	Input low voltage during programming or verify	See appropriate “DC GPIO Specifications” on page 15	–	–	V _{IL}	V
V _{IHP}	Input high voltage during programming or verify	See appropriate “DC GPIO Specifications” on page 15	V _{IH}	–	–	V
I _{ILP}	Input current when Applying V _{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I _{IHP}	Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V _{OLP}	Output low voltage during programming or verify	–	–	–	V _{SS} + 0.75	V
V _{OHP}	Output high voltage during programming or verify	See appropriate “DC GPIO Specifications” on page 15. For V _{DD} > 3V use V _{OH4} in Table 10 on page 15.	V _{OH}	–	V _{DD}	V
Flash _{ENPB}	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
Flash _{DR}	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

Notes

46. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
 47. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
 48. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
 49. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

AC Chip-Level Specifications

Table 24 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 24. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{IMO24}	IMO frequency at 24 MHz Setting	—	22.8	24	25.2	MHz
F _{IMO12}	IMO frequency at 12 MHz setting	—	11.4	12	12.6	MHz
F _{IMO6}	IMO frequency at 6 MHz setting	—	5.7	6.0	6.3	MHz
F _{CPU}	CPU frequency	—	0.75	—	25.20	MHz
F _{32K1}	ILO frequency	—	15	32	50	kHz
F _{32K_U}	ILO untrimmed frequency	—	—	32	—	kHz
DC _{IMO}	Duty cycle of IMO	—	40	50	60	%
DC _{ILO}	ILO duty cycle	—	40	50	60	%
SR _{POWER_UP}	Power supply slew rate	V _{DD} slew rate during power-up	—	—	250	V/ms
t _{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	—	—	ms
t _{XRST2}	External reset pulse width after power-up ^[52]	Applies after part has booted	10	—	—	μs
t _{JIT_IMO} ^[53]	6 MHz IMO cycle-to-cycle jitter (RMS)	—	—	0.7	6.7	ns
	6 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	—	—	4.3	29.3	ns
	6 MHz IMO period jitter (RMS)	—	—	0.7	3.3	ns
	12 MHz IMO cycle-to-cycle jitter (RMS)	—	—	0.5	5.2	ns
	12 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	—	—	2.3	5.6	ns
	12 MHz IMO period jitter (RMS)	—	—	0.4	2.6	ns
	24 MHz IMO cycle-to-cycle jitter (RMS)	—	—	1.0	8.7	ns
	24 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	—	—	1.4	6.0	ns
	24 MHz IMO period jitter (RMS)	—	—	0.6	4.0	ns

Note

52. The minimum required XRES pulse length is longer when programming the device (see Table 28 on page 23).

53. See the Cypress Jitter Specifications application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information.

AC Programming Specifications

Figure 10. AC Waveform

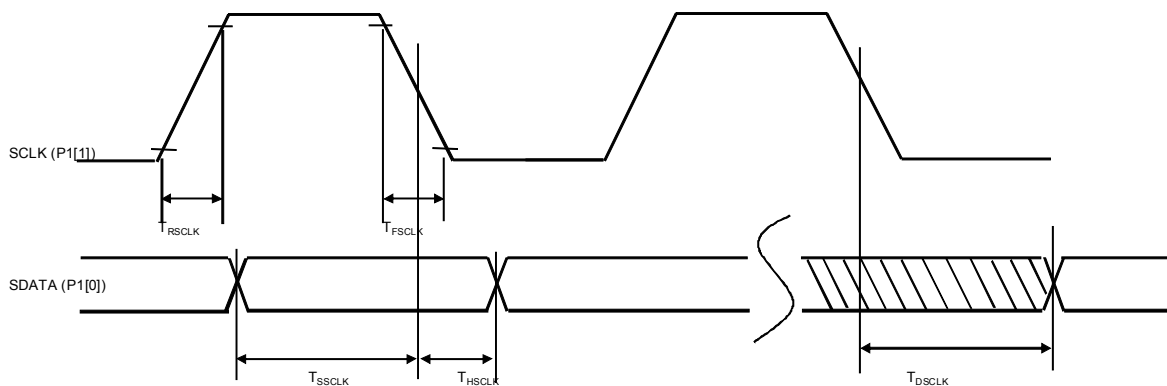


Table 28 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 28. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{RSCLK}	Rise time of SCLK	—	1	—	20	ns
t_{FSCLK}	Fall time of SCLK	—	1	—	20	ns
t_{SSCLK}	Data setup time to falling edge of SCLK	—	40	—	—	ns
t_{HSCLK}	Data hold time from falling edge of SCLK	—	40	—	—	ns
F_{SCLK}	Frequency of SCLK	—	0	—	8	MHz
t_{ERASEB}	Flash erase time (block)	—	—	—	18	ms
t_{WRITE}	Flash block write time	—	—	—	25	ms
t_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	—	—	60	ns
t_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \leq V_{DD} \leq 3.6$	—	—	85	ns
t_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \leq V_{DD} \leq 3.0$	—	—	130	ns
t_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	—	—	μ s
t_{XRES}	XRES pulse length	—	300	—	—	μ s
$t_{VDDWAIT}^{[54]}$	V_{DD} stable to wait-and-poll hold off	—	0.1	—	1	ms
$t_{VDDXRES}^{[54]}$	V_{DD} stable to XRES assertion delay	—	14.27	—	—	ms
t_{POLL}	SDAT high pulse time	—	0.01	—	200	ms
$t_{ACQ}^{[54]}$	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.	—	3.20	—	19.60	ms
$t_{XRESINI}^{[54]}$	“Key window” time after an XRES event, based on 8 ILO clocks	—	98	—	615	μ s

Note

54. Valid from 5 to 50 °C. See the spec, [CY8C20X66](#), [CY8C20X46](#), [CY8C20X36](#), [CY7C643XX](#), [CY7C604XX](#), [CY8CTST2XX](#), [CY8CTMG2XX](#), [CY8C20X67](#), [CY8C20X47](#), [CY8C20X37](#), [Programming Spec](#) for more details.

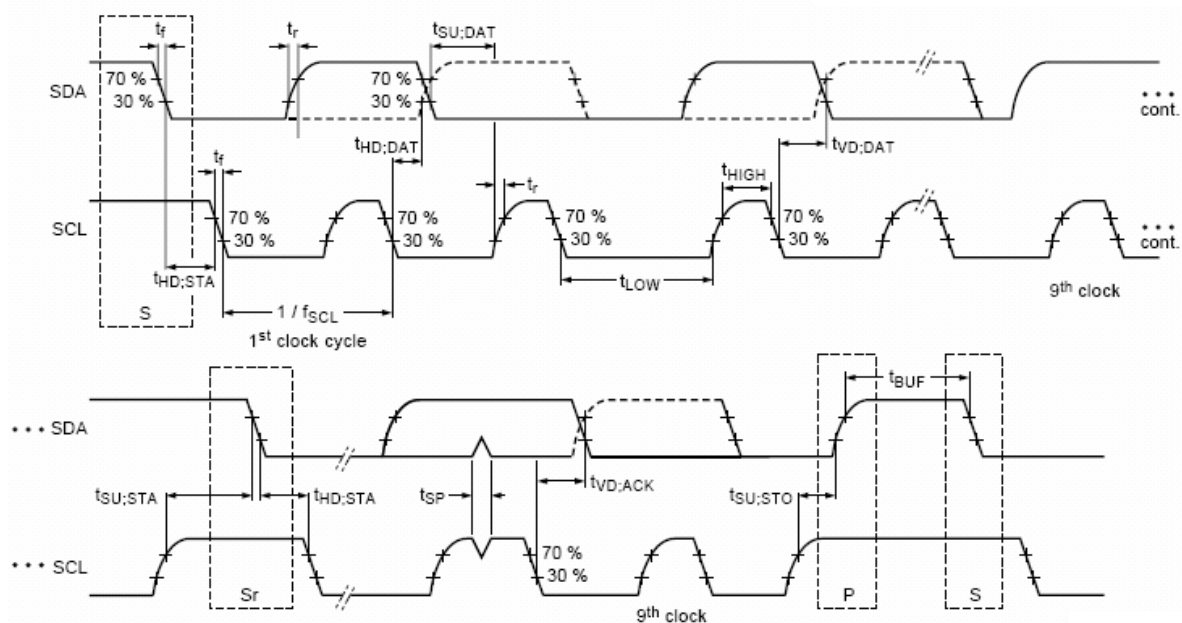
AC I²C Specifications

Table 29 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	μ s
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	μ s
t_{HIGH}	HIGH Period of the SCL clock	4.0	–	0.6	–	μ s
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	–	0.6	–	μ s
$t_{HD;DAT}^{[55]}$	Data hold time	20	3.45	20	0.90	μ s
$t_{SU;DAT}$	Data setup time	250	–	100 ^[56]	–	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	–	0.6	–	μ s
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	μ s
t_{SP}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 11. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

55. **Errata:** To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. For more information see item #5 in the "Errata" on page 37.
56. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Table 30. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	– –	– –	6 3	MHz MHz
DC	SCLK duty cycle	–	–	50	–	%
t_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	60 100	– –	– –	ns ns
t_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
t_{OUT_H}	MOSI high time	–	40	–	–	ns

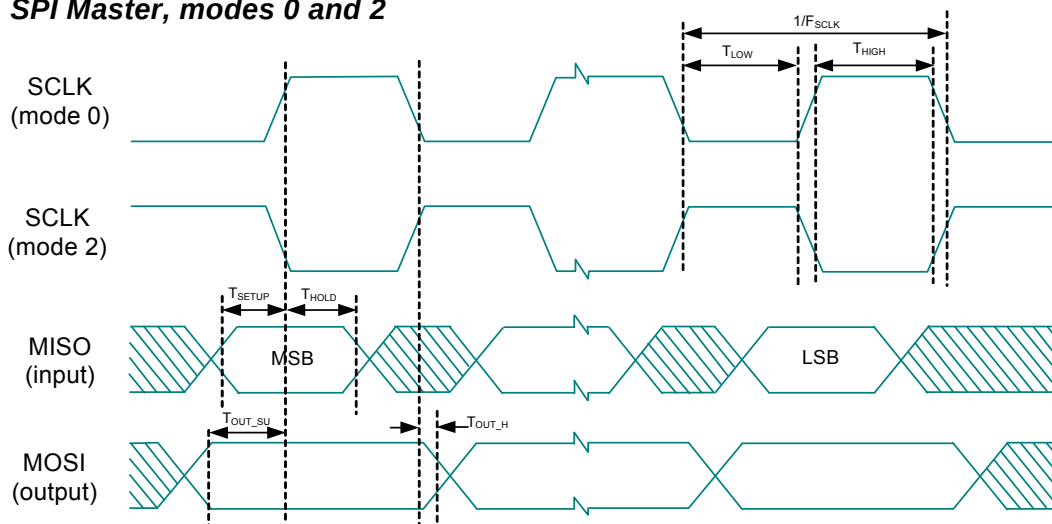
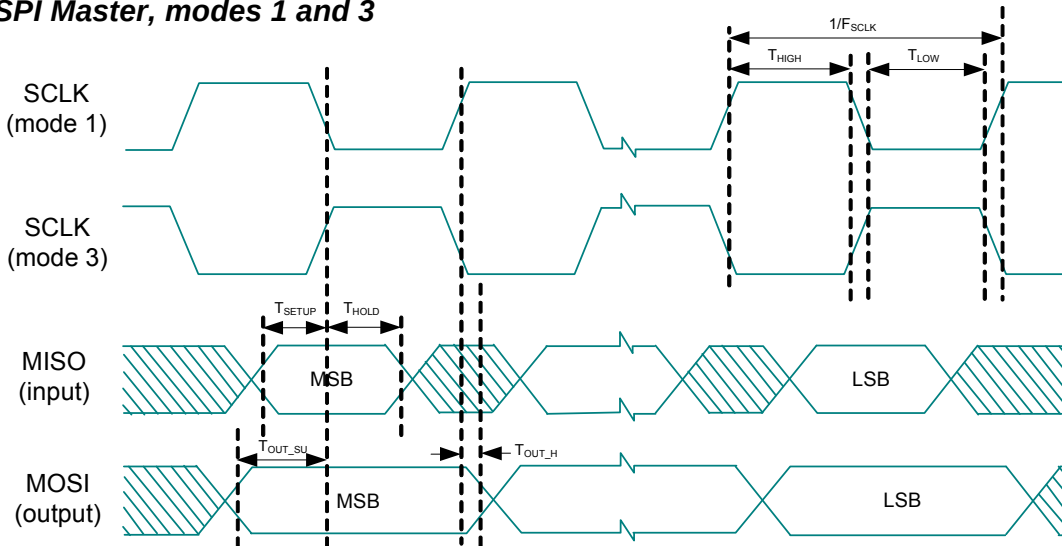
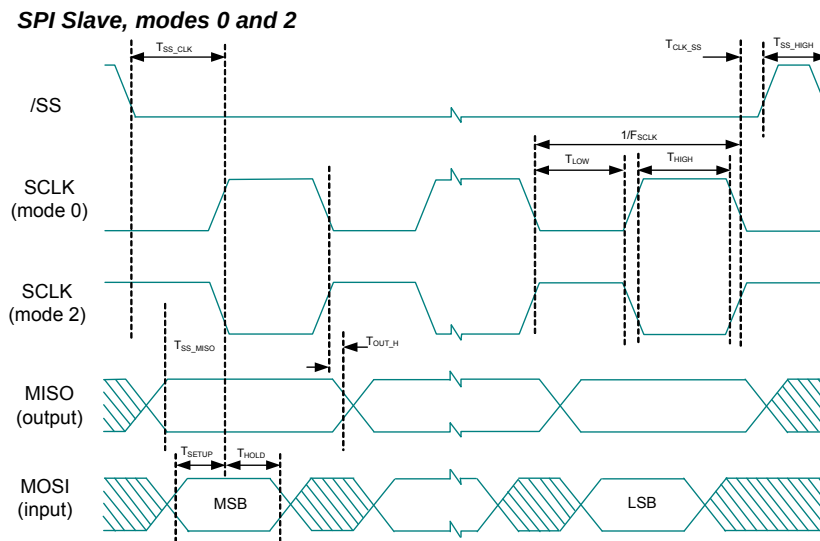
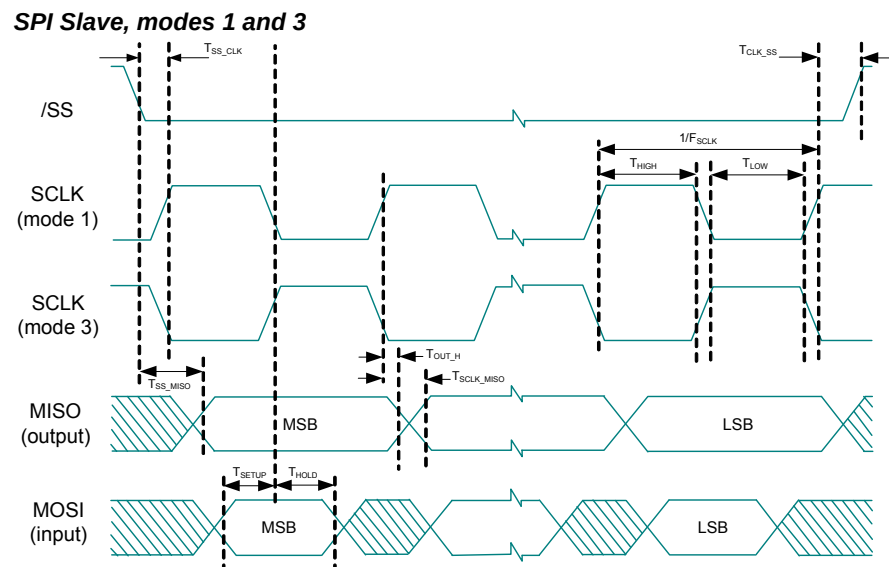
Figure 12. SPI Master Mode 0 and 2
SPI Master, modes 0 and 2

Figure 13. SPI Master Mode 1 and 3
SPI Master, modes 1 and 3


Table 31. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	—	—	—	4	MHz
t_{LOW}	SCLK low time	—	42	—	—	ns
t_{HIGH}	SCLK high time	—	42	—	—	ns
t_{SETUP}	MOSI to SCLK setup time	—	30	—	—	ns
t_{HOLD}	SCLK to MOSI hold time	—	50	—	—	ns
t_{SS_MISO}	SS high to MISO valid	—	—	—	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	—	—	—	125	ns
t_{SS_HIGH}	SS high time	—	50	—	—	ns
t_{SS_CLK}	Time from SS low to first SCLK	—	$2/SCLK$	—	—	ns
t_{CLK_SS}	Time from last SCLK to SS high	—	$2/SCLK$	—	—	ns

Figure 14. SPI Slave Mode 0 and 2

Figure 15. SPI Slave Mode 1 and 3


Packaging Information

This section illustrates the packaging specifications for the CY8C20x37/47/67 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

Figure 16. 16-pin (150 Mil) SOIC

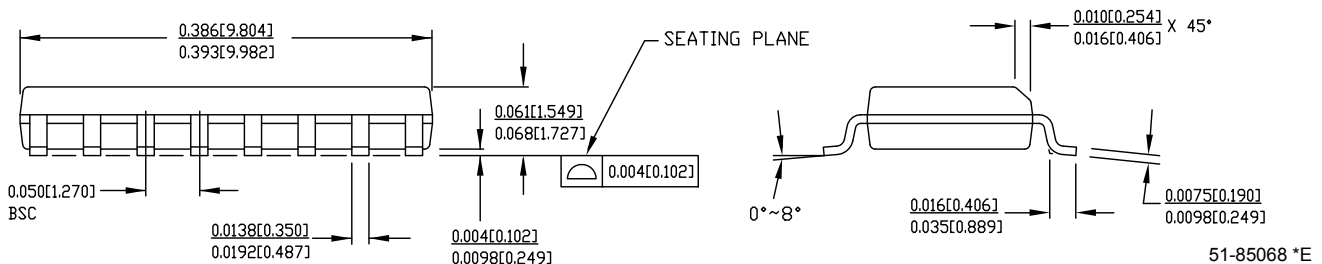
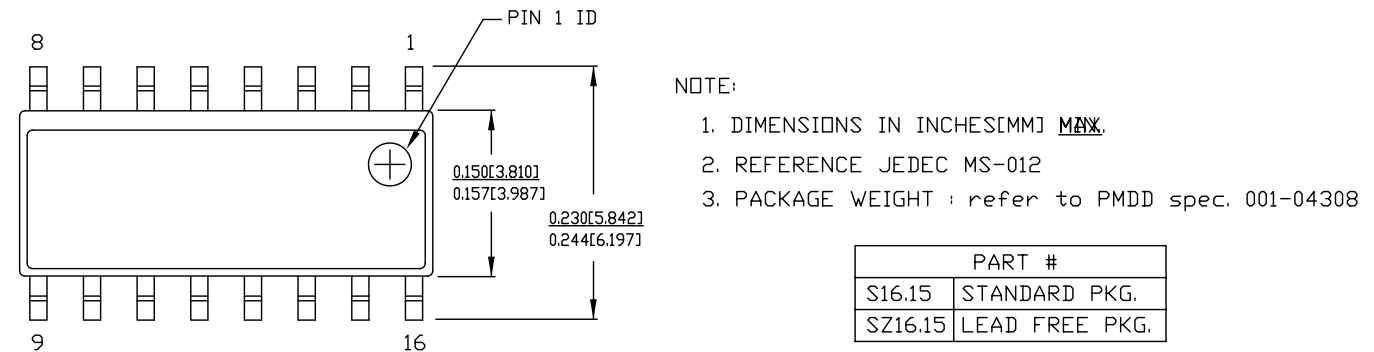
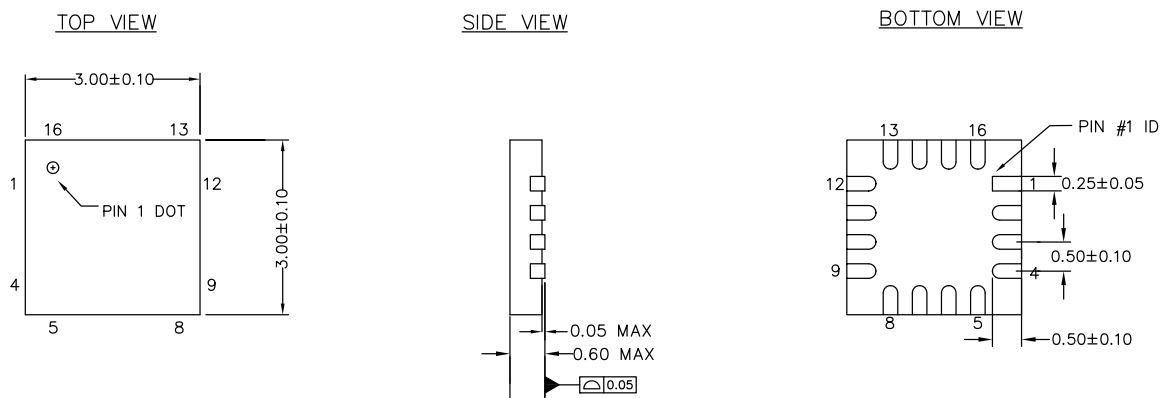


Figure 17. 16-pin Chip-On-Lead (3 × 3 × 0.6 mm) (Sawn) Package Outline, 001-09116



NOTES

1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

Ordering Information

Table 35 lists the CY8C20x37/47/67/S PSoC devices' key package features and ordering codes.

Table 35. PSoC Device Key Features and Ordering Information

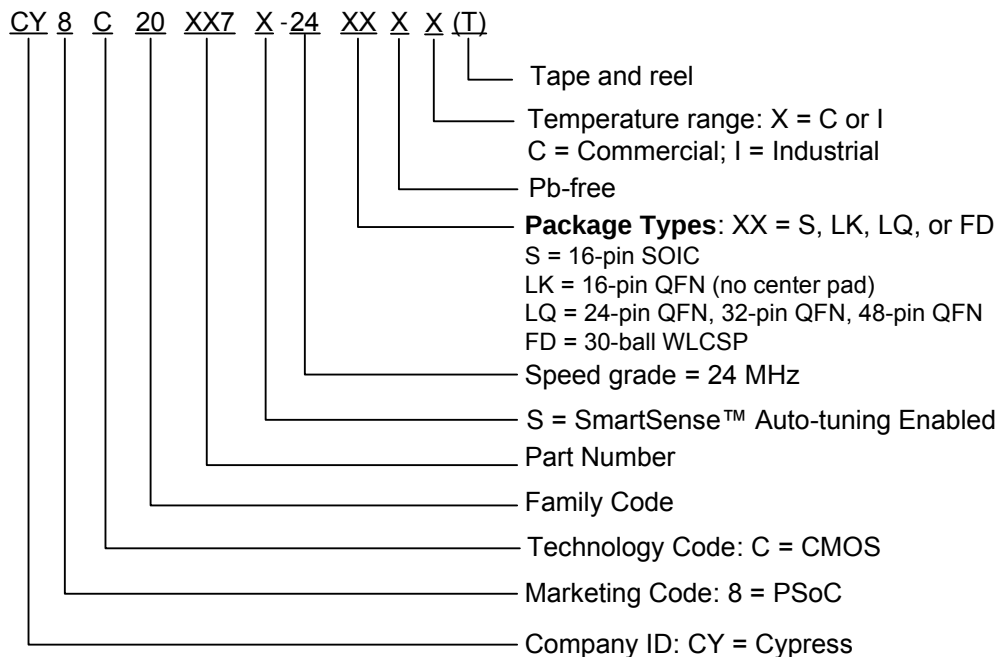
Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	CapSense Sensors	Digital I/O Pins	Analog Inputs ^[59]	XRES Pin	ADC
CY8C20237-24SXI	16-pin SOIC	8 K	1 K	10	13	13	Yes	Yes
CY8C20247S-24SXI	16-pin SOIC	16 K	2 K	10	13	13	Yes	Yes
CY8C20237-24LKXI	16-pin QFN	8 K	1 K	10	13	13	Yes	Yes
CY8C20237-24LKXIT	16-pin QFN (Tape and Reel)	8 K	1 K	10	13	13	Yes	Yes
CY8C20247S-24LKXI	16-pin QFN	16 K	2 K	10	13	13	Yes	Yes
CY8C20247S-24LKXIT	16-pin QFN (Tape and Reel)	16 K	2 K	10	13	13	Yes	Yes
CY8C20337-24LQXI	24-pin QFN	8 K	1 K	16	19	19	Yes	Yes
CY8C20337-24LQXIT	24-pin QFN (Tape and Reel)	8 K	1 K	16	19	19	Yes	Yes
CY8C20347-24LQXI	24-pin QFN	16 K	2 K	16	19	19	Yes	Yes
CY8C20347-24LQXIT	24-pin QFN (Tape and Reel)	16 K	2 K	16	19	19	Yes	Yes
CY8C20347S-24LQXI	24-pin QFN	16 K	2 K	16	19	19	Yes	Yes
CY8C20347S-24LQXIT	24-pin QFN (Tape and Reel)	16 K	2 K	16	19	19	Yes	Yes
CY8C20437-24LQXI	32-pin QFN	8 K	1 K	25	28	28	Yes	Yes
CY8C20437-24LQXIT	32-pin QFN (Tape and Reel)	8 K	1 K	25	28	28	Yes	Yes
CY8C20447-24LQXI	32-pin QFN	16 K	2 K	25	28	28	Yes	Yes
CY8C20447-24LQXIT	32-pin QFN (Tape and Reel)	16 K	2 K	25	28	28	Yes	Yes
CY8C20447S-24LQXI	32-pin QFN	16 K	2 K	25	28	28	Yes	Yes
CY8C20447S-24LQXIT	32-pin QFN (Tape and Reel)	16 K	2 K	25	28	28	Yes	Yes
CY8C20467-24LQXI	32-pin QFN	32 K	2 K	25	28	28	Yes	Yes
CY8C20467-24LQXIT	32-pin QFN (Tape and Reel)	32 K	2 K	25	28	28	Yes	Yes
CY8C20467S-24LQXI	32-pin QFN	32 K	2 K	25	28	28	Yes	Yes
CY8C20467S-24LQXIT	32-pin QFN (Tape and Reel)	32 K	2 K	25	28	28	Yes	Yes
CY8C20637-24LQXI	48-pin QFN	8 K	1 K	31	34	34	Yes	Yes
CY8C20637-24LQXIT	48-pin QFN (Tape and Reel)	8 K	1 K	31	34	34	Yes	Yes
CY8C20647-24LQXI	48-pin QFN	16 K	2 K	31	34	34	Yes	Yes
CY8C20647-24LQXIT	48-pin QFN (Tape and Reel)	16 K	2 K	31	34	34	Yes	Yes
CY8C20647S-24LQXI	48-pin QFN	16 K	2 K	31	34	34	Yes	Yes
CY8C20647S-24LQXIT	48-pin QFN (Tape and Reel)	16 K	2 K	31	34	34	Yes	Yes
CY8C20667-24LQXI	48-pin QFN	32 K	2 K	31	34	34	Yes	Yes
CY8C20667-24LQXIT	48-pin QFN (Tape and Reel)	32 K	2 K	31	34	34	Yes	Yes
CY8C20667S-24LQXI	48-pin QFN	32 K	2 K	31	34	34	Yes	Yes
CY8C20667S-24LQXIT	48-pin QFN (Tape and Reel)	32 K	2 K	31	34	34	Yes	Yes

Note

⁵⁹. Dual-function Digital I/O Pins also connect to the common analog mux.

Table 35. PSoC Device Key Features and Ordering Information *(continued)*

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	CapSense Sensors	Digital I/O Pins	Analog Inputs ^[59]	XRES Pin	ADC
CY8C20767-24FDXC	30-pin WLCSP	32 K	2 K	24	27	27	Yes	Yes
CY8C20767-24FDXCT	30-pin WLCSP (Tape and Reel)	32 K	2 K	24	27	27	Yes	Yes

Ordering Code Definitions


6. I2C Port Pin Pull-up Supply Voltage

■Problem Definition

Pull-up resistor on I2C interface cannot be connected to a supply voltage that is greater than 0.7 V of CY8C20xx7/S V_{DD} .

■Parameters Affected

None.

■Trigger Condition(S)

This problem occurs only when the I2C master is powered at a higher voltage than CY8C20xx7/S.

■Scope of Impact

This trigger condition will corrupt the I2C communication between the I2C host and the CY8C20xx7/S CapSense controller.

■Workaround

I2C master cannot be powered at a supply voltage that is greater than 0.7 V compared to CY8C20xx7/S supply voltage.

■Fix Status

Will not be fixed

■Changes

None

7. Port1 Pin Voltage

■Problem Definition

Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C20xx7/S V_{DD} .

■Parameters Affected

None.

■Trigger Condition(S)

This problem occurs only when port1 pins are at voltage 0.7 V higher than V_{DD} of CY8C20xx7/S.

■Scope of Impact

This trigger condition will not allow CY8C20xx7/S to drive the output signal on port1 pins, input path is unaffected by this condition.

■Workaround

Port1 should not be connected to a higher voltage than V_{DD} of CY8C20xx7/S.

■Fix Status

Will not be fixed

■Changes

None

Document History Page

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3276782	DST	06/27/2011	New silicon and document
*A	3327230	DST	07/28/2011	Changed 48-pin dimensions to 6 × 6 × 0.6 mm QFN Updated pins name in Table 3 on page 9 and removed USB column and updated dimensions for 48-pin parts in Table 35 on page 33 Updated Figure 20 on page 29 Removed ICE and Debugger sections. Removed CY3215 Development Kit and CY3280-20x66 UCC sections. Updated Ordering Information .
*B	3403111	YVA	10/12/2011	Moved status from Advance to Preliminary. Updated Ordering Information Removed the row named "48-Pin (6 × 6 mm) QFN (OCD)". Changed all 48-pin ordering code column from CY8C20XXX-24LTxx to CY8C20XXX-24LQxx. Updated 16-pin SOIC and 16-pin QFN package drawings.
*C	3473317	DST	12/23/2011	Updated Features . Updated Pinouts (Removed PSoC in captions of Figure 2 , Figure 3 , Figure 4 , Figure 6 , and Figure 7). Updated DC Chip-Level Specifications under Electrical Specifications (Updated typical value of I _{DD24} parameter from 3.32 mA to 2.88 mA, updated typical value of I _{DD12} parameter from 1.86 mA to 1.71 mA, updated typical value of I _{DD6} parameter from 1.13 mA to 1.16 mA, updated maximum value of I _{SB0} parameter from 0.50 µA to 1.1 µA, added I _{SB12C} parameter and its details). Updated DC GPIO Specifications under Electrical Specifications (Added the parameters namely V _{ILLVT3.3} , V _{IHLVT3.3} , V _{ILLVT5.5} , V _{IHLVT5.5} and their details in Table 10 , added the parameters namely V _{ILLVT2.5} , V _{IHLVT2.5} and their details in Table 11). Added the following sections namely DC I2C Specifications , Shield Driver DC Specifications , and DC IDAC Specifications under Electrical Specifications . Updated AC Chip-Level Specifications (Added the parameter namely t _{JIT_IMO} and its details). Updated Ordering Information (updated Table 35).
*D	3510277	YVA/DST	02/16/2012	Added CY8C20x37/37S/47/47S/67/67S part numbers and changed title to "1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders" Updated Features . Modified comparator blocks in Logic Block Diagram . Replaced SmartSense with SmartSense auto-tuning. Added CY8C20xx7S part numbers in Pin Definitions. Added footnote for Table 20 . Updated Table 21 and Table 22 and added Table 23 . Updated F _{32K1} min value. Updated data hold time min values. Updated CY8C206x7 part information in Table "Emulation and Programming Accessories". Updated Ordering Information .
*E	3539259	DST	03/01/2012	Changed Datasheet status from Preliminary to Final. Updated all Pinouts to include Driven Shield Output (optional) information. Updated Min value for V _{LPC} Table 15 . Updated Offset and Input range in Table 16 .

Document History Page *(continued)*

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*O	5122184	JFMD	02/02/2016	Updated Features : Removed Note "Please contact your nearest sales office for additional details." and its reference. Updated Ordering Information : Updated Table 35 : Updated part numbers.