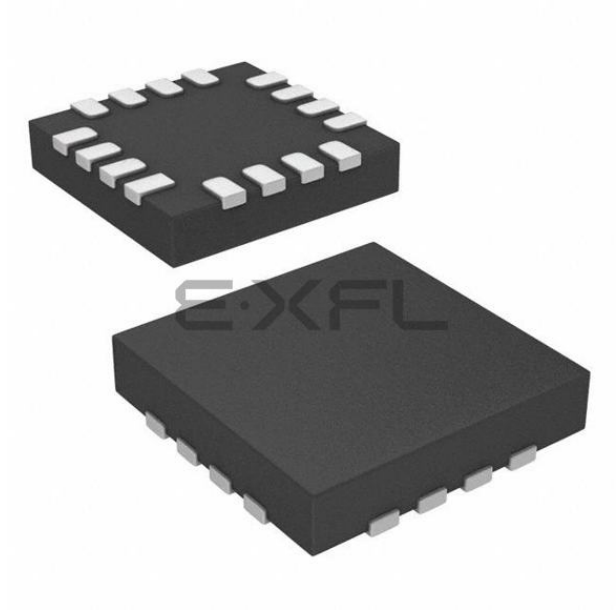

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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Active |
| Applications | Capacitive Sensing |
| Core Processor | M8C |
| Program Memory Type | FLASH (16kB) |
| Controller Series | CY8C20xx7/S |
| RAM Size | 2K x 8 |
| Interface | I²C, SPI |
| Number of I/O | 13 |
| Voltage - Supply | 1.71V ~ 5.5V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 16-UFQFN |
| Supplier Device Package | 16-QFN (3x3) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20247s-24lkxi |

## Contents

### Additional System Resources

System resources provide additional capability, such as configurable $I^2C$ slave, SPI master/slave communication interface, three 16-bit programmable timers, various system resets supported by the M8C low voltage detection and power-on reset. The merits of each system resource are listed here:

- The $I^2C$ slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The $I^2C$ hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The $I^2C$ enhanced slave interface appears as a 32-byte RAM buffer to the external $I^2C$ master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For more details, refer to the I2CSBUF User Module datasheet.
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

## Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20x37/47/67/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

### Application Notes/Design Guides

Application notes and design guides are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/gocapsense. Select Application Notes under the Related Documentation tab.

### Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. See “Development Kits” on page 31.

### Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

### CYPros Consultants

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## Designing with PSoC Designer

The PSoC development process can be summarized in the following four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate and Verify

### Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

### 30-ball WLCSP (24 Sensing Inputs)

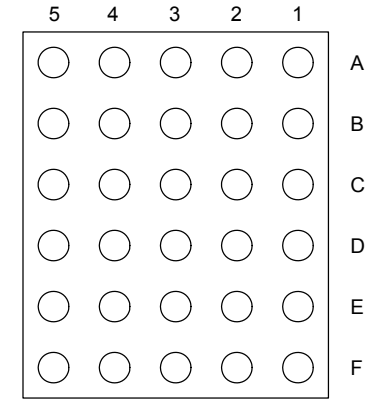
**Table 4. Pin Definitions – CY8C20767, CY8C20747 30-ball Part Pinout (WLCSP)** [20]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| A1 | IOH | I | P0[2] | Driven Shield Output (optional) |
| A2 | IOH | I | P0[6] | |
| A3 | Power | | $V_{DD}$ | Supply voltage |
| A4 | IOH | I | P0[1] | Integrating Input |
| A5 | I/O | I | P2[7] | |
| B1 | I/O | I | P4[2] | |
| B2 | IOH | I | P0[0] | Driven Shield Output (optional) |
| B3 | IOH | I | P0[4] | |
| B4 | IOH | I | P0[3] | Integrating Input |
| B5 | I/O | I | P2[5] | Crystal Output (Xout) |
| C1 | I/O | I | P2[2] | Driven Shield Output (optional) |
| C2 | I/O | I | P2[4] | Driven Shield Output (optional) |
| C3 | I/O | I | P0[7] | |
| C4 | IOH | I | P3[2] | |
| C5 | I/O | I | P2[3] | Crystal Input (Xin) |
| D1 | I/O | I | P2[0] | |
| D2 | I/O | I | P3[0] | |
| D3 | I/O | I | P3[1] | |
| D4 | I/O | I | P3[3] | |
| D5 | I/O | I | P2[1] | |
| E1 | Input | | XRES | Active high external reset with internal pull-down[21] |
| E2 | IOHR | I | P1[6] | |
| E3 | IOHR | I | P1[4] | Optional external clock input (EXT CLK) |
| E4 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| E5 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| F1 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| F2 | IOHR | I | P1[0] | ISSP DATA[22], $I^2C$ SDA, SPI CLK[23] |
| F3 | Power | | $V_{SS}$ | Supply ground[24] |
| F4 | IOHR | I | P1[1] | ISSP CLK[22], $I^2C$ SCL, SPI MOSI |
| F5 | IOHR | I | P1[3] | SPI CLK |

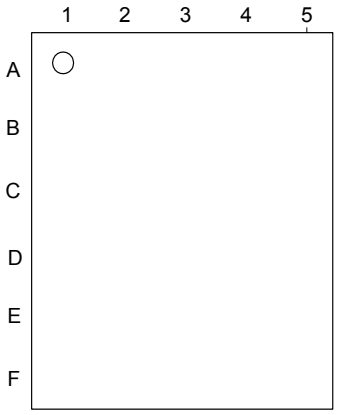
**LEGEND:** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

**Figure 5. CY8C20767, CY8C20747 30-ball WLCSP**

**Bottom View**




**Top View**




**Notes**

20. 27 GPIOs = 24 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
21. The internal pull down is 5KOhm.
22. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
23. Alternate SPI clock.
24. All VSS pins should be brought out to one common GND plane.

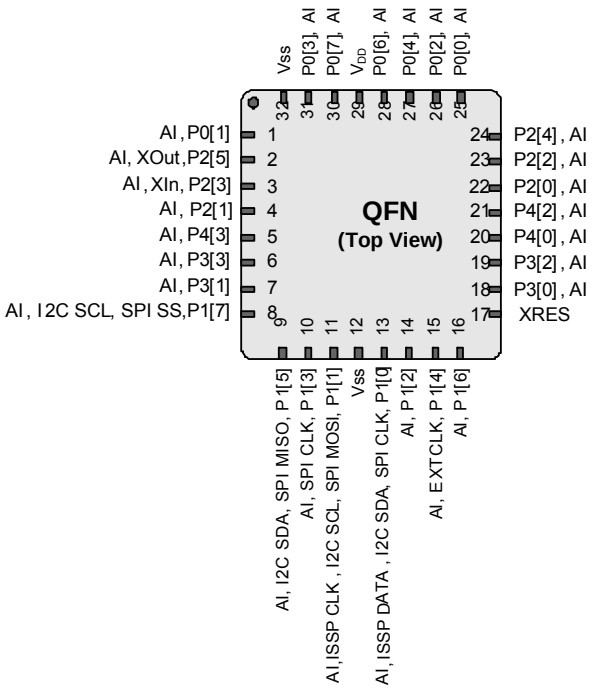
## 32-pin QFN (25 Sensing Inputs)[25]

**Table 5. Pin Definitions – CY8C20437, CY8C20447/S, CY8C20467/S** [26]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IOH | I | P0[1] | Integrating input |
| 2 | I/O | I | P2[5] | Crystal output (XOut) |
| 3 | I/O | I | P2[3] | Crystal input (XIn) |
| 4 | I/O | I | P2[1] | |
| 5 | I/O | I | P4[3] | |
| 6 | I/O | I | P3[3] | |
| 7 | I/O | I | P3[1] | |
| 8 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| 9 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| 10 | IOHR | I | P1[3] | SPI CLK. |
| 11 | IOHR | I | P1[1] | ISSP CLK[27], $I^2C$ SCL, SPI MOSI. |
| 12 | Power | | $V_{SS}$ | Ground connection[30] |
| 13 | IOHR | I | P1[0] | ISSP DATA[27], $I^2C$ SDA, SPI CLK[28] |
| 14 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 15 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 16 | IOHR | I | P1[6] | |
| 17 | Input | | XRES | Active high external reset with internal pull-down[29] |
| 18 | I/O | I | P3[0] | |
| 19 | I/O | I | P3[2] | |
| 20 | I/O | I | P4[0] | |
| 21 | I/O | I | P4[2] | |
| 22 | I/O | I | P2[0] | |
| 23 | I/O | I | P2[2] | Driven Shield Output (optional) |
| 24 | I/O | I | P2[4] | Driven Shield Output (optional) |
| 25 | IOH | I | P0[0] | Driven Shield Output (optional) |
| 26 | IOH | I | P0[2] | Driven Shield Output (optional) |
| 27 | IOH | I | P0[4] | |
| 28 | IOH | I | P0[6] | |
| 29 | Power | | $V_{DD}$ | |
| 30 | IOH | I | P0[7] | |
| 31 | IOH | I | P0[3] | Integrating input |
| 32 | Power | | $V_{SS}$ | Ground connection[30] |
| CP | Power | | $V_{SS}$ | Center pad must be connected to ground |

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 6. CY8C20437, CY8C20447/S, CY8C20467/S Device**



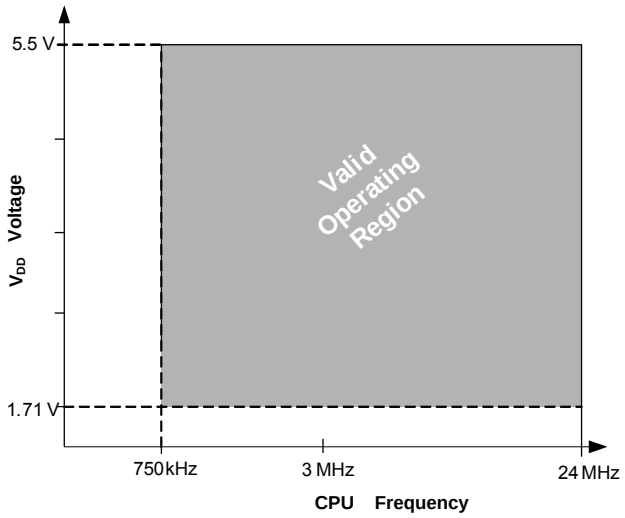

**Notes**

25. The center pad (CP) on the QFN package must be connected to ground ($V_{SS}$) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
26. 28 GPIOs = 25 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
27. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
28. Alternate SPI clock.
29. The internal pull down is 5KOhm.
30. All VSS pins should be brought out to one common GND plane.

## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x37/47/67/S PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at http://www.cypress.com/psoc.

**Figure 8. Voltage versus CPU Frequency**




### Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 7. Absolute Maximum Ratings**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability. | –55 | +25 | +125 | °C |
| $V_{DD}$ | Supply voltage relative to $V_{SS}$ | – | –0.5 | – | +6.0 | V |
| $V_{IO}$ | DC input voltage | – | $V_{SS}$ – 0.5 | – | $V_{DD}$ + 0.5 | V |
| $V_{IOZ}$ | DC voltage applied to tristate | – | $V_{SS}$ – 0.5 | – | $V_{DD}$ + 0.5 | V |
| $I_{MIO}$ | Maximum current into any port pin | – | –25 | – | +50 | mA |
| ESD | Electro static discharge voltage | Human body model ESD | 2000 | – | – | V |
| LU | Latch up current | In accordance with JESD78 standard | – | – | 200 | mA |

### Operating Temperature

**Table 8. Operating Temperature**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | – | –40 | – | +85 | °C |
| $T_C$ | Commercial temperature range | – | 0 | | 70 | °C |
| $T_J$ | Operational die temperature | The temperature rise from ambient to junction is package specific. See the Thermal Impedances on page 30. The user must limit the power consumption to comply with this requirement. | –40 | – | +100 | °C |

**Table 11. 2.4 V to 3.0 V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| $V_{OH1}$ | High output voltage Port 2 or 3 pins | $I_{OH}$ < 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.20 | – | – | V |
| $V_{OH2}$ | High output voltage Port 2 or 3 Pins | $I_{OH}$ = 0.2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.40 | – | – | V |
| $V_{OH3}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | $I_{OH}$ < 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.20 | – | – | V |
| $V_{OH4}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | $I_{OH}$ = 2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.50 | – | – | V |
| $V_{OH5A}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | $I_{OH}$ < 10 µA, $V_{DD}$ > 2.4 V, maximum of 20 mA source current in all I/Os | 1.50 | 1.80 | 2.10 | V |
| $V_{OH6A}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | $I_{OH}$ = 1 mA, $V_{DD}$ > 2.4 V, maximum of 20 mA source current in all I/Os | 1.20 | – | – | V |
| $V_{OL}$ | Low output voltage | $I_{OL}$ = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| $V_{IL}$ | Input low voltage | – | – | – | 0.72 | V |
| $V_{IH}$ | Input high voltage | – | $V_{DD}$ × 0.65 | – | $V_{DD}$ + 0.7 | V |
| $V_H$ | Input hysteresis voltage | – | – | 80 | – | mV |
| $I_{IL}$ | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| $C_{PIN}$ | Capacitive load on pins | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |
| $V_{ILLVT2.5}$ | Input Low Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 0.7 | V | – | |
| $V_{IHLVT2.5}$ | Input High Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 1.2 | | – | V |

**Table 12. 1.71 V to 2.4 V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| $V_{OH1}$ | High output voltage Port 2 or 3 pins | $I_{OH}$ = 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH2}$ | High output voltage Port 2 or 3 pins | $I_{OH}$ = 0.5 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.50 | – | – | V |
| $V_{OH3}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | $I_{OH}$ = 100 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH4}$ | High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | $I_{OH}$ = 2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.50 | – | – | V |

**Table 12. 1.71 V to 2.4 V DC GPIO Specifications** *(continued)*

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Low output voltage | $I_{OL}$ = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.40 | V |
| $V_{IL}$ | Input low voltage | – | – | – | 0.30 × $V_{DD}$ | V |
| $V_{IH}$ | Input high voltage | – | 0.65 × $V_{DD}$ | – | – | V |
| $V_H$ | Input hysteresis voltage | – | – | 80 | – | mV |
| $I_{IL}$ | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| $C_{PIN}$ | Capacitive load on pins | Package and pin dependent temp = 25 °C | 0.50 | 1.70 | 7 | pF |

**Table 13. GPIO Current Sink and Source Specifications**

| Supply Voltage | Mode | Port 0/1 per I/O (max) | Port 2/3/4 per I/O (max) | Total Current Even Pins (max) | Total Current Odd Pins (max) | Units |
|---|---|---|---|---|---|---|
| 1.71–2.4 | Sink | 5 | 5 | 20 | 30 | mA |
| | Source | 2 | 0.5 | 10[45] | | mA |
| 2.4–3.0 | Sink | 10 | 10 | 30 | 30 | mA |
| | Source | 2 | 0.2 | 10[45] | | mA |
| 3.0–5.0 | Sink | 25 | 25 | 60 | 60 | mA |
| | Source | 5 | 1 | 20[45] | | mA |

## DC Analog Mux Bus Specifications

Table 14 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 14. DC Analog Mux Bus Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{SW}$ | Switch resistance to common analog bus | – | – | – | 800 | Ω |
| $R_{GND}$ | Resistance of initialization switch to $V_{SS}$ | – | – | – | 800 | Ω |

The maximum pin voltage for measuring $R_{SW}$ and $R_{GND}$ is 1.8 V

## DC Low Power Comparator Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 15. DC Comparator Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{LPC}$ | Low power comparator (LPC) common mode | Maximum voltage limited to $V_{DD}$ | 0.2 | – | 1.8 | V |
| $I_{LPC}$ | LPC supply current | – | – | 10 | 80 | µA |
| $V_{OSLPC}$ | LPC voltage offset | – | – | 2.5 | 30 | mV |

**Note**
45. Total current (odd + even ports)

## Comparator User Module Electrical Specifications

Table 16 lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40 °C ≤ TA ≤ 85 °C, 1.71 V ≤ $V_{DD}$ ≤ 5.5 V.

**Table 16. Comparator User Module Electrical Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{COMP}$ | Comparator response time | 50 mV overdrive | – | 70 | 100 | ns |
| Offset | – | Valid from 0.2 V to 1.5 V | – | 2.5 | 30 | mV |
| Current | – | Average DC current, 50 mV overdrive | – | 20 | 80 | µA |
| PSRR | Supply voltage > 2 V | Power supply rejection ratio | – | 80 | – | dB |
| | Supply voltage < 2 V | Power supply rejection ratio | – | 40 | – | dB |
| Input range | – | – | 0.2 | | 1.5 | V |

## ADC Electrical Specifications

**Table 17. ADC User Module Electrical Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| $V_{IN}$ | Input voltage range | – | 0 | – | VREFADC | V |
| $C_{IIN}$ | Input capacitance | – | – | – | 5 | pF |
| $R_{IN}$ | Input resistance | Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution | 1/(500fF × data clock) | 1/(400fF × data clock) | 1/(300fF × data clock) | Ω |
| **Reference** | | | | | | |
| $V_{REFADC}$ | ADC reference voltage | – | 1.14 | – | 1.26 | V |
| **Conversion Rate** | | | | | | |
| $F_{CLK}$ | Data clock | Source is chip's internal main oscillator. See AC Chip-Level Specifications on page 21 for accuracy | 2.25 | – | 6 | MHz |
| S8 | 8-bit sample rate | Data clock set to 6 MHz. sample rate = 0.001/ (2^Resolution/Data Clock) | – | 23.43 | – | ksps |
| S10 | 10-bit sample rate | Data clock set to 6 MHz. sample rate = 0.001/ (2^resolution/data clock) | – | 5.85 | – | ksps |
| **DC Accuracy** | | | | | | |
| RES | Resolution | Can be set to 8, 9, or 10 bit | 8 | – | 10 | bits |
| DNL | Differential nonlinearity | – | –1 | – | +2 | LSB |
| INL | Integral nonlinearity | – | –2 | – | +2 | LSB |
| $E_{OFFSET}$ | Offset error | 8-bit resolution | 0 | 3.20 | 19.20 | LSB |
| | | 10-bit resolution | 0 | 12.80 | 76.80 | LSB |
| $E_{GAIN}$ | Gain error | For any resolution | –5 | – | +5 | %FSR |
| **Power** | | | | | | |
| $I_{ADC}$ | Operating current | – | – | 2.10 | 2.60 | mA |
| PSRR | Power supply rejection ratio | PSRR ($V_{DD}$ > 3.0 V) | – | 24 | – | dB |
| | | PSRR ($V_{DD}$ < 3.0 V) | – | 30 | – | dB |

## DC I²C Specifications

Table 20 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ $T_A$ ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 20. DC I²C Specifications**[50]

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{ILI2C}$ | Input low level | 3.1 V ≤ $V_{DD}$ ≤ 5.5 V | – | – | 0.25 × $V_{DD}$ | V |
| | | 2.5 V ≤ $V_{DD}$ ≤ 3.0 V | – | – | 0.3 × $V_{DD}$ | V |
| | | 1.71 V ≤ $V_{DD}$ ≤ 2.4 V | – | – | 0.3 × $V_{DD}$ | V |
| $V_{IHI2C}$ | Input high level | 1.71 V ≤ $V_{DD}$ ≤ 5.5 V | 0.65 × $V_{DD}$ | – | $V_{DD}$ + 0.7 V[51] | V |

## Shield Driver DC Specifications

Table 21 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ $T_A$ ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 21. Shield Driver DC Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{Ref}$ | Reference buffer output | 1.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.942 | – | 1.106 | V |
| $V_{RefHi}$ | Reference buffer output | 1.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.104 | – | 1.296 | V |

## DC IDAC Specifications

Table 22 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 22. DC IDAC Specifications (8-bit IDAC)**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| IDAC_DNL | Differential nonlinearity | –1 | – | 1 | LSB | – |
| IDAC_DNL | Integral nonlinearity | –2 | – | 2 | LSB | – |
| IDAC_Current | Range = 4x | 138 | – | 169 | µA | DAC setting = 127 dec |
| | Range = 8x | 138 | – | 169 | µA | DAC setting = 64 dec |

**Table 23. DC IDAC Specifications (7-bit IDAC)**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| IDAC_DNL | Differential nonlinearity | –1 | – | 1 | LSB | – |
| IDAC_DNL | Integral nonlinearity | –2 | – | 2 | LSB | – |
| IDAC_Current | Range = 4x | 137 | – | 168 | µA | DAC setting = 127 dec |
| | Range = 8x | 138 | – | 169 | µA | DAC setting = 64 dec |

**Notes**

50. Errata: Pull-up resistors on I2C interface cannot be connected to a supply voltage that is more than 0.7 V higher than the CY8C20xx7/S power supply. For more information see item #6 in the "Errata" on page 37.
51. Errata: For more information see item #6 in the "Errata" on page 37.

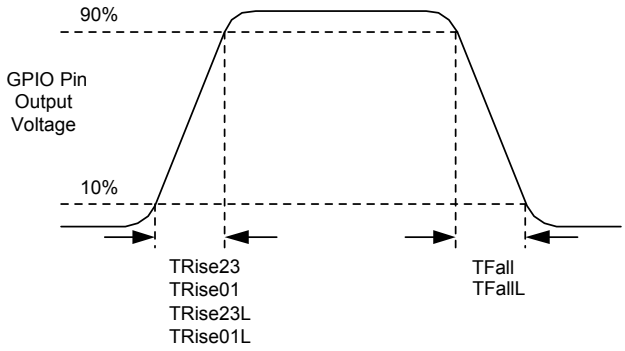
## AC General Purpose I/O Specifications

Table 25 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 25. AC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO operating frequency | Normal strong mode Port 0, 1 | 0<br>0 | –<br>– | 6 MHz for 1.71 V <$V_{DD}$ < 2.40 V<br>12 MHz for 2.40 V < $V_{DD}$< 5.50 V | MHz<br>MHz |
| $t_{RISE23}$ | Rise time, strong mode, Cload = 50 pF Ports 2 or 3 | $V_{DD}$ = 3.0 to 3.6 V, 10% to 90% | 15 | – | 80 | ns |
| $t_{RISE23L}$ | Rise time, strong mode low supply, Cload = 50 pF, Ports 2 or 3 | $V_{DD}$ = 1.71 to 3.0 V, 10% to 90% | 15 | – | 80 | ns |
| $t_{RISE01}$ | Rise time, strong mode, Cload = 50 pF Ports 0 or 1 | $V_{DD}$ = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled | 10 | – | 50 | ns |
| $t_{RISE01L}$ | Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1 | $V_{DD}$ = 1.71 to 3.0 V, 10% to 90% LDO enabled or disabled | 10 | – | 80 | ns |
| $t_{FALL}$ | Fall time, strong mode, Cload = 50 pF all ports | $V_{DD}$ = 3.0 to 3.6 V, 10% to 90% | 10 | – | 50 | ns |
| $t_{FALLL}$ | Fall time, strong mode low supply, Cload = 50 pF, all ports | $V_{DD}$ = 1.71 to 3.0 V, 10% to 90% | 10 | – | 70 | ns |

**Figure 9. GPIO Timing Diagram**




## AC Comparator Specifications

Table 26 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 26. AC Low Power Comparator Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{LPC}$ | Comparator response time, 50 mV overdrive | 50 mV overdrive does not include offset voltage. | – | – | 100 | ns |

## AC External Clock Specifications

Table 27 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 27. AC External Clock Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency (external oscillator frequency) | – | 0.75 | – | 25.20 | MHz |
| | High period | – | 20.60 | – | 5300 | ns |
| | Low period | – | 20.60 | – | – | ns |
| | Power-up IMO to switch | – | 150 | – | – | µs |

## AC Programming Specifications

**Figure 10. AC Waveform**

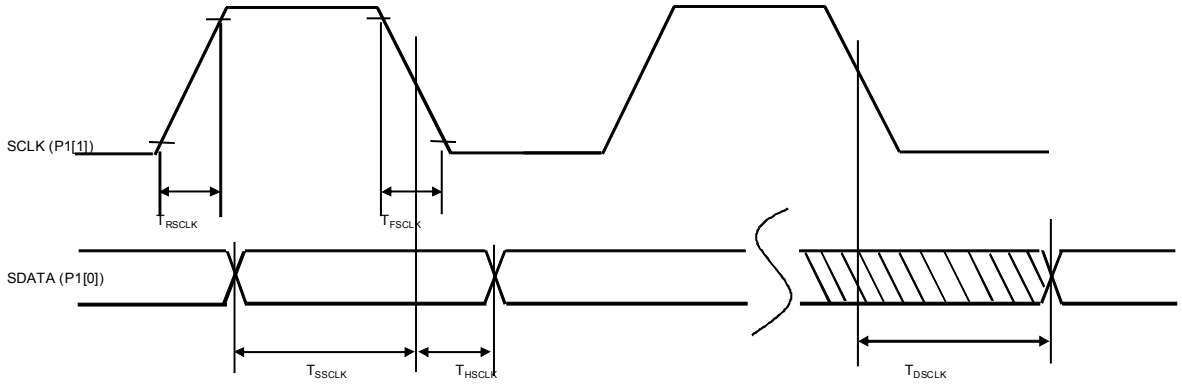



Table 28 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 28. AC Programming Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{RSCLK}$ | Rise time of SCLK | – | 1 | – | 20 | ns |
| $t_{FSCLK}$ | Fall time of SCLK | – | 1 | – | 20 | ns |
| $t_{SSCLK}$ | Data setup time to falling edge of SCLK | – | 40 | – | – | ns |
| $t_{HSCLK}$ | Data hold time from falling edge of SCLK | – | 40 | – | – | ns |
| $F_{SCLK}$ | Frequency of SCLK | – | 0 | – | 8 | MHz |
| $t_{ERASEB}$ | Flash erase time (block) | – | – | – | 18 | ms |
| $t_{WRITE}$ | Flash block write time | – | – | – | 25 | ms |
| $t_{DSCLK}$ | Data out delay from falling edge of SCLK | $3.6 < V_{DD}$ | – | – | 60 | ns |
| $t_{DSCLK3}$ | Data out delay from falling edge of SCLK | $3.0 \le V_{DD} \le 3.6$ | – | – | 85 | ns |
| $t_{DSCLK2}$ | Data out delay from falling edge of SCLK | $1.71 \le V_{DD} \le 3.0$ | – | – | 130 | ns |
| $t_{XRST3}$ | External reset pulse width after power-up | Required to enter programming mode when coming out of sleep | 300 | – | – | µs |
| $t_{XRES}$ | XRES pulse length | – | 300 | – | – | µs |
| $t_{VDDWAIT}$[54] | $V_{DD}$ stable to wait-and-poll hold off | – | 0.1 | – | 1 | ms |
| $t_{VDDXRES}$[54] | $V_{DD}$ stable to XRES assertion delay | – | 14.27 | – | – | ms |
| $t_{POLL}$ | SDAT high pulse time | – | 0.01 | – | 200 | ms |
| $t_{ACQ}$[54] | “Key window” time after a $V_{DD}$ ramp acquire event, based on 256 ILO clocks. | – | 3.20 | – | 19.60 | ms |
| $t_{XRESINI}$[54] | “Key window” time after an XRES event, based on 8 ILO clocks | – | 98 | – | 615 | µs |

**Note**
54. Valid from 5 to 50 °C. See the spec, CY8C20X66, CY8C20X46, CY8C20X36, CY7C643XX, CY7C604XX, CY8CTST2XX, CY8CTMG2XX, CY8C20X67, CY8C20X47, CY8C20X37, Programming Spec for more details.

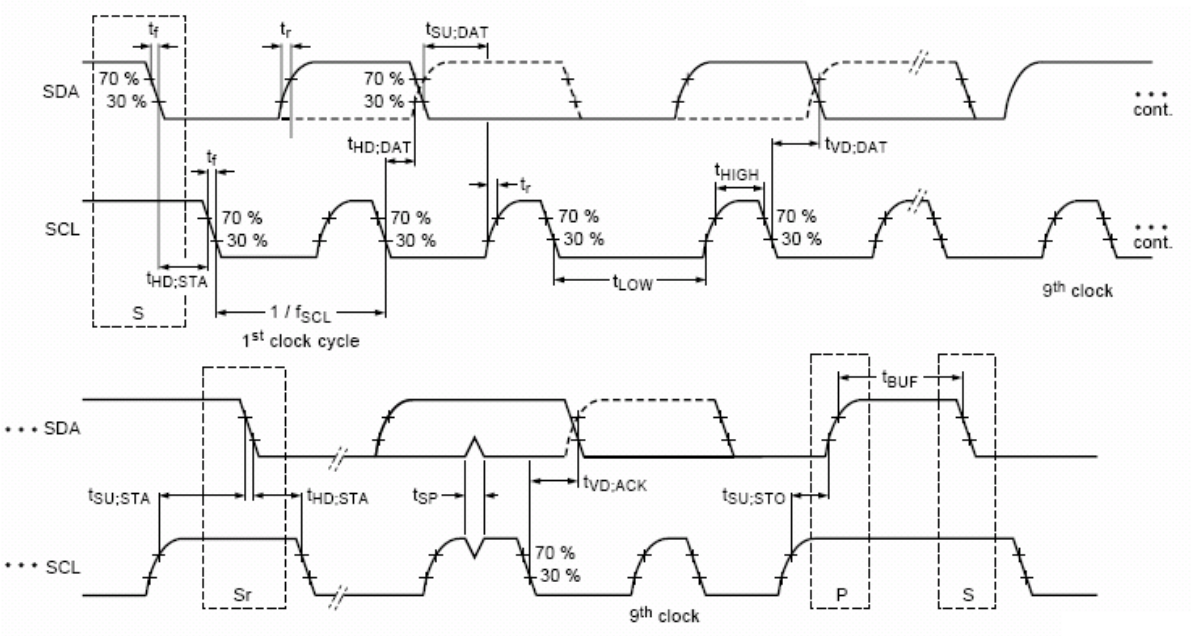
## AC I²C Specifications

Table 29 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 29. AC Characteristics of the I²C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0 | – | 0.6 | – | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | – | 1.3 | – | µs |
| $t_{HIGH}$ | HIGH Period of the SCL clock | 4.0 | – | 0.6 | – | µs |
| $t_{SU;STA}$ | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | µs |
| $t_{HD;DAT}$[55] | Data hold time | 20 | 3.45 | 20 | 0.90 | µs |
| $t_{SU;DAT}$ | Data setup time | 250 | – | 100[56] | – | ns |
| $t_{SU;STO}$ | Setup time for STOP condition | 4.0 | – | 0.6 | – | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | µs |
| $t_{SP}$ | Pulse width of spikes are suppressed by the input filter | – | – | 0 | 50 | ns |

**Figure 11. Definition for Timing for Fast/Standard Mode on the I²C Bus**




**Notes**

55. Errata: To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. For more information see item #5 in the "Errata" on page 37.
56. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

**Table 30. SPI Master AC Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{SCLK}$ | SCLK clock frequency | $V_{DD} \geq 2.4$ V<br>$V_{DD} < 2.4$ V | –<br>– | –<br>– | 6<br>3 | MHz<br>MHz |
| DC | SCLK duty cycle | – | – | 50 | – | % |
| $t_{SETUP}$ | MISO to SCLK setup time | $V_{DD} \geq 2.4$ V<br>$V_{DD} < 2.4$ V | 60<br>100 | –<br>– | –<br>– | ns<br>ns |
| $t_{HOLD}$ | SCLK to MISO hold time | – | 40 | – | – | ns |
| $t_{OUT\_VAL}$ | SCLK to MOSI valid time | – | – | – | 40 | ns |
| $t_{OUT\_H}$ | MOSI high time | – | 40 | – | – | ns |

**Figure 12. SPI Master Mode 0 and 2**

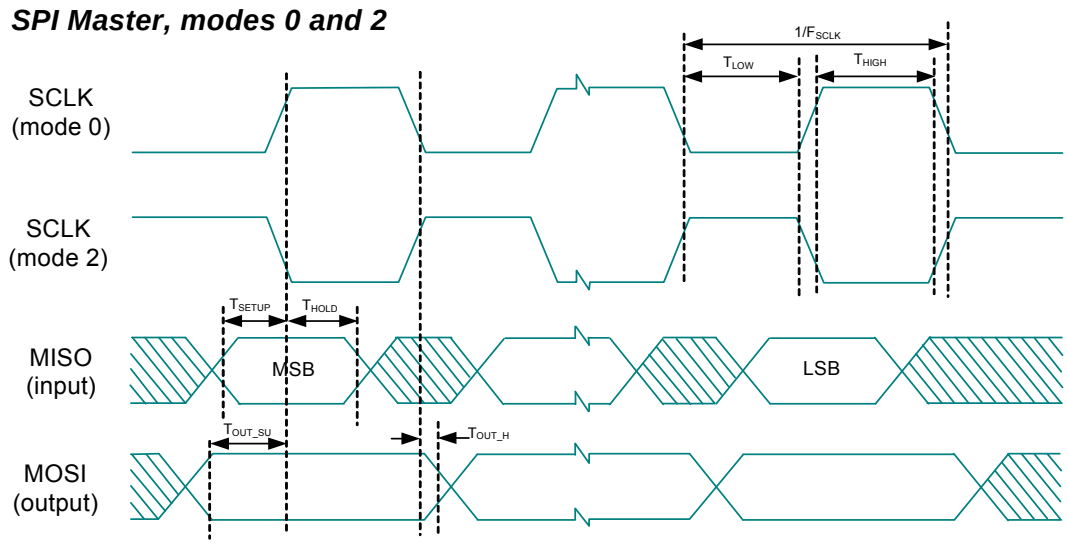



**Figure 13. SPI Master Mode 1 and 3**

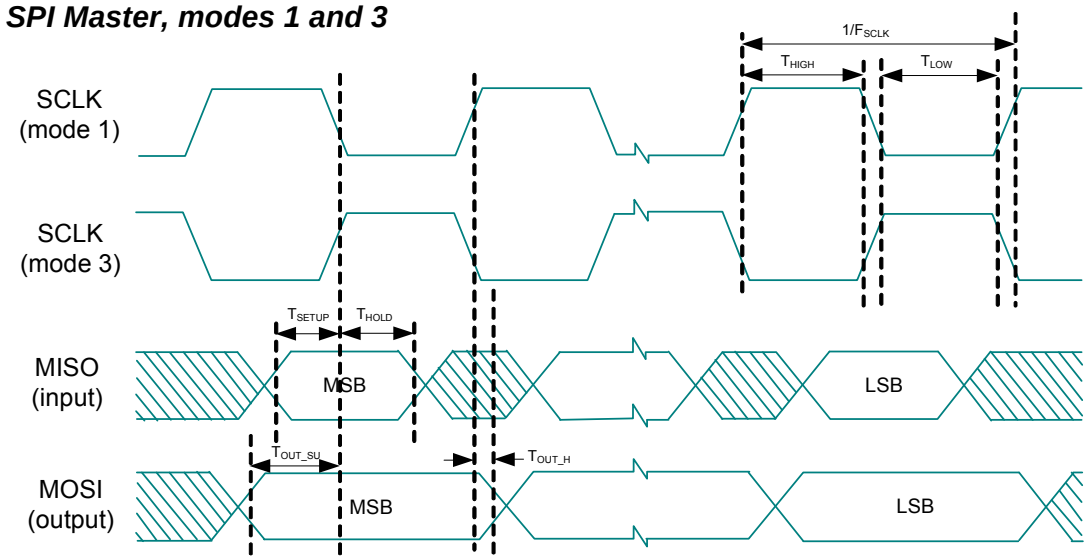


**Table 31. SPI Slave AC Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{SCLK}$ | SCLK clock frequency | – | – | – | 4 | MHz |
| $t_{LOW}$ | SCLK low time | – | 42 | – | – | ns |
| $t_{HIGH}$ | SCLK high time | – | 42 | – | – | ns |
| $t_{SETUP}$ | MOSI to SCLK setup time | – | 30 | – | – | ns |
| $t_{HOLD}$ | SCLK to MOSI hold time | – | 50 | – | – | ns |
| $t_{SS\_MISO}$ | SS high to MISO valid | – | – | – | 153 | ns |
| $t_{SCLK\_MISO}$ | SCLK to MISO valid | – | – | – | 125 | ns |
| $t_{SS\_HIGH}$ | SS high time | – | 50 | – | – | ns |
| $t_{SS\_CLK}$ | Time from SS low to first SCLK | – | 2/SCLK | – | – | ns |
| $t_{CLK\_SS}$ | Time from last SCLK to SS high | – | 2/SCLK | – | – | ns |

**Figure 14. SPI Slave Mode 0 and 2**

***SPI Slave, modes 0 and 2***

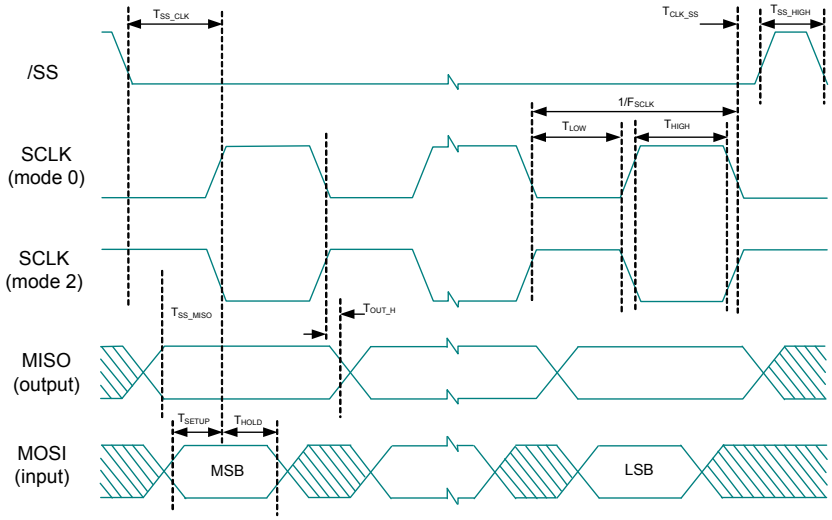
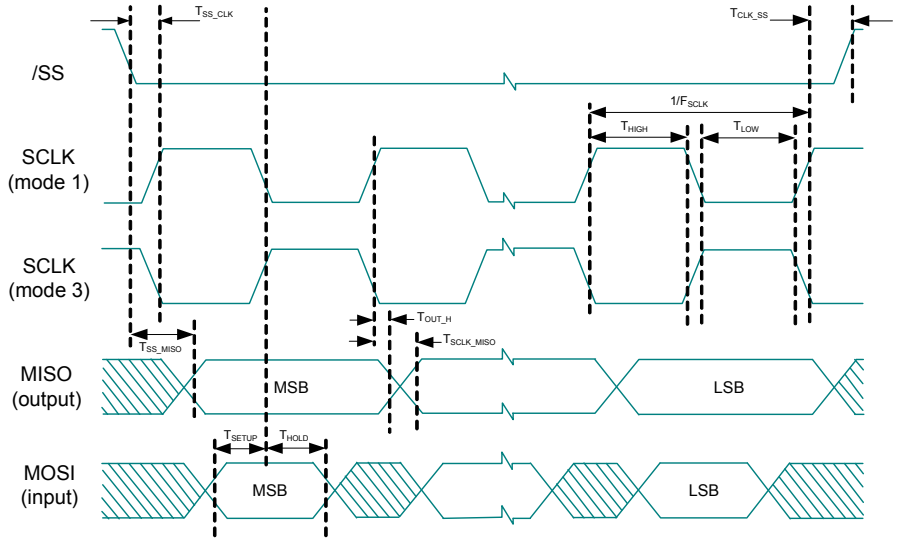



**Figure 15. SPI Slave Mode 1 and 3**

***SPI Slave, modes 1 and 3***



## Ordering Information

Table 35 lists the CY8C20x37/47/67/S PSoC devices' key package features and ordering codes.

**Table 35. PSoC Device Key Features and Ordering Information**

| Ordering Code | Package | Flash (Bytes) | SRAM (Bytes) | CapSense Sensors | Digital I/O Pins | Analog Inputs [59] | XRES Pin | ADC |
|---|---|---|---|---|---|---|---|---|
| CY8C20237-24SXI | 16-pin SOIC | 8 K | 1 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20247S-24SXI | 16-pin SOIC | 16 K | 2 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20237-24LKXI | 16-pin QFN | 8 K | 1 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20237-24LKXIT | 16-pin QFN (Tape and Reel) | 8 K | 1 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20247S-24LKXI | 16-pin QFN | 16 K | 2 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20247S-24LKXIT | 16-pin QFN (Tape and Reel) | 16 K | 2 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20337-24LQXI | 24-pin QFN | 8 K | 1 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20337-24LQXIT | 24-pin QFN (Tape and Reel) | 8 K | 1 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347-24LQXI | 24-pin QFN | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347-24LQXIT | 24-pin QFN (Tape and Reel) | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347S-24LQXI | 24-pin QFN | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347S-24LQXIT | 24-pin QFN (Tape and Reel) | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20437-24LQXI | 32-pin QFN | 8 K | 1 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20437-24LQXIT | 32-pin QFN (Tape and Reel) | 8 K | 1 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447-24LQXI | 32-pin QFN | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447-24LQXIT | 32-pin QFN (Tape and Reel) | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447S-24LQXI | 32-pin QFN | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447S-24LQXIT | 32-pin QFN (Tape and Reel) | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467-24LQXI | 32-pin QFN | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467-24LQXIT | 32-pin QFN (Tape and Reel) | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467S-24LQXI | 32-pin QFN | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467S-24LQXIT | 32-pin QFN (Tape and Reel) | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20637-24LQXI | 48-pin QFN | 8 K | 1 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20637-24LQXIT | 48-pin QFN (Tape and Reel) | 8 K | 1 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647-24LQXI | 48-pin QFN | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647-24LQXIT | 48-pin QFN (Tape and Reel) | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647S-24LQXI | 48-pin QFN | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647S-24LQXIT | 48-pin QFN (Tape and Reel) | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667-24LQXI | 48-pin QFN | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667-24LQXIT | 48-pin QFN (Tape and Reel) | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667S-24LQXI | 48-pin QFN | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667S-24LQXIT | 48-pin QFN (Tape and Reel) | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |

**Note**
59. Dual-function Digital I/O Pins also connect to the common analog mux.

### 3. Missed Interrupt During Transition to Sleep

**■Problem Definition**

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

**■Parameters Affected**

No datasheet parameters are affected.

**■Trigger Condition(S)**

Triggered by enabling sleep mode just prior to an interrupt.

**■Scope of Impact**

The relevant interrupt service routine will not be run.

**■Workaround**

None.

**■Fix Status**

Will not be fixed

**■Changes**

None

### 4. Wakeup from sleep with analog interrupt

**■Problem Definition**

Device wakes up from sleep when an analog interrupt is trigger

**■Parameters Affected**

No datasheet parameters are affected.

**■Trigger Condition(S)**

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

**■Scope of Impact**

Device unexpectedly wakes up from sleep

**■Workaround**

Disable the analog interrupt before entering sleep and turn it back on upon wake-up.

**■Fix Status**

Will not be fixed

**■Changes**

None

### 6. I2C Port Pin Pull-up Supply Voltage

**■Problem Definition**
Pull-up resistor on I2C interface cannot be connected to a supply voltage that is greater than 0.7 V of CY8C20xx7/S $V_{DD}$.

**■Parameters Affected**
None.

**■Trigger Condition(S)**
This problem occurs only when the I2C master is powered at a higher voltage than CY8C20xx7/S.

**■Scope of Impact**
This trigger condition will corrupt the I2C communication between the I2C host and the CY8C20xx7/S CapSense controller.

**■Workaround**
I2C master cannot be powered at a supply voltage that is greater than 0.7 V compared to CY8C20xx7/S supply voltage.

**■Fix Status**
Will not be fixed

**■Changes**
None

### 7. Port1 Pin Voltage

**■Problem Definition**
Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C20xx7/S $V_{DD}$.

**■Parameters Affected**
None.

**■Trigger Condition(S)**
This problem occurs only when port1 pins are at voltage 0.7 V higher than $V_{DD}$ of CY8C20xx7/S.

**■Scope of Impact**
This trigger condition will not allow CY8C20xx7/S to drive the output signal on port1 pins, input path is unaffected by this condition.

**■Workaround**
Port1 should not be connected to a higher voltage than $V_{DD}$ of CY8C20xx7/S.

**■Fix Status**
Will not be fixed

**■Changes**
None

## Document History Page *(continued)*

| Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors<br>Document Number: 001-69257 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *K | 4248645 | DST | 01/16/2014 | Updated Pinouts:<br>Updated 32-pin QFN (25 Sensing Inputs)[25]:<br>Updated Figure 6.<br><br>Updated Packaging Information:<br>spec 001-09116 – Changed revision from *H to *I. |
| *L | 4404150 | SLAN | 06/10/2014 | Updated Pinouts:<br>Updated 16-pin SOIC (10 Sensing Inputs):<br>Updated Table 1:<br>Added Note 6 and referred the same note in description of XRES pin.<br>Updated 16-pin QFN (10 Sensing Inputs)[8]:<br>Updated Table 2:<br>Added Note 12 and referred the same note in description of XRES pin.<br>Updated 24-pin QFN (16 Sensing Inputs)[14]:<br>Updated Table 3:<br>Added Note 18 and referred the same note in description of XRES pin.<br>Updated 30-ball WLCSP (24 Sensing Inputs):<br>Updated Table 4:<br>Added Note 21 and referred the same note in description of XRES pin.<br>Updated 32-pin QFN (25 Sensing Inputs)[25]:<br>Updated Table 5:<br>Added Note 29 and referred the same note in description of XRES pin.<br>Updated 48-pin QFN (31 Sensing Inputs)[31]:<br>Updated Table 6:<br>Added Note 35 and referred the same note in description of XRES pin.<br><br>Updated Electrical Specifications:<br>Updated DC GPIO Specifications:<br>Updated Table 10:<br>Updated minimum and maximum values of $V_{IH}$ parameter.<br>Updated Table 11:<br>Updated minimum and maximum values of $V_{IH}$ parameter.<br>Updated AC Chip-Level Specifications:<br>Updated Table 24:<br>Removed minimum and maximum values of “ILO untrimmed frequency”.<br><br>Updated Packaging Information:<br>spec 001-09116 – Changed revision from *I to *J.<br><br>Completing Sunset Review. |
| *M | 4825924 | SLAN | 07/07/2015 | Added the footnote “All VSS pins should be brought out to one common GND plane” in pinout tables (Table 1 through Table 6).<br>Updated Packaging Information:<br>spec 001-13937 – Changed revision from *E to *F.<br>Updated to new template. |
| *N | 5068999 | ARVI | 12/31/2015 | Updated hyperlink of “Technical Reference Manual” in all instances across the document.<br>Updated PSoC® Functional Overview:<br>Updated Additional System Resources:<br>Updated description.<br>Updated Development Tool Selection:<br>Removed “Accessories (Emulation and Programming)”.<br>Removed “Build a PSoC Emulator into Your Board”. |

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