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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details

|	
Product Status	Active
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY8C20xx7/S
RAM Size	2K x 8
Interface	I²C, SPI
Number of I/O	13
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20247s-24lkxit

Logic Block Diagram
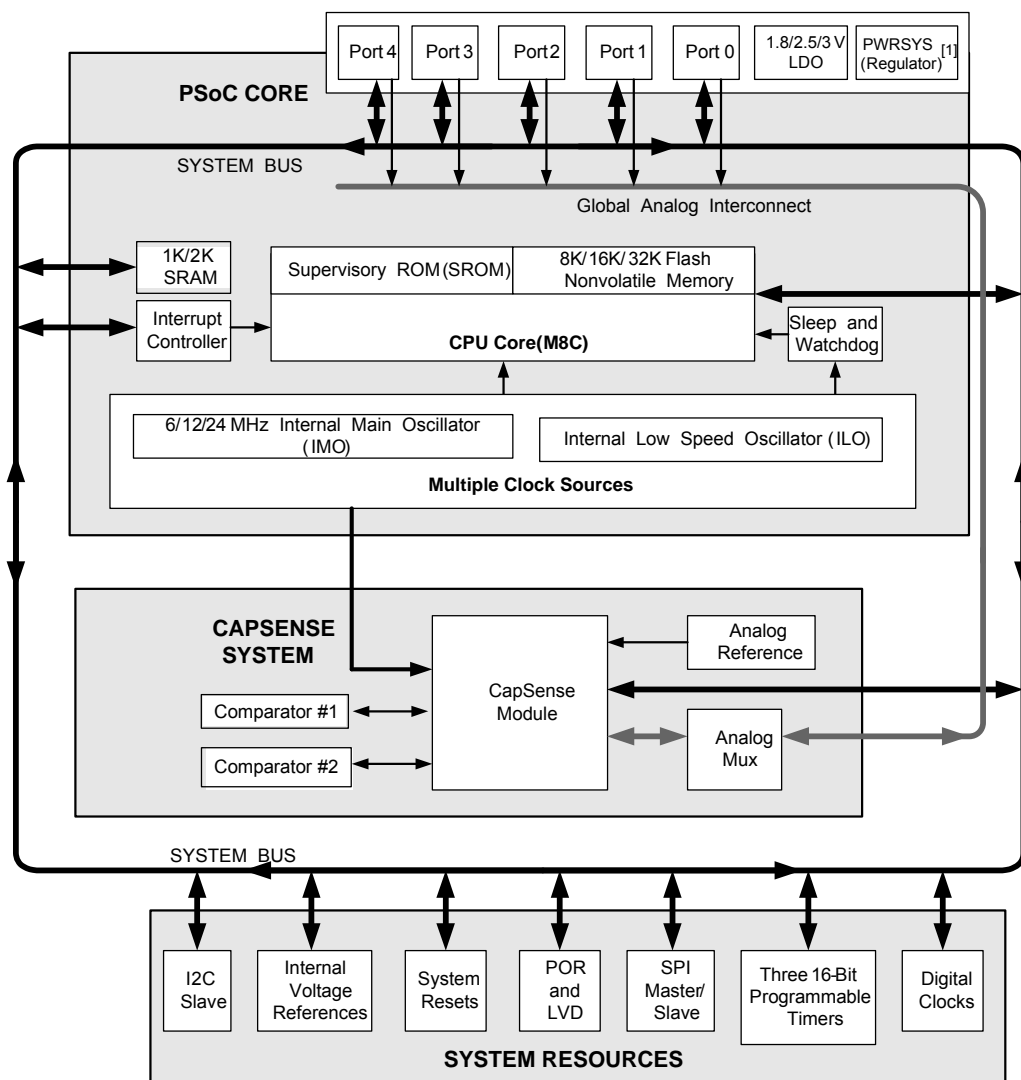
16-pin QFN (10 Sensing Inputs)[8]

Table 2. Pin Definitions – CY8C20237, CY8C20247/S [9]

Pin No.	Type		Name	Description
	Digital	**Analog**		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I^{2}C SCL, SPI SS
4	IOHR	I	P1[5]	I^{2}C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK[10], I^{2}C SCL, SPI MOSI
7	Power		V$_{SS}$	Ground connection[13]
8	IOHR	I	P1[0]	ISSP DATA[10], I^{2}C SDA, SPI CLK[11]
9	IOHR	I	P1[2]	Driven Shield Output (optional)
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down[12]
12	IOH	I	P0[4]	
13	Power		V$_{DD}$	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.
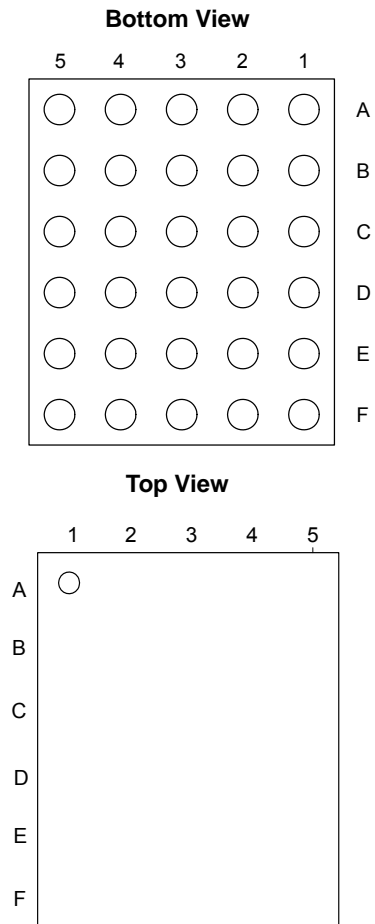
Figure 3. CY8C20237, CY8C20247/S Device
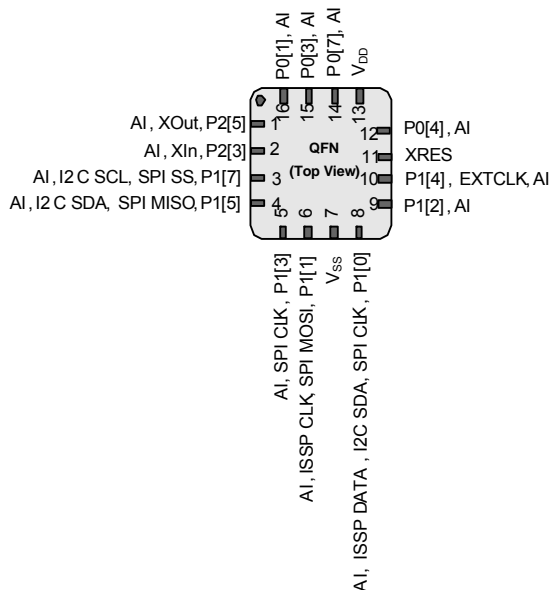
Notes
8. No center pad.
9. 13 GPIOs = 10 pins for capacitive sensing+2 pins for I^{2}C + 1 pin for modulator capacitor.
10. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I^{2}C bus. Use alternate pins if you encounter issues.
11. Alternate SPI clock.
12. The internal pull down is 5KOhm.
13. All VSS pins should be brought out to one common GND plane.

30-ball WLCSP (24 Sensing Inputs)

Table 4. Pin Definitions – CY8C20767, CY8C20747 30-ball Part Pinout (WLCSP) [20]

Pin No.	Type		Name	Description
	Digital	Analog		
A1	IOH	I	P0[2]	Driven Shield Output (optional)
A2	IOH	I	P0[6]	
A3	Power		V_{DD}	Supply voltage
A4	IOH	I	P0[1]	Integrating Input
A5	I/O	I	P2[7]	
B1	I/O	I	P4[2]	
B2	IOH	I	P0[0]	Driven Shield Output (optional)
B3	IOH	I	P0[4]	
B4	IOH	I	P0[3]	Integrating Input
B5	I/O	I	P2[5]	Crystal Output (Xout)
C1	I/O	I	P2[2]	Driven Shield Output (optional)
C2	I/O	I	P2[4]	Driven Shield Output (optional)
C3	I/O	I	P0[7]	
C4	IOH	I	P3[2]	
C5	I/O	I	P2[3]	Crystal Input (Xin)
D1	I/O	I	P2[0]	
D2	I/O	I	P3[0]	
D3	I/O	I	P3[1]	
D4	I/O	I	P3[3]	
D5	I/O	I	P2[1]	
E1	Input		XRES	Active high external reset with internal pull-down[21]
E2	IOHR	I	P1[6]	
E3	IOHR	I	P1[4]	Optional external clock input (EXT CLK)
E4	IOHR	I	P1[7]	I²C SCL, SPI SS
E5	IOHR	I	P1[5]	I²C SDA, SPI MISO
F1	IOHR	I	P1[2]	Driven Shield Output (optional)
F2	IOHR	I	P1[0]	ISSP DATA[22], I²C SDA, SPI CLK[23]
F3	Power		V_{SS}	Supply ground[24]
F4	IOHR	I	P1[1]	ISSP CLK[22], I²C SCL, SPI MOSI
F5	IOHR	I	P1[3]	SPI CLK

LEGEND: A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 5. CY8C20767, CY8C20747 30-ball WLCSP

Bottom View

Top View

Notes

20. 27 GPIOs = 24 pins for capacitive sensing+2 pins for I²C + 1 pin for modulator capacitor.
21. The internal pull down is 5KOhm.
22. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I²C bus. Use alternate pins if you encounter issues.
23. Alternate SPI clock.
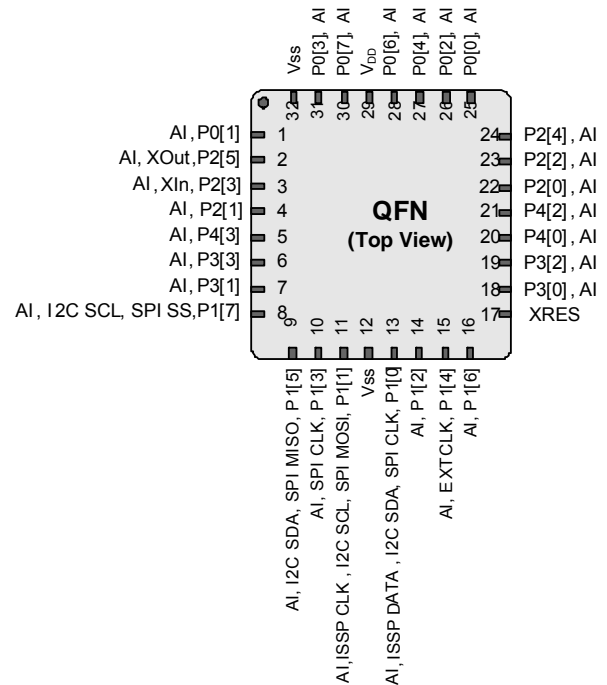24. All VSS pins should be brought out to one common GND plane.

32-pin QFN (25 Sensing Inputs)[25]

Table 5. Pin Definitions – CY8C20437, CY8C20447/S, CY8C20467/S [26]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[5]	Crystal output (XOut)
3	I/O	I	P2[3]	Crystal input (XIn)
4	I/O	I	P2[1]	
5	I/O	I	P4[3]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I2C SCL, SPI SS
9	IOHR	I	P1[5]	I2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK[27], I2C SCL, SPI MOSI.
12	Power		V_{SS}	Ground connection[30]
13	IOHR	I	P1[0]	ISSP DATA[27], I2C SDA, SPI CLK[28]
14	IOHR	I	P1[2]	Driven Shield Output (optional)
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down[29]
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P4[0]	
21	I/O	I	P4[2]	
22	I/O	I	P2[0]	
23	I/O	I	P2[2]	Driven Shield Output (optional)
24	I/O	I	P2[4]	Driven Shield Output (optional)
25	IOH	I	P0[0]	Driven Shield Output (optional)
26	IOH	I	P0[2]	Driven Shield Output (optional)
27	IOH	I	P0[4]	
28	IOH	I	P0[6]	
29	Power		V_{DD}	
30	IOH	I	P0[7]	
31	IOH	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[30]
CP	Power		V_{SS}	Center pad must be connected to ground

Figure 6. CY8C20437, CY8C20447/S, CY8C20467/S Device

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes
25. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
26. 28 GPIOs = 25 pins for capacitive sensing+2 pins for I2C + 1 pin for modulator capacitor.
27. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
28. Alternate SPI clock.
29. The internal pull down is 5KOhm.
30. All VSS pins should be brought out to one common GND plane.

DC Chip-Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 9. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}[37, 38, 39]	Supply voltage	See Table 14 on page 17.	1.71	–	5.50	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	2.88	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.71	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.16	1.80	mA
I_{SB0} [40, 41, 42, 43]	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.1	μA
I_{SB1} [40, 41, 42, 43]	Standby current with POR, LVD and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	μA
I_{SBI2C} [40, 41, 42, 43]	Standby current with I^2C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	μA

Notes

37. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 μs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
38. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that V_{DD} falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the Technical Reference Manual. In deep sleep/standby sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected and resets the device when V_{DD} goes lower than 1.1 V at edge rates slower than 1 V/ms.
39. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.
40. Errata: When programmable timer 0 is used in "one-shot" mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the "Errata" on page 37.
41. Errata: When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the "Errata" on page 37.
42. Errata: If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the "Errata" on page 37.
43. Errata: Device wakes up from sleep when an analog interrupt is trigger. For more information, see the "Errata" on page 37.

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C $\leq$ T_A $\leq$ 85 °C, 2.4 V to 3.0 V and –40 °C $\leq$ T_A $\leq$ 85 °C, or 1.71 V to 2.4 V and –40 °C $\leq$ T_A $\leq$ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 10.   3.0 V to 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	$I_{OH} \leq 10$ µA, maximum of 10 mA source current in all I/Os	$V_{DD} - 0.20$	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	$I_{OH} = 1$ mA, maximum of 20 mA source current in all I/Os	$V_{DD} - 0.90$	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	$I_{OH} < 10$ µA, maximum of 10 mA source current in all I/Os	$V_{DD} - 0.20$	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	$I_{OH} = 5$ mA, maximum of 20 mA source current in all I/Os	$V_{DD} - 0.90$	–	–	V
V_{OH5}	High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out	$I_{OH} < 10$ µA, $V_{DD} > 3.1$ V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	$I_{OH} = 5$ mA, $V_{DD} > 3.1$ V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	$I_{OH} < 10$ µA, $V_{DD} > 2.7$ V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	$I_{OH} = 2$ mA, $V_{DD} > 2.7$ V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	$I_{OH} < 10$ µA, $V_{DD} > 2.7$ V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	$I_{OH} = 1$ mA, $V_{DD} > 2.7$ V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	$I_{OL} = 25$ mA, $V_{DD} > 3.3$ V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.80	V
V_{IH}	Input high voltage	–	$V_{DD} \times 0.65$	–	$V_{DD} + 0.7$	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (Absolute Value)	–	–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT3.3}$	Input Low Voltage with low threshold enable set, Enable for Port1 [44]	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT3.3}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.4	–	–	V
$V_{ILLVT5.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT5.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.7	–	–	V

Note
44. Errata: Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C20xx7/S VDD. For more information see item #7 in "Errata" on page 37.

AC Programming Specifications
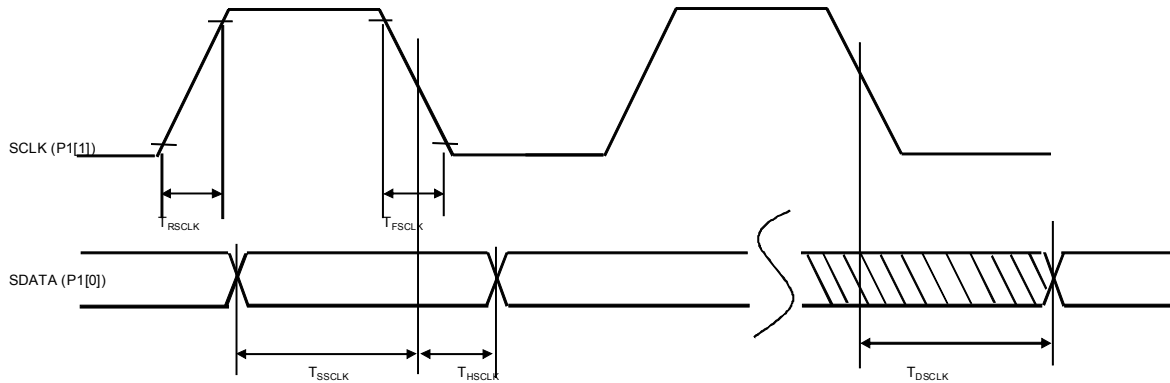
Figure 10. AC Waveform

Table 28 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 28. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{RSCLK}	Rise time of SCLK	–	1	–	20	ns
t_{FSCLK}	Fall time of SCLK	–	1	–	20	ns
t_{SSCLK}	Data setup time to falling edge of SCLK	–	40	–	–	ns
t_{HSCLK}	Data hold time from falling edge of SCLK	–	40	–	–	ns
F_{SCLK}	Frequency of SCLK	–	0	–	8	MHz
t_{ERASEB}	Flash erase time (block)	–	–	–	18	ms
t_{WRITE}	Flash block write time	–	–	–	25	ms
t_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
t_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \leq V_{DD} \leq 3.6$	–	–	85	ns
t_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \leq V_{DD} \leq 3.0$	–	–	130	ns
t_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	μs
t_{XRES}	XRES pulse length	–	300	–	–	μs
$t_{VDDWAIT}$[54]	V_{DD} stable to wait-and-poll hold off	–	0.1	–	1	ms
$t_{VDDXRES}$[54]	V_{DD} stable to XRES assertion delay	–	14.27	–	–	ms
t_{POLL}	SDAT high pulse time	–	0.01	–	200	ms
t_{ACQ}[54]	"Key window" time after a V_{DD} ramp acquire event, based on 256 ILO clocks.	–	3.20	–	19.60	ms
$t_{XRESINI}$[54]	"Key window" time after an XRES event, based on 8 ILO clocks	–	98	–	615	μs

Table 31. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
t_{LOW}	SCLK low time	–	42	–	–	ns
t_{HIGH}	SCLK high time	–	42	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
t_{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Figure 14. SPI Slave Mode 0 and 2
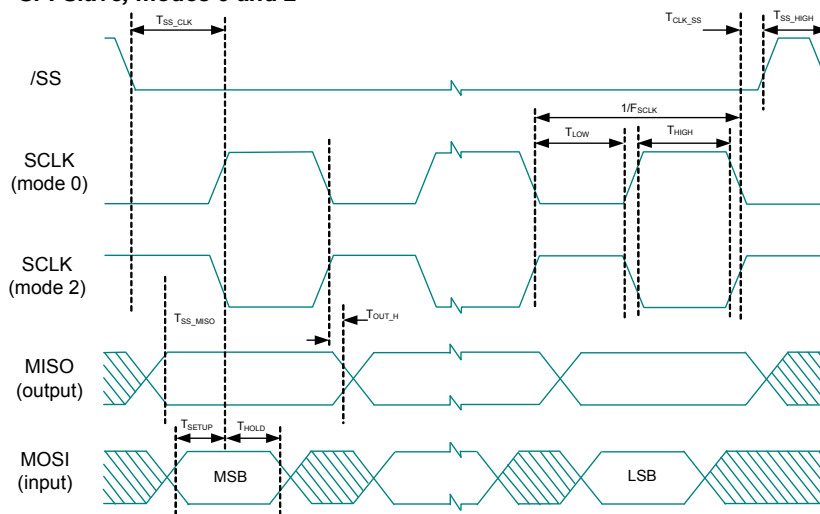
Figure 15. SPI Slave Mode 1 and 3

Figure 18. 24-Pin (4 × 4 × 0.6 mm) QFN

TOP VIEW   SIDE VIEW   BOTTOM VIEW
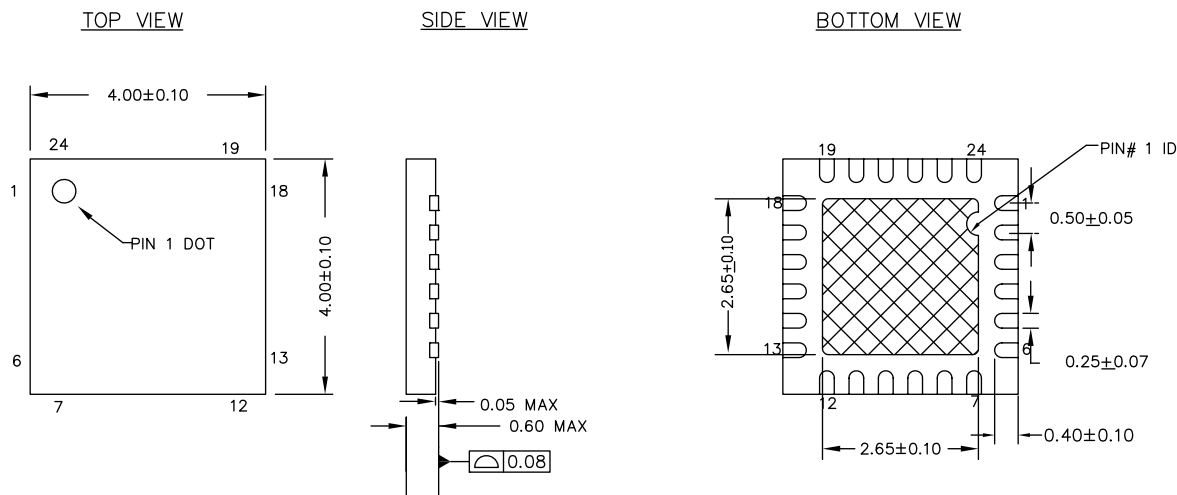
NOTES :

1. [hatch] HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Figure 19. 32-Pin (5 × 5 × 0.6 mm) QFN

NOTES:

1. [hatch] HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Figure 20. 48-Pin (6 × 6 × 0.6 mm) QFN

TOP VIEW

SIDE VIEW

BOTTOM VIEW

6.00±0.10

48   37

1

36

PIN 1 DOT

6.00±0.10

12   25

13   24

0.05 MAX
0.60 MAX

0.08

PIN# 1 ID

37   48

36   1

0.40±0.05

4.60±0.10

0.20±0.05

25   12

24   13

4.60±0.10   0.40±0.10
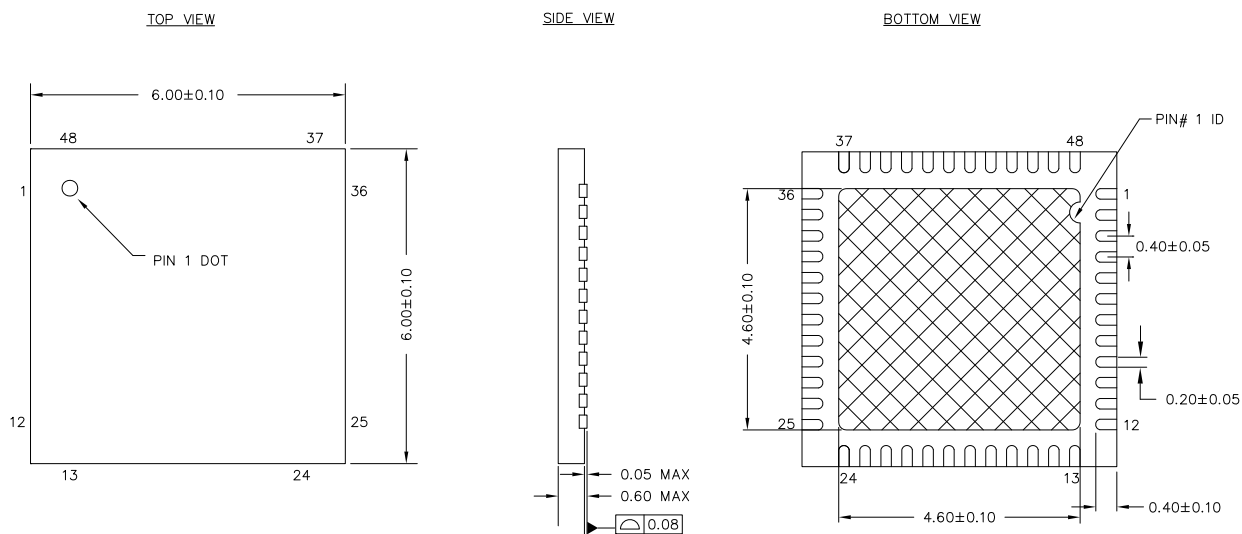
001-57280 *E

NOTES:

1. ⊠   HATCH AREA IS SOLDERABLE EXPOSED PAD

2. REFERENCE JEDEC # MO−248

3. PACKAGE WEIGHT: 68 ±7   mg

4. ALL DIMENSIONS ARE IN MILLIMETERS

Important Notes

■ For information on the preferred dimensions for mounting QFN packages, see the following Application Note at
http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

■ Pinned vias for thermal conduction are not required for the low power PSoC device.

Ordering Information

Table 35 lists the CY8C20x37/47/67/S PSoC devices' key package features and ordering codes.

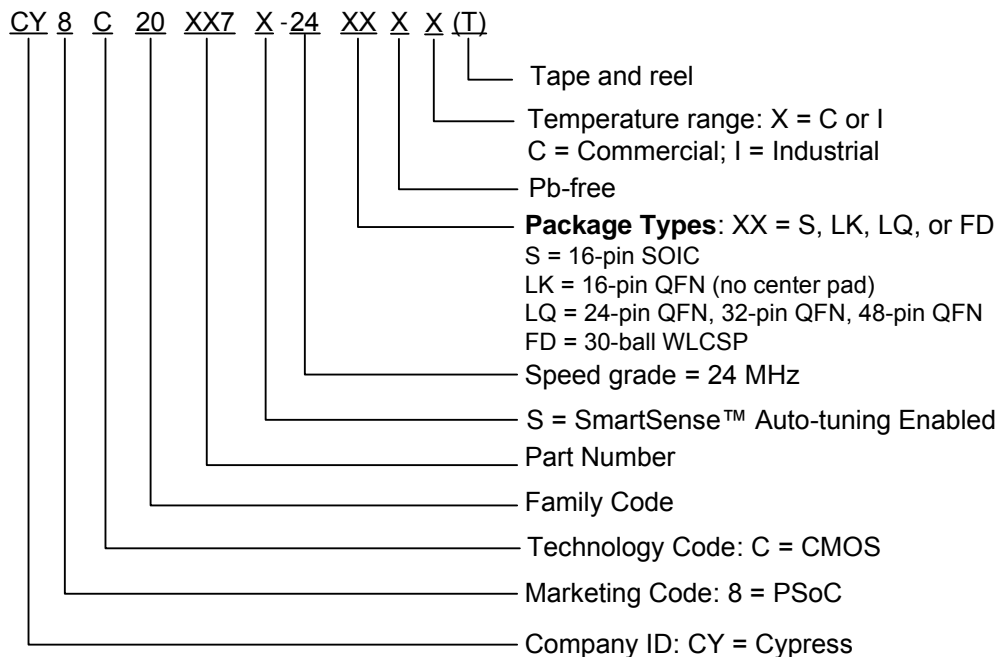**Table 35. PSoC Device Key Features and Ordering Information**

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	CapSense Sensors	Digital I/O Pins	Analog Inputs [59]	XRES Pin	ADC
CY8C20237-24SXI	16-pin SOIC	8 K	1 K	10	13	13	Yes	Yes
CY8C20247S-24SXI	16-pin SOIC	16 K	2 K	10	13	13	Yes	Yes
CY8C20237-24LKXI	16-pin QFN	8 K	1 K	10	13	13	Yes	Yes
CY8C20237-24LKXIT	16-pin QFN (Tape and Reel)	8 K	1 K	10	13	13	Yes	Yes
CY8C20247S-24LKXI	16-pin QFN	16 K	2 K	10	13	13	Yes	Yes
CY8C20247S-24LKXIT	16-pin QFN (Tape and Reel)	16 K	2 K	10	13	13	Yes	Yes
CY8C20337-24LQXI	24-pin QFN	8 K	1 K	16	19	19	Yes	Yes
CY8C20337-24LQXIT	24-pin QFN (Tape and Reel)	8 K	1 K	16	19	19	Yes	Yes
CY8C20347-24LQXI	24-pin QFN	16 K	2 K	16	19	19	Yes	Yes
CY8C20347-24LQXIT	24-pin QFN (Tape and Reel)	16 K	2 K	16	19	19	Yes	Yes
CY8C20347S-24LQXI	24-pin QFN	16 K	2 K	16	19	19	Yes	Yes
CY8C20347S-24LQXIT	24-pin QFN (Tape and Reel)	16 K	2 K	16	19	19	Yes	Yes
CY8C20437-24LQXI	32-pin QFN	8 K	1 K	25	28	28	Yes	Yes
CY8C20437-24LQXIT	32-pin QFN (Tape and Reel)	8 K	1 K	25	28	28	Yes	Yes
CY8C20447-24LQXI	32-pin QFN	16 K	2 K	25	28	28	Yes	Yes
CY8C20447-24LQXIT	32-pin QFN (Tape and Reel)	16 K	2 K	25	28	28	Yes	Yes
CY8C20447S-24LQXI	32-pin QFN	16 K	2 K	25	28	28	Yes	Yes
CY8C20447S-24LQXIT	32-pin QFN (Tape and Reel)	16 K	2 K	25	28	28	Yes	Yes
CY8C20467-24LQXI	32-pin QFN	32 K	2 K	25	28	28	Yes	Yes
CY8C20467-24LQXIT	32-pin QFN (Tape and Reel)	32 K	2 K	25	28	28	Yes	Yes
CY8C20467S-24LQXI	32-pin QFN	32 K	2 K	25	28	28	Yes	Yes
CY8C20467S-24LQXIT	32-pin QFN (Tape and Reel)	32 K	2 K	25	28	28	Yes	Yes
CY8C20637-24LQXI	48-pin QFN	8 K	1 K	31	34	34	Yes	Yes
CY8C20637-24LQXIT	48-pin QFN (Tape and Reel)	8 K	1 K	31	34	34	Yes	Yes
CY8C20647-24LQXI	48-pin QFN	16 K	2 K	31	34	34	Yes	Yes
CY8C20647-24LQXIT	48-pin QFN (Tape and Reel)	16 K	2 K	31	34	34	Yes	Yes
CY8C20647S-24LQXI	48-pin QFN	16 K	2 K	31	34	34	Yes	Yes
CY8C20647S-24LQXIT	48-pin QFN (Tape and Reel)	16 K	2 K	31	34	34	Yes	Yes
CY8C20667-24LQXI	48-pin QFN	32 K	2 K	31	34	34	Yes	Yes
CY8C20667-24LQXIT	48-pin QFN (Tape and Reel)	32 K	2 K	31	34	34	Yes	Yes
CY8C20667S-24LQXI	48-pin QFN	32 K	2 K	31	34	34	Yes	Yes
CY8C20667S-24LQXIT	48-pin QFN (Tape and Reel)	32 K	2 K	31	34	34	Yes	Yes

Note
59. Dual-function Digital I/O Pins also connect to the common analog mux.

Table 35. PSoC Device Key Features and Ordering Information *(continued)*

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	CapSense Sensors	Digital I/O Pins	Analog Inputs [59]	XRES Pin	ADC
CY8C20767-24FDXC	30-pin WLCSP	32 K	2 K	24	27	27	Yes	Yes
CY8C20767-24FDXCT	30-pin WLCSP (Tape and Reel)	32 K	2 K	24	27	27	Yes	Yes

Ordering Code Definitions

CY 8 C 20 XX7 X -24 XX X X (T)

- Tape and reel
- Temperature range: X = C or I
  C = Commercial; I = Industrial
- Pb-free
- **Package Types**: XX = S, LK, LQ, or FD
  S = 16-pin SOIC
  LK = 16-pin QFN (no center pad)
  LQ = 24-pin QFN, 32-pin QFN, 48-pin QFN
  FD = 30-ball WLCSP
- Speed grade = 24 MHz
- S = SmartSense™ Auto-tuning Enabled
- Part Number
- Family Code
- Technology Code: C = CMOS
- Marketing Code: 8 = PSoC
- Company ID: CY = Cypress

Acronyms

The following table lists the acronyms that are used in this document.

Table 36. Acronyms Used in this Document

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
ESD	electrostatic discharge
FSR	full scale range
GPIO	general purpose input/output
I^{2}C	inter-integrated circuit
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
ISSP	in-system serial programming
LCD	liquid crystal display
LDO	low dropout (regulator)
LED	light-emitting diode
LPC	low power comparator
LSB	least-significant bit
LVD	low voltage detect
MCU	micro-controller unit
MIPS	million instructions per second
MISO	master in slave out
MOSI	master out slave in
MSB	most-significant bit
OCD	on-chip debug
PCB	printed circuit board
POR	power on reset
PSRR	power supply rejection ratio
PWRSYS	power system
PSoC	programmable system-on-chip
QFN	quad flat no-lead
SCLK	serial I^{2}C clock
SDA	serial I^{2}C data
SDATA	serial ISSP data
SOIC	small outline integrated circuit
SPI	serial peripheral interface
SRAM	static random access memory
SS	slave select
USB	universal serial bus
WLCSP	wafer level chip scale package

Reference Documents

■ *Technical reference manual for CY20xx7 devices*

■ *In-system Serial Programming (ISSP) protocol for 20xx7*

■ *Host Sourced Serial Programming for 20xx7 devices*

Document Conventions

Units of Measure

Table 37 lists all the abbreviations used to measure the PSoC devices.

Table 37. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibel
kHz	kilohertz
ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

Glossary

Crosspoint connection	Connection between any GPIO combination via analog multiplexer bus.
Differential non linearity	Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step.
Hold time	Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.
I^2C	It is a serial multi-master bus used to connect low speed peripherals to MCU.
Integral nonlinearity	It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level.
Latch-up current	Current at which the latch-up test is conducted according to JESD78 standard (at 125 degree Celsius)
Power supply rejection ratio (PSRR)	The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device.
Scan	The conversion of all sensor capacitances to digital values.
Setup time	Period required to prepare a device, machine, process, or system for it to be ready to function.
Signal-to-noise ratio	The ratio between a capacitive finger signal and system noise.
SPI	Serial peripheral interface is a synchronous serial data link standard.

Errata

This section describes the errata for the CY8C20xx7/S family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY8C20xx7/S Qualification Status

Product Status: Production released.

CY8C20xx7/S Errata Summary

The following Errata items apply to the CY8C20xx7/S datasheet 001-69257.

1. DoubleTimer0 ISR

■Problem Definition

When programmable timer 0 is used in "one-shot" mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

■Parameters Affected

No datasheet parameters are affected.

■Trigger Condition(S)

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

■Scope of Impact

The ISR may be executed twice.

■Workaround

In the ISR, firmware should clear the one-shot bit with a statement such as "`and reg[B0h], FDh`"

■Fix Status

Will not be fixed

■Changes

None

2. Missed GPIO Interrupt

■Problem Definition

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

■Parameters Affected

No datasheet parameters are affected.

■Trigger Condition(S)

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

■Scope of Impact

The GPIO interrupt service routine will not be run.

■Workaround

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt. Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0. Alternatively, the ISR's for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

■Fix Status

Will not be fixed

■Changes

None

5. Wake-up from Sleep with Hardware I2C Address match on Pins P1[0], P1[1]

■**Problem Definition**

I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL, to wake-up from sleep using I2C hardware address match event.

■**Parameters Affected**

$t_{HD;DAT}$ increased to 20 ns from 0 ns

■**Trigger Condition(S)**

This is an issue only when all these three conditions are met:

1) P1.0 and P1.1 are used as I2C pins,

2) Wakeup from sleep with hardware address match feature is enabled, and

3) I2C master does not provide 20 ns hold time on SDA with respect to falling edge of SCL.

■**Scope of Impact**

These trigger conditions cause the device to never wake-up from sleep based on I2C address match event.

■**Workaround**

For a design that meets all of the trigger conditions, the following suggested circuit has to be implemented as a work-around. The R and C values proposed are 100 ohm and 200 pF respectively.
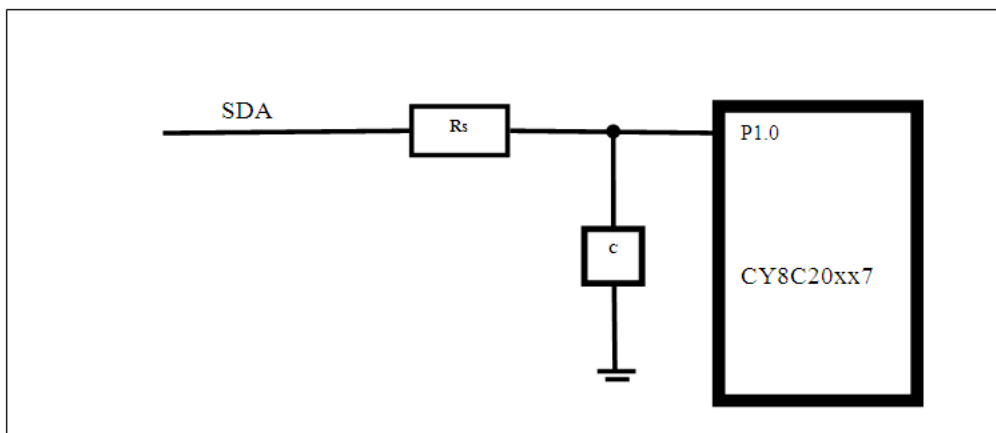
■**Fix Status**

Will not be fixed

■**Changes**

None

6. I2C Port Pin Pull-up Supply Voltage

■Problem Definition

Pull-up resistor on I2C interface cannot be connected to a supply voltage that is greater than 0.7 V of CY8C20xx7/S V_{DD}.

■Parameters Affected

None.

■Trigger Condition(S)

This problem occurs only when the I2C master is powered at a higher voltage than CY8C20xx7/S.

■Scope of Impact

This trigger condition will corrupt the I2C communication between the I2C host and the CY8C20xx7/S CapSense controller.

■Workaround

I2C master cannot be powered at a supply voltage that is greater than 0.7 V compared to CY8C20xx7/S supply voltage.

■Fix Status

Will not be fixed

■Changes

None

7. Port1 Pin Voltage

■Problem Definition

Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C20xx7/S V_{DD}.

■Parameters Affected

None.

■Trigger Condition(S)

This problem occurs only when port1 pins are at voltage 0.7 V higher than V_{DD} of CY8C20xx7/S.

■Scope of Impact

This trigger condition will not allow CY8C20xx7/S to drive the output signal on port1 pins, input path is unaffected by this condition.

■Workaround

Port1 should not be connected to a higher voltage than V_{DD} of CY8C20xx7/S.

■Fix Status

Will not be fixed

■Changes

None

Document History Page

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors				
Document Number: 001-69257				

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3276782	DST	06/27/2011	New silicon and document
*A	3327230	DST	07/28/2011	Changed 48-pin dimensions to 6 × 6 × 0.6 mm QFN Updated pins name in Table 3 on page 9 and removed USB column and updated dimensions for 48-pin parts in Table 35 on page 33 Updated Figure 20 on page 29 Removed ICE and Debugger sections. Removed CY3215 Development Kit and CY3280-20x66 UCC sections. Updated Ordering Information.
*B	3403111	YVA	10/12/2011	Moved status from Advance to Preliminary. Updated Ordering Information Removed the row named "48-Pin (6 × 6 mm) QFN (OCD)". Changed all 48-pin ordering code column from CY8C20XXX-24LTxx to CY8C20XXX-24LQxx. Updated 16-pin SOIC and 16-pin QFN package drawings.
*C	3473317	DST	12/23/2011	Updated Features. Updated Pinouts (Removed PSoC in captions of Figure 2, Figure 3, Figure 4, Figure 6, and Figure 7). Updated DC Chip-Level Specifications under Electrical Specifications (Updated typical value of I_{DD24} parameter from 3.32 mA to 2.88 mA, updated typical value of I_{DD12} parameter from 1.86 mA to 1.71 mA, updated typical value of I_{DD6} parameter from 1.13 mA to 1.16 mA, updated maximum value of I_{SB0} parameter from 0.50 µA to 1.1 µA, added I_{SBI2C} parameter and its details). Updated DC GPIO Specifications under Electrical Specifications (Added the parameters namely $V_{ILLVT3.3}$, $V_{IHLVT3.3}$, $V_{ILLVT5.5}$, $V_{IHLVT5.5}$ and their details in Table 10, added the parameters namely $V_{ILLVT2.5}$, $V_{IHLVT2.5}$ and their details in Table 11). Added the following sections namely DC I2C Specifications, Shield Driver DC Specifications, and DC IDAC Specifications under Electrical Specifications. Updated AC Chip-Level Specifications (Added the parameter namely t_{JIT_IMO} and its details). Updated Ordering Information (updated Table 35).
*D	3510277	YVA/DST	02/16/2012	Added CY8C20x37/37S/47/47S/67/67S part numbers and changed title to "1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders" Updated Features. Modified comparator blocks in Logic Block Diagram. Replaced SmartSense with SmartSense auto-tuning. Added CY8C20xx7S part numbers in Pin Definitions. Added footnote for Table 20. Updated Table 21 and Table 22 and added Table 23. Updated F_{32K1} min value. Updated data hold time min values. Updated CY8C206x7 part information in Table "Emulation and Programming Accessories". Updated Ordering Information.
*E	3539259	DST	03/01/2012	Changed Datasheet status from Preliminary to Final. Updated all Pinouts to include Driven Shield Output (optional) information. Updated Min value for V_{LPC} Table 15. Updated Offset and Input range in Table 16.

Document History Page *(continued)*

<table>
<tr><td colspan="5">Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors
Document Number: 001-69257</td></tr>
<tr><td>Revision</td><td>ECN</td><td>Orig. of Change</td><td>Submission Date</td><td>Description of Change</td></tr>
<tr><td>*F</td><td>3645807</td><td>DST/BVI</td><td>07/03/2012</td><td>Updated F_{SCLK} parameter in the Table 31, "SPI Slave AC Specifications," on page 26
Changed t_{OUT_HIGH} to t_{OUT_H} in Table 30, "SPI Master AC Specifications," on page 25
Updated Features section, "Programmable pin configurations" bullet:
■ Included the following sub-bullet point -
5 mA source current on port 0 and 1 and 1 mA on port 2,3 and 4
■ Changed the bullet point "High sink current of 25 mA for each GPIO" to "High sink current of 25 mA for each GPIO. Total 120 mA maximum sink current per chip"
■ Added "QuietZone™ Controller" bullet and updated "Low power CapSense® block with SmartSense™ auto-tuning" bullet.
Updated package diagrams 001-13937 to *D and 001-57280 to *C revisions.</td></tr>
<tr><td>*G</td><td>3800055</td><td>DST</td><td>11/23/2012</td><td>Changed document title.
Part named changed from CY8C20xx7 to CY8C20xx7/S
Table 20: Update to VIHI2C to match Item #6 in K2 Si Errata document (001-75370)
Updated package diagrams:
51-85068 to *E
001-09116 to *G
001-13937 to *E
001-42168 to *E
001-57280 to *E</td></tr>
<tr><td>*H</td><td>3881332</td><td>SRLI</td><td>02/04/2013</td><td>Updated Features:
Added Note "Please contact your nearest sales office for additional details." and referred the same note in "24 Sensing Inputs – 30-pin WLCSP".</td></tr>
<tr><td>*I</td><td>3993458</td><td>DST</td><td>05/07/2013</td><td>Updated Electrical Specifications (Updated DC GPIO Specifications (Updated heading of third column as "Port 0/1 per I/O (max)" for Table 13)).

Updated Packaging Information:
spec 001-09116 – Changed revision from *G to *H (Figure 17).

Added Errata.</td></tr>
<tr><td>*J</td><td>4081796</td><td>DST</td><td>07/31/2013</td><td>Added Errata footnotes (Note 40, 41, 42, 43, 44).

Updated already existing footnotes (Note 50, 51, 55) as Errata footnotes.

Updated Electrical Specifications:
Updated DC Chip-Level Specifications:
Added Note 40, 41, 42, 43 and referred the same notes in I_{SB0}, I_{SB1}, I_{SBI2C} parameters.
Updated DC GPIO Specifications:
Added Note 44 and referred the same note in description of V_{ILLVT3.3} parameter in Table 10.
Updated DC I2C Specifications:
Updated Note 50, 51 referred in Table 20.
Updated AC I2C Specifications:
Updated Note 55 referred in Table 29.

Updated to new template.</td></tr>
</table>

Document History Page *(continued)*

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors **Document Number: 001-69257**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*O	5122184	JFMD	02/02/2016	Updated Features: Removed Note "Please contact your nearest sales office for additional details." and its reference. Updated Ordering Information: Updated Table 35: Updated part numbers.