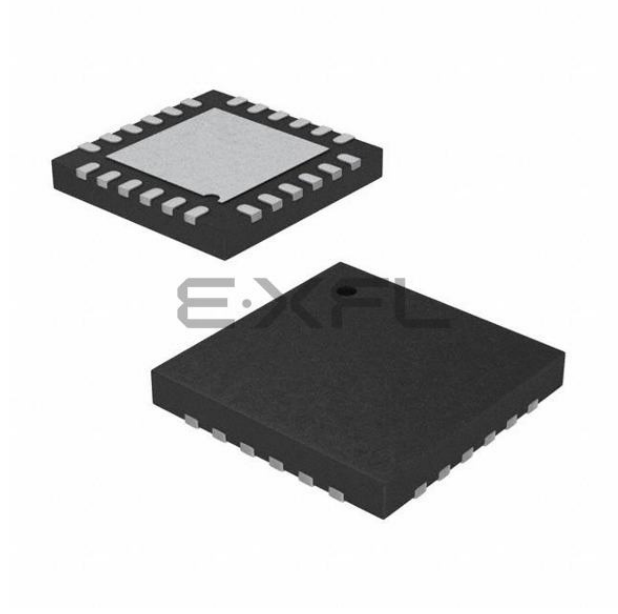

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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

**Embedded - Microcontrollers - Application Specific** represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Active |
| Applications | Capacitive Sensing |
| Core Processor | M8C |
| Program Memory Type | FLASH (8kB) |
| Controller Series | CY8C20xx7/S |
| RAM Size | 1K x 8 |
| Interface | I²C, SPI |
| Number of I/O | 20 |
| Voltage - Supply | 1.71V ~ 5.5V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 24-UFQFN Exposed Pad |
| Supplier Device Package | 24-QFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20337-24lqxi |

### Additional System Resources

System resources provide additional capability, such as configurable $I^2C$ slave, SPI master/slave communication interface, three 16-bit programmable timers, various system resets supported by the M8C low voltage detection and power-on reset. The merits of each system resource are listed here:

- The $I^2C$ slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The $I^2C$ hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The $I^2C$ enhanced slave interface appears as a 32-byte RAM buffer to the external $I^2C$ master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For more details, refer to the I2CSBUF User Module datasheet.
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

## Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20x37/47/67/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

### Application Notes/Design Guides

Application notes and design guides are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/gocapsense. Select Application Notes under the Related Documentation tab.

### Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. See “Development Kits” on page 31.

### Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

### CYPros Consultants

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### Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, create a technical support case or call technical support at 1-800-541-4736.

## Pinouts

The CY8C20x37/47/67/S PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, $V_{SS}$, $V_{DD}$, and XRES are not capable of digital I/O.

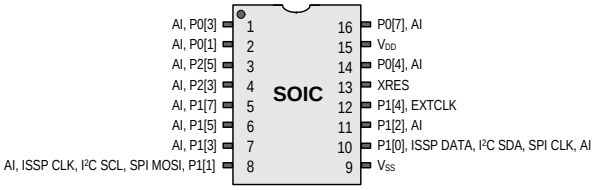
### 16-pin SOIC (10 Sensing Inputs)

**Table 1. Pin Definitions – CY8C20237-24SXI, CY8C20247/S-24SXI** [3]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I | P0[3] | Integrating Input |
| 2 | I/O | I | P0[1] | Integrating Input |
| 3 | I/O | I | P2[5] | Crystal output (XOut) |
| 4 | I/O | I | P2[3] | Crystal input (XIn) |
| 5 | I/O | I | P1[7] | I2C SCL, SPI SS |
| 6 | I/O | I | P1[5] | I2C SDA, SPI MISO |
| 7 | I/O | I | P1[3] | |
| 8 | I/O | I | P1[1] | ISSP CLK[4], I2C SCL, SPI MOSI |
| 9 | Power | | $V_{SS}$ | Ground connection[7] |
| 10 | I/O | I | P1[0] | ISSP DATA[4], I2C SDA, SPI CLK[5] |
| 11 | I/O | I | P1[2] | Driven Shield Output (optional) |
| 12 | I/O | I | P1[4] | Optional external clock (EXTCLK) |
| 13 | INPUT | | XRES | Active high external reset with internal pull-down[6] |
| 14 | I/O | I | P0[4] | |
| 15 | Power | | $V_{DD}$ | Supply voltage |
| 16 | I/O | I | P0[7] | |

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 2. CY8C20237-24SXI, CY8C20247/S-24SXI Device**




**Notes**
3. 13 GPIOs = 10 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
4. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
5. Alternate SPI clock.
6. The internal pull down is 5KOhm.
7. All VSS pins should be brought out to one common GND plane.

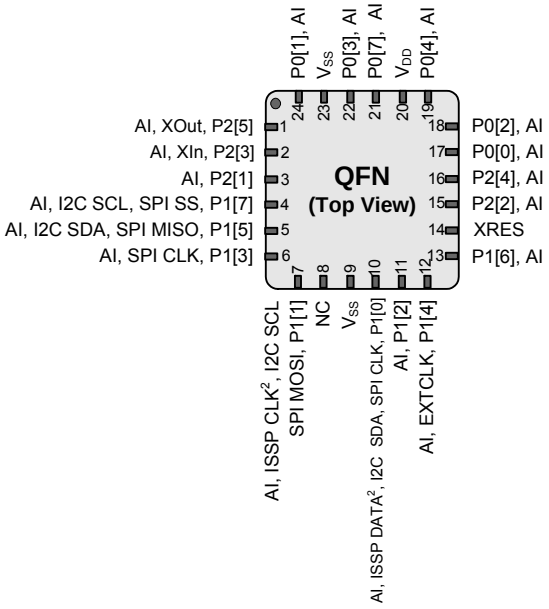
## 24-pin QFN (16 Sensing Inputs)[14]

**Table 3. Pin Definitions – CY8C20337, CY8C20347/S** [15]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | Crystal output (XOut) |
| 2 | I/O | I | P2[3] | Crystal input (XIn) |
| 3 | I/O | I | P2[1] | |
| 4 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| 5 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| 6 | IOHR | I | P1[3] | SPI CLK |
| 7 | IOHR | I | P1[1] | ISSP CLK[16], $I^2C$ SCL, SPI MOSI |
| 8 | | | NC | No connection |
| 9 | Power | | $V_{SS}$ | Ground connection[19] |
| 10 | IOHR | I | P1[0] | ISSP DATA[16], $I^2C$ SDA, SPI CLK[17] |
| 11 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 12 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 13 | IOHR | I | P1[6] | |
| 14 | Input | | XRES | Active high external reset with internal pull-down[18] |
| 15 | I/O | I | P2[2] | Driven Shield Output (optional) |
| 16 | I/O | I | P2[4] | Driven Shield Output (optional) |
| 17 | IOH | I | P0[0] | Driven Shield Output (optional) |
| 18 | IOH | I | P0[2] | Driven Shield Output (optional) |
| 19 | IOH | I | P0[4] | |
| 20 | Power | | $V_{DD}$ | Supply voltage |
| 21 | IOH | I | P0[7] | |
| 22 | IOH | I | P0[3] | Integrating input |
| 23 | Power | | $V_{SS}$ | Ground connection[19] |
| 24 | IOH | I | P0[1] | Integrating input |
| CP | Power | | $V_{SS}$ | Center pad must be connected to ground |

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 4. CY8C20337, CY8C20347/S Device**




**Notes**

14. The center pad (CP) on the QFN package must be connected to ground ($V_{SS}$) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. 19 GPIOs = 16 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
16. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
17. Alternate SPI clock.
18. The internal pull down is 5KOhm.
19. All VSS pins should be brought out to one common GND plane.

### 30-ball WLCSP (24 Sensing Inputs)

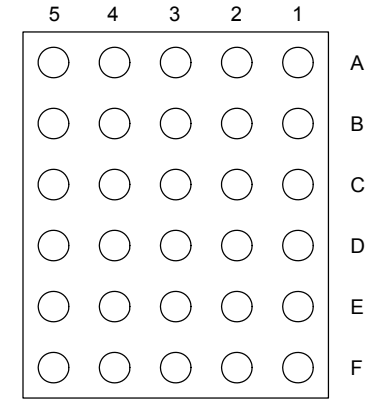
**Table 4. Pin Definitions – CY8C20767, CY8C20747 30-ball Part Pinout (WLCSP)** [20]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| A1 | IOH | I | P0[2] | Driven Shield Output (optional) |
| A2 | IOH | I | P0[6] | |
| A3 | Power | | $V_{DD}$ | Supply voltage |
| A4 | IOH | I | P0[1] | Integrating Input |
| A5 | I/O | I | P2[7] | |
| B1 | I/O | I | P4[2] | |
| B2 | IOH | I | P0[0] | Driven Shield Output (optional) |
| B3 | IOH | I | P0[4] | |
| B4 | IOH | I | P0[3] | Integrating Input |
| B5 | I/O | I | P2[5] | Crystal Output (Xout) |
| C1 | I/O | I | P2[2] | Driven Shield Output (optional) |
| C2 | I/O | I | P2[4] | Driven Shield Output (optional) |
| C3 | I/O | I | P0[7] | |
| C4 | IOH | I | P3[2] | |
| C5 | I/O | I | P2[3] | Crystal Input (Xin) |
| D1 | I/O | I | P2[0] | |
| D2 | I/O | I | P3[0] | |
| D3 | I/O | I | P3[1] | |
| D4 | I/O | I | P3[3] | |
| D5 | I/O | I | P2[1] | |
| E1 | Input | | XRES | Active high external reset with internal pull-down[21] |
| E2 | IOHR | I | P1[6] | |
| E3 | IOHR | I | P1[4] | Optional external clock input (EXT CLK) |
| E4 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| E5 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| F1 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| F2 | IOHR | I | P1[0] | ISSP DATA[22], $I^2C$ SDA, SPI CLK[23] |
| F3 | Power | | $V_{SS}$ | Supply ground[24] |
| F4 | IOHR | I | P1[1] | ISSP CLK[22], $I^2C$ SCL, SPI MOSI |
| F5 | IOHR | I | P1[3] | SPI CLK |

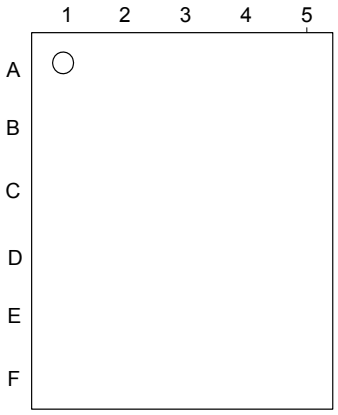
**LEGEND:** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

**Figure 5. CY8C20767, CY8C20747 30-ball WLCSP**

**Bottom View**




**Top View**




**Notes**

20. 27 GPIOs = 24 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
21. The internal pull down is 5KOhm.
22. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
23. Alternate SPI clock.
24. All VSS pins should be brought out to one common GND plane.

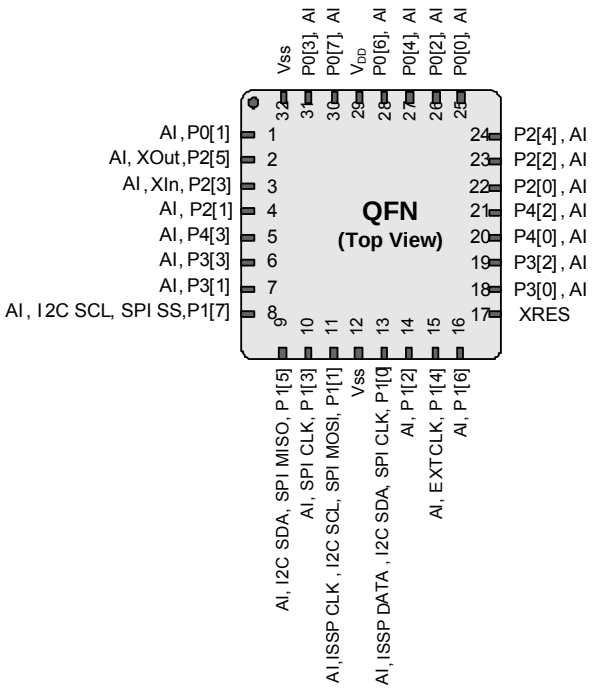
## 32-pin QFN (25 Sensing Inputs)[25]

**Table 5. Pin Definitions – CY8C20437, CY8C20447/S, CY8C20467/S** [26]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IOH | I | P0[1] | Integrating input |
| 2 | I/O | I | P2[5] | Crystal output (XOut) |
| 3 | I/O | I | P2[3] | Crystal input (XIn) |
| 4 | I/O | I | P2[1] | |
| 5 | I/O | I | P4[3] | |
| 6 | I/O | I | P3[3] | |
| 7 | I/O | I | P3[1] | |
| 8 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| 9 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| 10 | IOHR | I | P1[3] | SPI CLK. |
| 11 | IOHR | I | P1[1] | ISSP CLK[27], $I^2C$ SCL, SPI MOSI. |
| 12 | Power | | $V_{SS}$ | Ground connection[30] |
| 13 | IOHR | I | P1[0] | ISSP DATA[27], $I^2C$ SDA, SPI CLK[28] |
| 14 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 15 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 16 | IOHR | I | P1[6] | |
| 17 | Input | | XRES | Active high external reset with internal pull-down[29] |
| 18 | I/O | I | P3[0] | |
| 19 | I/O | I | P3[2] | |
| 20 | I/O | I | P4[0] | |
| 21 | I/O | I | P4[2] | |
| 22 | I/O | I | P2[0] | |
| 23 | I/O | I | P2[2] | Driven Shield Output (optional) |
| 24 | I/O | I | P2[4] | Driven Shield Output (optional) |
| 25 | IOH | I | P0[0] | Driven Shield Output (optional) |
| 26 | IOH | I | P0[2] | Driven Shield Output (optional) |
| 27 | IOH | I | P0[4] | |
| 28 | IOH | I | P0[6] | |
| 29 | Power | | $V_{DD}$ | |
| 30 | IOH | I | P0[7] | |
| 31 | IOH | I | P0[3] | Integrating input |
| 32 | Power | | $V_{SS}$ | Ground connection[30] |
| CP | Power | | $V_{SS}$ | Center pad must be connected to ground |

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 6. CY8C20437, CY8C20447/S, CY8C20467/S Device**




**Notes**

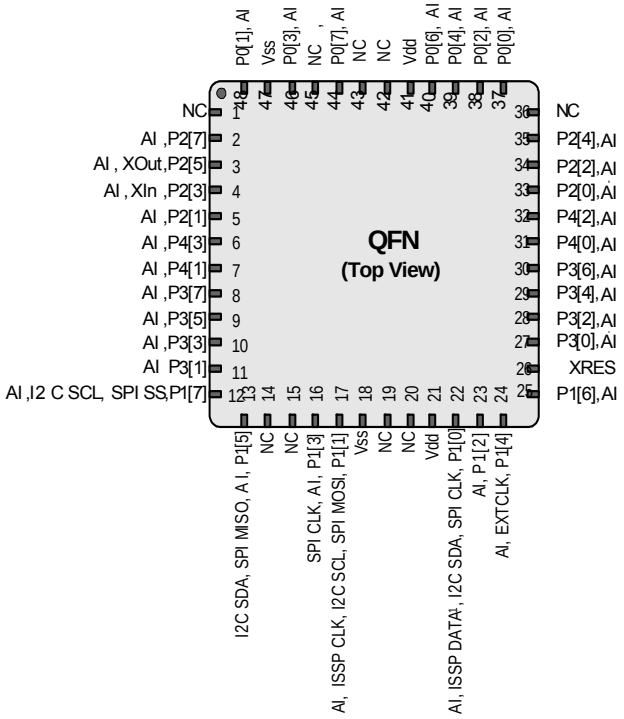
25. The center pad (CP) on the QFN package must be connected to ground ($V_{SS}$) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
26. 28 GPIOs = 25 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
27. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
28. Alternate SPI clock.
29. The internal pull down is 5KOhm.
30. All VSS pins should be brought out to one common GND plane.

## 48-pin QFN (31 Sensing Inputs)[31]

**Table 6. Pin Definitions – CY8C20637, CY8C20647/S, CY8C20667/S** [32]

| Pin No. | Digital | Analog | Name | Description |
|---|---|---|---|---|
| 1 | | | NC | No connection |
| 2 | I/O | I | P2[7] | |
| 3 | I/O | I | P2[5] | Crystal output (XOut) |
| 4 | I/O | I | P2[3] | Crystal input (XIn) |
| 5 | I/O | I | P2[1] | |
| 6 | I/O | I | P4[3] | |
| 7 | I/O | I | P4[1] | |
| 8 | I/O | I | P3[7] | |
| 9 | I/O | I | P3[5] | |
| 10 | I/O | I | P3[3] | |
| 11 | I/O | I | P3[1] | |
| 12 | IOHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| 13 | IOHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| 14 | | | NC | No connection |
| 15 | | | NC | No connection |
| 16 | IOHR | I | P1[3] | SPI CLK |
| 17 | IOHR | I | P1[1] | ISSP CLK[33], $I^2C$ SCL, SPI MOSI |
| 18 | Power | | $V_{SS}$ | Ground connection[36] |
| 19 | | | NC | No connection |
| 20 | | | NC | No connection |
| 21 | Power | | $V_{DD}$ | Supply voltage |
| 22 | IOHR | I | P1[0] | ISSP DATA[33], $I^2C$ SDA, SPI CLK[34] |
| 23 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 24 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 25 | IOHR | I | P1[6] | |
| 26 | Input | | XRES | Active high external reset with internal pull-down[35] |
| 27 | I/O | I | P3[0] | |
| 28 | I/O | I | P3[2] | |
| 29 | I/O | I | P3[4] | |
| 30 | I/O | I | P3[6] | |
| 31 | I/O | I | P4[0] | |
| 32 | I/O | I | P4[2] | |
| 33 | I/O | I | P2[0] | |
| 34 | I/O | I | P2[2] | Driven Shield Output (optional) |
| 35 | I/O | I | P2[4] | Driven Shield Output (optional) |
| 36 | | | NC | No connection |
| 37 | IOH | I | P0[0] | Driven Shield Output (optional) |
| 38 | IOH | I | P0[2] | Driven Shield Output (optional) |
| 39 | IOH | I | P0[4] | |

**Figure 7. CY8C20637, CY8C20647/S, CY8C20667/S Device**




| Pin No. | Digital | Analog | Name | Description |
|---|---|---|---|---|
| 40 | IOH | I | P0[6] | |
| 41 | Power | | $V_{DD}$ | Supply voltage |
| 42 | | | NC | No connection |
| 43 | | | NC | No connection |
| 44 | IOH | I | P0[7] | |
| 45 | | | NC | No connection |
| 46 | IOH | I | P0[3] | Integrating input |
| 47 | Power | | $V_{SS}$ | Ground connection[36] |
| 48 | IOH | I | P0[1] | Integrating input |
| CP | Power | | $V_{SS}$ | Center pad must be connected to ground |

**LEGEND** A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

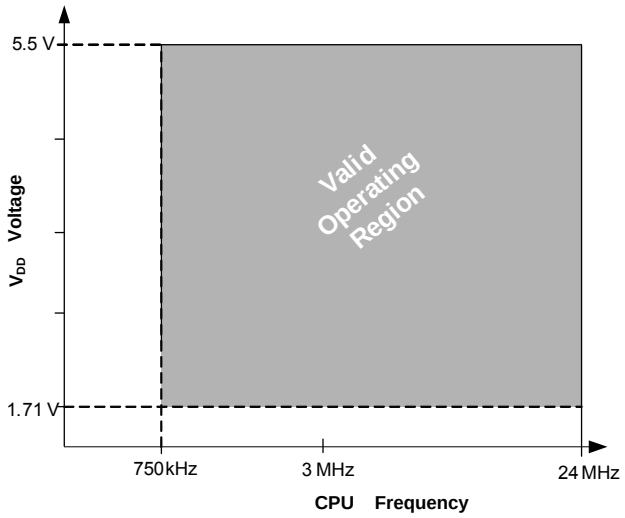
**Notes**

31. The center pad (CP) on the QFN package must be connected to ground ($V_{SS}$) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
32. 34 GPIOs = 31 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.
33. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the $I^2C$ bus. Use alternate pins if you encounter issues.
34. Alternate SPI clock.
35. The internal pull down is 5KOhm.
36. All VSS pins should be brought out to one common GND plane.

## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x37/47/67/S PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at http://www.cypress.com/psoc.

**Figure 8. Voltage versus CPU Frequency**




### Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 7. Absolute Maximum Ratings**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability. | –55 | +25 | +125 | °C |
| $V_{DD}$ | Supply voltage relative to $V_{SS}$ | – | –0.5 | – | +6.0 | V |
| $V_{IO}$ | DC input voltage | – | $V_{SS}$ – 0.5 | – | $V_{DD}$ + 0.5 | V |
| $V_{IOZ}$ | DC voltage applied to tristate | – | $V_{SS}$ – 0.5 | – | $V_{DD}$ + 0.5 | V |
| $I_{MIO}$ | Maximum current into any port pin | – | –25 | – | +50 | mA |
| ESD | Electro static discharge voltage | Human body model ESD | 2000 | – | – | V |
| LU | Latch up current | In accordance with JESD78 standard | – | – | 200 | mA |

### Operating Temperature

**Table 8. Operating Temperature**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | – | –40 | – | +85 | °C |
| $T_C$ | Commercial temperature range | – | 0 | | 70 | °C |
| $T_J$ | Operational die temperature | The temperature rise from ambient to junction is package specific. See the Thermal Impedances on page 30. The user must limit the power consumption to comply with this requirement. | –40 | – | +100 | °C |

## DC Chip-Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 9. DC Chip-Level Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ [37, 38, 39] | Supply voltage | See Table 14 on page 17. | 1.71 | – | 5.50 | V |
| $I_{DD24}$ | Supply current, IMO = 24 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 2.88 | 4.00 | mA |
| $I_{DD12}$ | Supply current, IMO = 12 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 1.71 | 2.60 | mA |
| $I_{DD6}$ | Supply current, IMO = 6 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current | – | 1.16 | 1.80 | mA |
| $I_{SB0}$ [40, 41, 42, 43] | Deep sleep current | $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off | – | 0.10 | 1.1 | µA |
| $I_{SB1}$ [40, 41, 42, 43] | Standby current with POR, LVD and sleep timer | $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off | – | 1.07 | 1.50 | µA |
| $I_{SBI2C}$ [40, 41, 42, 43] | Standby current with $I^2C$ enabled | Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz | – | 1.64 | – | µA |

**Notes**

37. When $V_{DD}$ remains in the range from 1.71 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the $SR_{POWER\_UP}$ parameter.
38. If powering down in standby sleep mode, to properly detect and recover from a $V_{DD}$ brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that $V_{DD}$ falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of $V_{DD}$ is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the Technical Reference Manual. In deep sleep/standby sleep mode, additional low power voltage monitoring circuitry allows $V_{DD}$ brown out conditions to be detected and resets the device when $V_{DD}$ goes lower than 1.1 V at edge rates slower than 1 V/ms.
39. For proper CapSense block functionality, if the drop in $V_{DD}$ exceeds 5% of the base $V_{DD}$, the rate at which $V_{DD}$ drops should not exceed 200 mV/s. Base $V_{DD}$ can be between 1.8 V and 5.5 V.
40. Errata: When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the “Errata” on page 37.
41. Errata: When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the “Errata” on page 37.
42. Errata: If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the “Errata” on page 37.
43. Errata: Device wakes up from sleep when an analog interrupt is trigger. For more information, see the “Errata” on page 37.

**Table 11. 2.4 V to 3.0 V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| $V_{OH1}$ | High output voltage Port 2 or 3 pins | $I_{OH}$ < 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.20 | – | – | V |
| $V_{OH2}$ | High output voltage Port 2 or 3 Pins | $I_{OH}$ = 0.2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.40 | – | – | V |
| $V_{OH3}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | $I_{OH}$ < 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.20 | – | – | V |
| $V_{OH4}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | $I_{OH}$ = 2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.50 | – | – | V |
| $V_{OH5A}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | $I_{OH}$ < 10 µA, $V_{DD}$ > 2.4 V, maximum of 20 mA source current in all I/Os | 1.50 | 1.80 | 2.10 | V |
| $V_{OH6A}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | $I_{OH}$ = 1 mA, $V_{DD}$ > 2.4 V, maximum of 20 mA source current in all I/Os | 1.20 | – | – | V |
| $V_{OL}$ | Low output voltage | $I_{OL}$ = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| $V_{IL}$ | Input low voltage | – | – | – | 0.72 | V |
| $V_{IH}$ | Input high voltage | – | $V_{DD}$ × 0.65 | – | $V_{DD}$ + 0.7 | V |
| $V_H$ | Input hysteresis voltage | – | – | 80 | – | mV |
| $I_{IL}$ | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| $C_{PIN}$ | Capacitive load on pins | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |
| $V_{ILLVT2.5}$ | Input Low Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 0.7 | V | – | |
| $V_{IHLVT2.5}$ | Input High Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 1.2 | | – | V |

**Table 12. 1.71 V to 2.4 V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| $V_{OH1}$ | High output voltage Port 2 or 3 pins | $I_{OH}$ = 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH2}$ | High output voltage Port 2 or 3 pins | $I_{OH}$ = 0.5 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.50 | – | – | V |
| $V_{OH3}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | $I_{OH}$ = 100 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH4}$ | High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | $I_{OH}$ = 2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.50 | – | – | V |

## AC Programming Specifications

**Figure 10. AC Waveform**

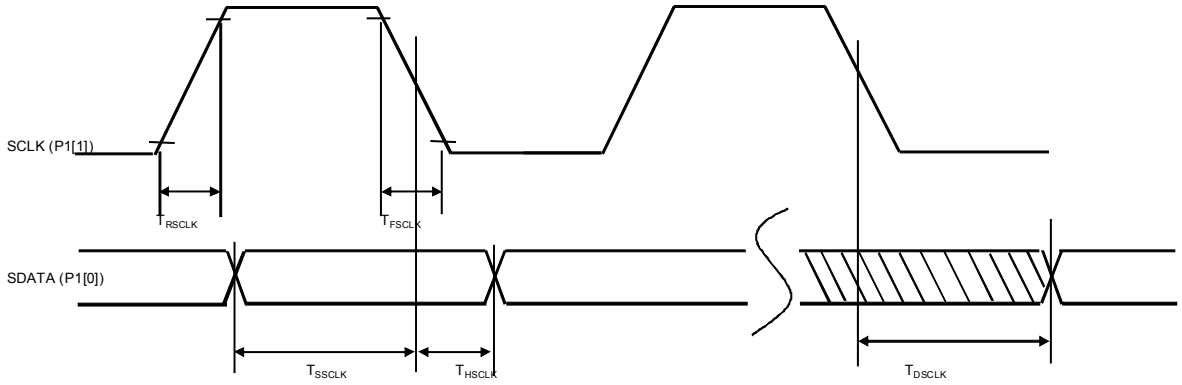



Table 28 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 28. AC Programming Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{RSCLK}$ | Rise time of SCLK | – | 1 | – | 20 | ns |
| $t_{FSCLK}$ | Fall time of SCLK | – | 1 | – | 20 | ns |
| $t_{SSCLK}$ | Data setup time to falling edge of SCLK | – | 40 | – | – | ns |
| $t_{HSCLK}$ | Data hold time from falling edge of SCLK | – | 40 | – | – | ns |
| $F_{SCLK}$ | Frequency of SCLK | – | 0 | – | 8 | MHz |
| $t_{ERASEB}$ | Flash erase time (block) | – | – | – | 18 | ms |
| $t_{WRITE}$ | Flash block write time | – | – | – | 25 | ms |
| $t_{DSCLK}$ | Data out delay from falling edge of SCLK | $3.6 < V_{DD}$ | – | – | 60 | ns |
| $t_{DSCLK3}$ | Data out delay from falling edge of SCLK | $3.0 \le V_{DD} \le 3.6$ | – | – | 85 | ns |
| $t_{DSCLK2}$ | Data out delay from falling edge of SCLK | $1.71 \le V_{DD} \le 3.0$ | – | – | 130 | ns |
| $t_{XRST3}$ | External reset pulse width after power-up | Required to enter programming mode when coming out of sleep | 300 | – | – | µs |
| $t_{XRES}$ | XRES pulse length | – | 300 | – | – | µs |
| $t_{VDDWAIT}$[54] | $V_{DD}$ stable to wait-and-poll hold off | – | 0.1 | – | 1 | ms |
| $t_{VDDXRES}$[54] | $V_{DD}$ stable to XRES assertion delay | – | 14.27 | – | – | ms |
| $t_{POLL}$ | SDAT high pulse time | – | 0.01 | – | 200 | ms |
| $t_{ACQ}$[54] | “Key window” time after a $V_{DD}$ ramp acquire event, based on 256 ILO clocks. | – | 3.20 | – | 19.60 | ms |
| $t_{XRESINI}$[54] | “Key window” time after an XRES event, based on 8 ILO clocks | – | 98 | – | 615 | µs |

**Note**
54. Valid from 5 to 50 °C. See the spec, CY8C20X66, CY8C20X46, CY8C20X36, CY7C643XX, CY7C604XX, CY8CTST2XX, CY8CTMG2XX, CY8C20X67, CY8C20X47, CY8C20X37, Programming Spec for more details.

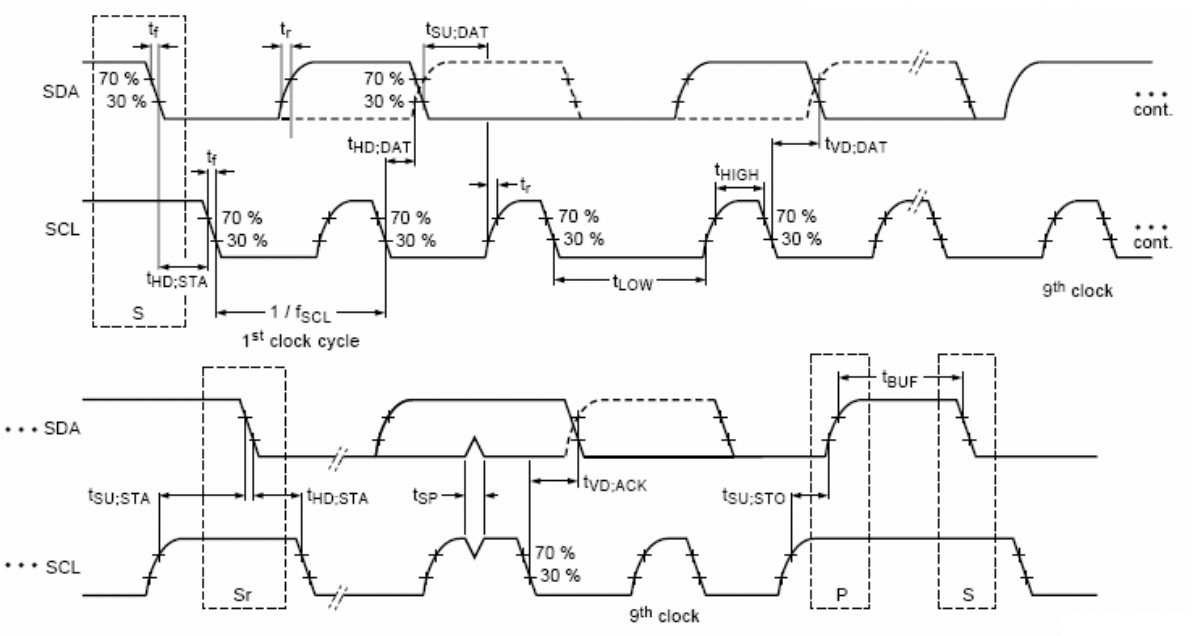
## AC I²C Specifications

Table 29 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 29. AC Characteristics of the I²C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0 | – | 0.6 | – | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | – | 1.3 | – | µs |
| $t_{HIGH}$ | HIGH Period of the SCL clock | 4.0 | – | 0.6 | – | µs |
| $t_{SU;STA}$ | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | µs |
| $t_{HD;DAT}$[55] | Data hold time | 20 | 3.45 | 20 | 0.90 | µs |
| $t_{SU;DAT}$ | Data setup time | 250 | – | 100[56] | – | ns |
| $t_{SU;STO}$ | Setup time for STOP condition | 4.0 | – | 0.6 | – | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | µs |
| $t_{SP}$ | Pulse width of spikes are suppressed by the input filter | – | – | 0 | 50 | ns |

**Figure 11. Definition for Timing for Fast/Standard Mode on the I²C Bus**




**Notes**

55. Errata: To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. For more information see item #5 in the "Errata" on page 37.
56. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

**Table 30. SPI Master AC Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{SCLK}$ | SCLK clock frequency | $V_{DD} \geq 2.4$ V<br>$V_{DD} < 2.4$ V | –<br>– | –<br>– | 6<br>3 | MHz<br>MHz |
| DC | SCLK duty cycle | – | – | 50 | – | % |
| $t_{SETUP}$ | MISO to SCLK setup time | $V_{DD} \geq 2.4$ V<br>$V_{DD} < 2.4$ V | 60<br>100 | –<br>– | –<br>– | ns<br>ns |
| $t_{HOLD}$ | SCLK to MISO hold time | – | 40 | – | – | ns |
| $t_{OUT\_VAL}$ | SCLK to MOSI valid time | – | – | – | 40 | ns |
| $t_{OUT\_H}$ | MOSI high time | – | 40 | – | – | ns |

**Figure 12. SPI Master Mode 0 and 2**

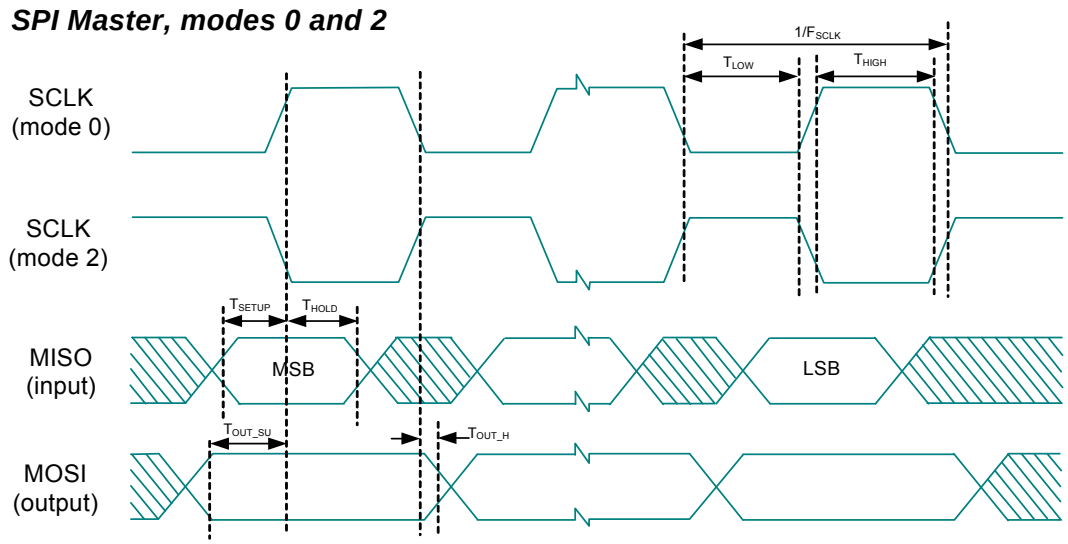
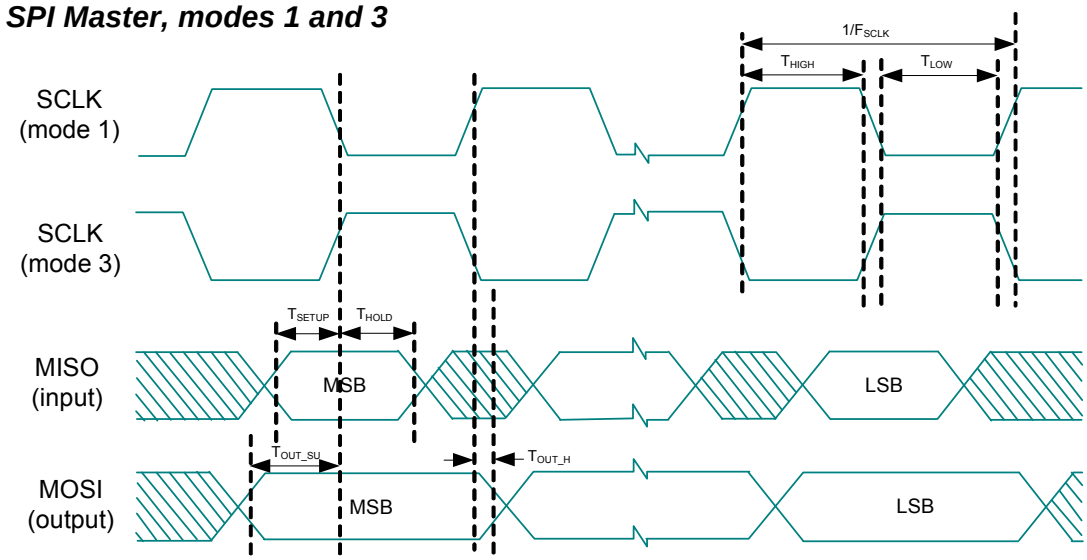



**Figure 13. SPI Master Mode 1 and 3**



## Development Tool Selection

### Software

*PSoC Designer™*

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, in-system programming support, and built-in support for third-party assemblers and C compilers. PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler.

*PSoC Designer Software Subsystems*

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

**Assemblers.** The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*PSoC Programmer*

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube in-circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at http://www.cypress.com/psocprogrammer.

### Development Kits

All development kits are sold at the Cypress Online Store.

### Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

*CY3210-MiniProg1*

The CY3210-MiniProg1 kit allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- 28-pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

*CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

## Ordering Information

Table 35 lists the CY8C20x37/47/67/S PSoC devices' key package features and ordering codes.

**Table 35. PSoC Device Key Features and Ordering Information**

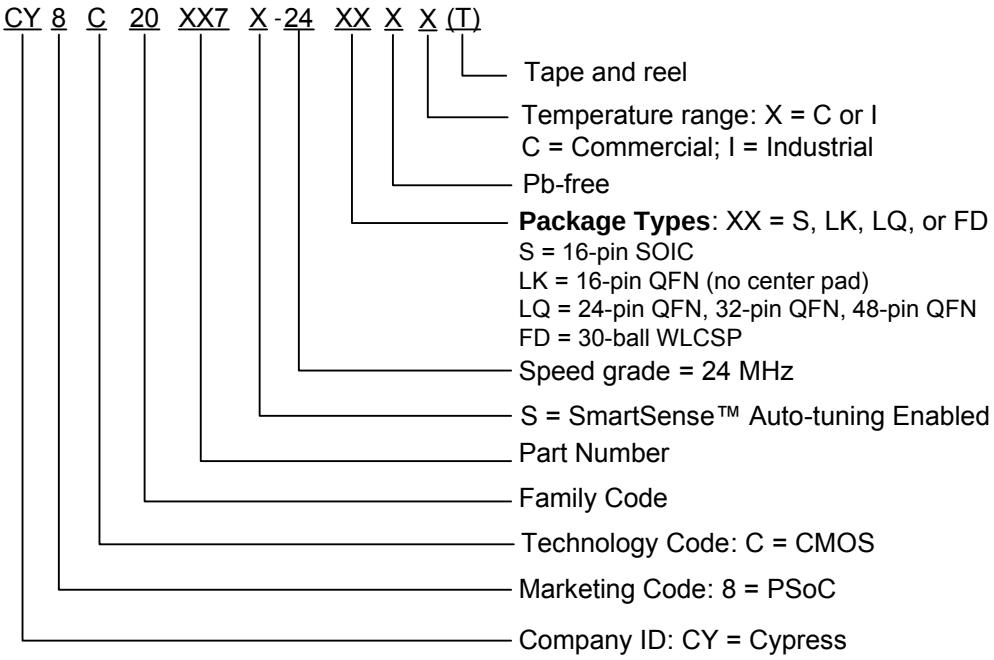
| Ordering Code | Package | Flash (Bytes) | SRAM (Bytes) | CapSense Sensors | Digital I/O Pins | Analog Inputs [59] | XRES Pin | ADC |
|---|---|---|---|---|---|---|---|---|
| CY8C20237-24SXI | 16-pin SOIC | 8 K | 1 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20247S-24SXI | 16-pin SOIC | 16 K | 2 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20237-24LKXI | 16-pin QFN | 8 K | 1 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20237-24LKXIT | 16-pin QFN (Tape and Reel) | 8 K | 1 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20247S-24LKXI | 16-pin QFN | 16 K | 2 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20247S-24LKXIT | 16-pin QFN (Tape and Reel) | 16 K | 2 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20337-24LQXI | 24-pin QFN | 8 K | 1 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20337-24LQXIT | 24-pin QFN (Tape and Reel) | 8 K | 1 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347-24LQXI | 24-pin QFN | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347-24LQXIT | 24-pin QFN (Tape and Reel) | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347S-24LQXI | 24-pin QFN | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347S-24LQXIT | 24-pin QFN (Tape and Reel) | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20437-24LQXI | 32-pin QFN | 8 K | 1 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20437-24LQXIT | 32-pin QFN (Tape and Reel) | 8 K | 1 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447-24LQXI | 32-pin QFN | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447-24LQXIT | 32-pin QFN (Tape and Reel) | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447S-24LQXI | 32-pin QFN | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447S-24LQXIT | 32-pin QFN (Tape and Reel) | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467-24LQXI | 32-pin QFN | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467-24LQXIT | 32-pin QFN (Tape and Reel) | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467S-24LQXI | 32-pin QFN | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467S-24LQXIT | 32-pin QFN (Tape and Reel) | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20637-24LQXI | 48-pin QFN | 8 K | 1 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20637-24LQXIT | 48-pin QFN (Tape and Reel) | 8 K | 1 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647-24LQXI | 48-pin QFN | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647-24LQXIT | 48-pin QFN (Tape and Reel) | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647S-24LQXI | 48-pin QFN | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647S-24LQXIT | 48-pin QFN (Tape and Reel) | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667-24LQXI | 48-pin QFN | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667-24LQXIT | 48-pin QFN (Tape and Reel) | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667S-24LQXI | 48-pin QFN | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667S-24LQXIT | 48-pin QFN (Tape and Reel) | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |

**Note**
59. Dual-function Digital I/O Pins also connect to the common analog mux.

**Table 35. PSoC Device Key Features and Ordering Information** *(continued)*

| Ordering Code | Package | Flash (Bytes) | SRAM (Bytes) | CapSense Sensors | Digital I/O Pins | Analog Inputs [59] | XRES Pin | ADC |
|---|---|---|---|---|---|---|---|---|
| CY8C20767-24FDXC | 30-pin WLCSP | 32 K | 2 K | 24 | 27 | 27 | Yes | Yes |
| CY8C20767-24FDXCT | 30-pin WLCSP (Tape and Reel) | 32 K | 2 K | 24 | 27 | 27 | Yes | Yes |

## Ordering Code Definitions



## Acronyms

The following table lists the acronyms that are used in this document.

**Table 36. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CMOS | complementary metal oxide semiconductor |
| CPU | central processing unit |
| DAC | digital-to-analog converter |
| DC | direct current |
| ESD | electrostatic discharge |
| FSR | full scale range |
| GPIO | general purpose input/output |
| $I^2C$ | inter-integrated circuit |
| ICE | in-circuit emulator |
| ILO | internal low speed oscillator |
| IMO | internal main oscillator |
| I/O | input/output |
| ISSP | in-system serial programming |
| LCD | liquid crystal display |
| LDO | low dropout (regulator) |
| LED | light-emitting diode |
| LPC | low power comparator |
| LSB | least-significant bit |
| LVD | low voltage detect |
| MCU | micro-controller unit |
| MIPS | million instructions per second |
| MISO | master in slave out |
| MOSI | master out slave in |
| MSB | most-significant bit |
| OCD | on-chip debug |
| PCB | printed circuit board |
| POR | power on reset |
| PSRR | power supply rejection ratio |
| PWRSYS | power system |
| PSoC | programmable system-on-chip |
| QFN | quad flat no-lead |
| SCLK | serial $I^2C$ clock |
| SDA | serial $I^2C$ data |
| SDATA | serial ISSP data |
| SOIC | small outline integrated circuit |
| SPI | serial peripheral interface |
| SRAM | static random access memory |
| SS | slave select |
| USB | universal serial bus |
| WLCSP | wafer level chip scale package |

## Reference Documents

- *Technical reference manual for CY20xx7 devices*
- *In-system Serial Programming (ISSP) protocol for 20xx7*
- *Host Sourced Serial Programming for 20xx7 devices*

## Document Conventions

### Units of Measure

Table 37 lists all the abbreviations used to measure the PSoC devices.

**Table 37. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| dB | decibel |
| kHz | kilohertz |
| ksps | kilo samples per second |
| kΩ | kilohm |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

# Errata

This section describes the errata for the CY8C20xx7/S family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

## CY8C20xx7/S Qualification Status

Product Status: Production released.

## CY8C20xx7/S Errata Summary

The following Errata items apply to the CY8C20xx7/S datasheet 001-69257.

### 1. DoubleTimer0 ISR

**■Problem Definition**

When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

**■Parameters Affected**

No datasheet parameters are affected.

**■Trigger Condition(S)**

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

**■Scope of Impact**

The ISR may be executed twice.

**■Workaround**

In the ISR, firmware should clear the one-shot bit with a statement such as “`and reg[B0h], FDh`”

**■Fix Status**

Will not be fixed

**■Changes**

None

### 2. Missed GPIO Interrupt

**■Problem Definition**

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

**■Parameters Affected**

No datasheet parameters are affected.

**■Trigger Condition(S)**

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

**■Scope of Impact**

The GPIO interrupt service routine will not be run.

**■Workaround**

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt.

Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0.

Alternatively, the ISR’s for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

**■Fix Status**

Will not be fixed

**■Changes**

None

## Document History Page

| Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors<br>Document Number: 001-69257 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 3276782 | DST | 06/27/2011 | New silicon and document |
| *A | 3327230 | DST | 07/28/2011 | Changed 48-pin dimensions to 6 × 6 × 0.6 mm QFN<br>Updated pins name in Table 3 on page 9 and removed USB column and updated dimensions for 48-pin parts in Table 35 on page 33<br>Updated Figure 20 on page 29<br>Removed ICE and Debugger sections.<br>Removed CY3215 Development Kit and CY3280-20x66 UCC sections.<br>Updated Ordering Information. |
| *B | 3403111 | YVA | 10/12/2011 | Moved status from Advance to Preliminary.<br>Updated Ordering Information<br>Removed the row named “48-Pin (6 × 6 mm) QFN (OCD)”.<br>Changed all 48-pin ordering code column from CY8C20XXX-24LTxx to CY8C20XXX-24LQxx.<br>Updated 16-pin SOIC and 16-pin QFN package drawings. |
| *C | 3473317 | DST | 12/23/2011 | Updated Features.<br>Updated Pinouts (Removed PSoC in captions of Figure 2, Figure 3, Figure 4, Figure 6, and Figure 7).<br>Updated DC Chip-Level Specifications under Electrical Specifications (Updated typical value of $I_{DD24}$ parameter from 3.32 mA to 2.88 mA, updated typical value of $I_{DD12}$ parameter from 1.86 mA to 1.71 mA, updated typical value of $I_{DD6}$ parameter from 1.13 mA to 1.16 mA, updated maximum value of $I_{SB0}$ parameter from 0.50 µA to 1.1 µA, added $I_{SBI2C}$ parameter and its details).<br>Updated DC GPIO Specifications under Electrical Specifications (Added the parameters namely $V_{ILLVT3.3}$, $V_{IHLVT3.3}$, $V_{ILLVT5.5}$, $V_{IHLVT5.5}$ and their details in Table 10, added the parameters namely $V_{ILLVT2.5}$, $V_{IHLVT2.5}$ and their details in Table 11).<br>Added the following sections namely DC I2C Specifications, Shield Driver DC Specifications, and DC IDAC Specifications under Electrical Specifications.<br>Updated AC Chip-Level Specifications (Added the parameter namely $t_{JIT\_IMO}$ and its details).<br>Updated Ordering Information (updated Table 35). |
| *D | 3510277 | YVA/DST | 02/16/2012 | Added CY8C20x37/37S/47/47S/67/67S part numbers and changed title to “1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders”<br>Updated Features.<br>Modified comparator blocks in Logic Block Diagram.<br>Replaced SmartSense with SmartSense auto-tuning.<br>Added CY8C20xx7S part numbers in Pin Definitions.<br>Added footnote for Table 20.<br>Updated Table 21 and Table 22 and added Table 23.<br>Updated $F_{32K1}$ min value.<br>Updated data hold time min values.<br>Updated CY8C206x7 part information in Table “Emulation and Programming Accessories”.<br>Updated Ordering Information. |
| *E | 3539259 | DST | 03/01/2012 | Changed Datasheet status from Preliminary to Final.<br>Updated all Pinouts to include Driven Shield Output (optional) information.<br>Updated Min value for $V_{LPC}$ Table 15.<br>Updated Offset and Input range in Table 16. |

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|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *F | 3645807 | DST/BVI | 07/03/2012 | Updated $F_{SCLK}$ parameter in the Table 31, “SPI Slave AC Specifications,” on page 26<br>Changed $t_{OUT\_HIGH}$ to $t_{OUT\_H}$ in Table 30, “SPI Master AC Specifications,” on page 25<br>Updated Features section, “Programmable pin configurations” bullet:<br>■ Included the following sub-bullet point - 5 mA source current on port 0 and 1 and 1 mA on port 2,3 and 4<br>■ Changed the bullet point “High sink current of 25 mA for each GPIO” to “High sink current of 25 mA for each GPIO. Total 120 mA maximum sink current per chip”<br>■ Added “QuietZone™ Controller” bullet and updated “Low power CapSense® block with SmartSense™ auto-tuning” bullet.<br>Updated package diagrams 001-13937 to *D and 001-57280 to *C revisions. |
| *G | 3800055 | DST | 11/23/2012 | Changed document title.<br>Part named changed from CY8C20xx7 to CY8C20xx7/S<br>Table 20: Update to VIHI2C to match Item #6 in K2 Si Errata document (001-75370)<br>Updated package diagrams:<br>51-85068 to *E<br>001-09116 to *G<br>001-13937 to *E<br>001-42168 to *E<br>001-57280 to *E |
| *H | 3881332 | SRLI | 02/04/2013 | Updated Features:<br>Added Note “Please contact your nearest sales office for additional details.” and referred the same note in “24 Sensing Inputs – 30-pin WLCSP”. |
| *I | 3993458 | DST | 05/07/2013 | Updated Electrical Specifications (Updated DC GPIO Specifications (Updated heading of third column as “Port 0/1 per I/O (max)” for Table 13)).<br><br>Updated Packaging Information:<br>spec 001-09116 – Changed revision from *G to *H (Figure 17).<br><br>Added Errata. |
| *J | 4081796 | DST | 07/31/2013 | Added Errata footnotes (Note 40, 41, 42, 43, 44).<br><br>Updated already existing footnotes (Note 50, 51, 55) as Errata footnotes.<br><br>Updated Electrical Specifications:<br>Updated DC Chip-Level Specifications:<br>Added Note 40, 41, 42, 43 and referred the same notes in $I_{SB0}$, $I_{SB1}$, $I_{SBI2C}$ parameters.<br>Updated DC GPIO Specifications:<br>Added Note 44 and referred the same note in description of $V_{ILLVT3.3}$ parameter in Table 10.<br>Updated DC I2C Specifications:<br>Updated Note 50, 51 referred in Table 20.<br>Updated AC I2C Specifications:<br>Updated Note 55 referred in Table 29.<br><br>Updated to new template. |

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|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *K | 4248645 | DST | 01/16/2014 | Updated Pinouts:<br>Updated 32-pin QFN (25 Sensing Inputs)[25]:<br>Updated Figure 6.<br><br>Updated Packaging Information:<br>spec 001-09116 – Changed revision from *H to *I. |
| *L | 4404150 | SLAN | 06/10/2014 | Updated Pinouts:<br>Updated 16-pin SOIC (10 Sensing Inputs):<br>Updated Table 1:<br>Added Note 6 and referred the same note in description of XRES pin.<br>Updated 16-pin QFN (10 Sensing Inputs)[8]:<br>Updated Table 2:<br>Added Note 12 and referred the same note in description of XRES pin.<br>Updated 24-pin QFN (16 Sensing Inputs)[14]:<br>Updated Table 3:<br>Added Note 18 and referred the same note in description of XRES pin.<br>Updated 30-ball WLCSP (24 Sensing Inputs):<br>Updated Table 4:<br>Added Note 21 and referred the same note in description of XRES pin.<br>Updated 32-pin QFN (25 Sensing Inputs)[25]:<br>Updated Table 5:<br>Added Note 29 and referred the same note in description of XRES pin.<br>Updated 48-pin QFN (31 Sensing Inputs)[31]:<br>Updated Table 6:<br>Added Note 35 and referred the same note in description of XRES pin.<br><br>Updated Electrical Specifications:<br>Updated DC GPIO Specifications:<br>Updated Table 10:<br>Updated minimum and maximum values of $V_{IH}$ parameter.<br>Updated Table 11:<br>Updated minimum and maximum values of $V_{IH}$ parameter.<br>Updated AC Chip-Level Specifications:<br>Updated Table 24:<br>Removed minimum and maximum values of “ILO untrimmed frequency”.<br><br>Updated Packaging Information:<br>spec 001-09116 – Changed revision from *I to *J.<br><br>Completing Sunset Review. |
| *M | 4825924 | SLAN | 07/07/2015 | Added the footnote “All VSS pins should be brought out to one common GND plane” in pinout tables (Table 1 through Table 6).<br>Updated Packaging Information:<br>spec 001-13937 – Changed revision from *E to *F.<br>Updated to new template. |
| *N | 5068999 | ARVI | 12/31/2015 | Updated hyperlink of “Technical Reference Manual” in all instances across the document.<br>Updated PSoC® Functional Overview:<br>Updated Additional System Resources:<br>Updated description.<br>Updated Development Tool Selection:<br>Removed “Accessories (Emulation and Programming)”.<br>Removed “Build a PSoC Emulator into Your Board”. |