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[Embedded - Microcontrollers - Application Specific](#) represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

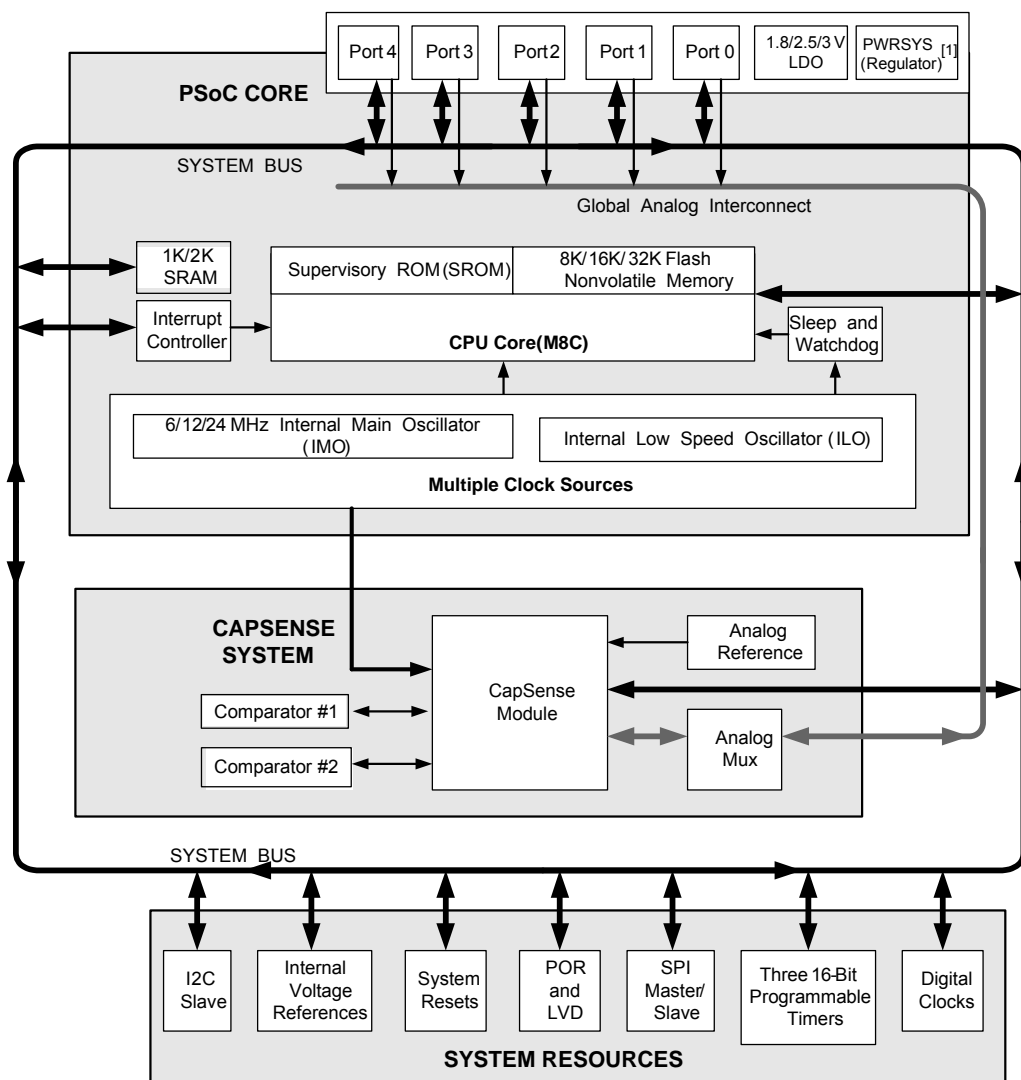
### What Are [Embedded - Microcontrollers - Application Specific](#)?

Application specific microcontrollers are engineered to

#### Details

Product Status	Active
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (8kB)
Controller Series	CY8C20xx7/S
RAM Size	1K x 8
Interface	I <sup>2</sup> C, SPI
Number of I/O	29
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20437-24lqxi">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20437-24lqxi</a>

## Logic Block Diagram



### Note

1. Internal voltage regulator for internal circuitry

## Additional System Resources

System resources provide additional capability, such as configurable I<sup>2</sup>C slave, SPI master/slave communication interface, three 16-bit programmable timers, various system resets supported by the M8C low voltage detection and power-on reset. The merits of each system resource are listed here:

- The I<sup>2</sup>C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I<sup>2</sup>C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I<sup>2</sup>C enhanced slave interface appears as a 32-byte RAM buffer to the external I<sup>2</sup>C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For more details, refer to the [I2CSBUF User Module datasheet](#).
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

## Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for the CY8C20x37/47/67/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at [www.cypress.com/psoc](http://www.cypress.com/psoc).

## Application Notes/Design Guides

Application notes and design guides are an excellent introduction to the wide variety of possible PSoC designs. They are located at [www.cypress.com/gocapsense](http://www.cypress.com/gocapsense). Select Application Notes under the Related Documentation tab.

## Development Kits

PSoC Development Kits are available online from Cypress at [www.cypress.com/shop](http://www.cypress.com/shop) and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. See “[Development Kits](#)” on page 31.

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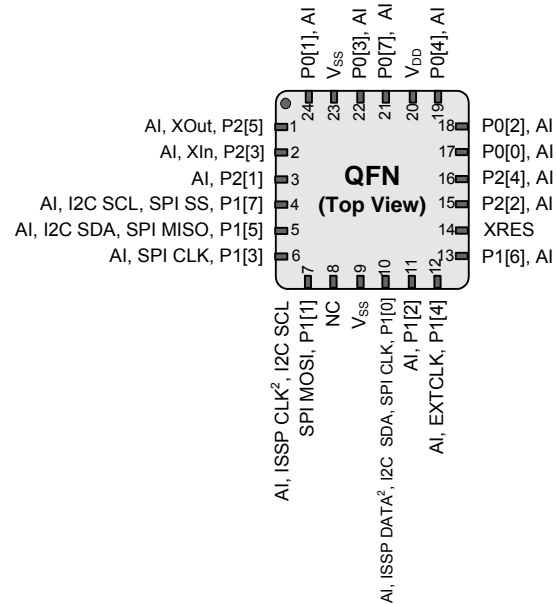
**24-pin QFN (16 Sensing Inputs)<sup>[14]</sup>**
**Table 3. Pin Definitions – CY8C20337, CY8C20347/S<sup>[15]</sup>**

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS
5	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK <sup>[16]</sup> , I <sup>2</sup> C SCL, SPI MOSI
8			NC	No connection
9	Power		V <sub>SS</sub>	Ground connection <sup>[19]</sup>
10	IOHR	I	P1[0]	ISSP DATA <sup>[16]</sup> , I <sup>2</sup> C SDA, SPI CLK <sup>[17]</sup>
11	IOHR	I	P1[2]	Driven Shield Output (optional)
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down <sup>[18]</sup>
15	I/O	I	P2[2]	Driven Shield Output (optional)
16	I/O	I	P2[4]	Driven Shield Output (optional)
17	IOH	I	P0[0]	Driven Shield Output (optional)
18	IOH	I	P0[2]	Driven Shield Output (optional)
19	IOH	I	P0[4]	
20	Power		V <sub>DD</sub>	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[3]	Integrating input
23	Power		V <sub>SS</sub>	Ground connection <sup>[19]</sup>
24	IOH	I	P0[1]	Integrating input
CP	Power		V <sub>SS</sub>	Center pad must be connected to ground

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Notes**

14. The center pad (CP) on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. 19 GPIOs = 16 pins for capacitive sensing+2 pins for I<sup>2</sup>C + 1 pin for modulator capacitor.
16. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I<sup>2</sup>C bus. Use alternate pins if you encounter issues.
17. Alternate SPI clock.
18. The internal pull down is 5KOhm.
19. All VSS pins should be brought out to one common GND plane.

**Figure 4. CY8C20337, CY8C20347/S Device**


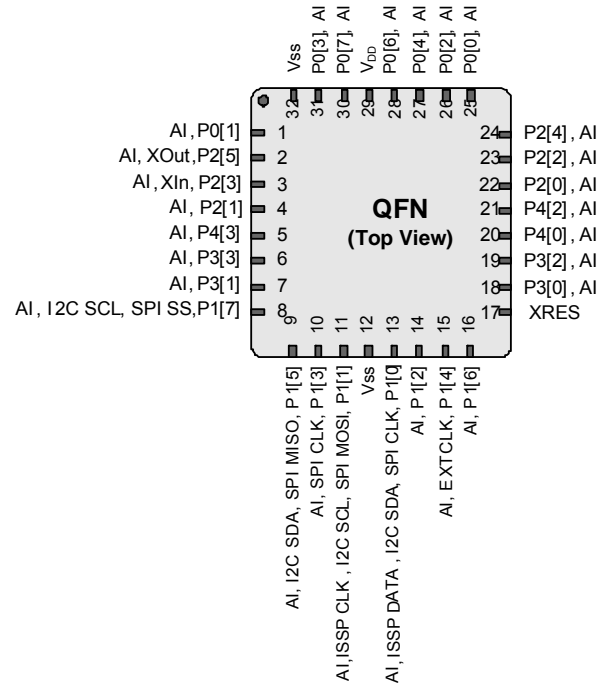
**32-pin QFN (25 Sensing Inputs)<sup>[25]</sup>**
**Table 5. Pin Definitions – CY8C20437, CY8C20447/S, CY8C20467/S <sup>[26]</sup>**

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[5]	Crystal output (XOut)
3	I/O	I	P2[3]	Crystal input (XIn)
4	I/O	I	P2[1]	
5	I/O	I	P4[3]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS
9	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK <sup>[27]</sup> , I <sup>2</sup> C SCL, SPI MOSI.
12	Power		V <sub>SS</sub>	Ground connection <sup>[30]</sup>
13	IOHR	I	P1[0]	ISSP DATA <sup>[27]</sup> , I <sup>2</sup> C SDA, SPI CLK <sup>[28]</sup>
14	IOHR	I	P1[2]	Driven Shield Output (optional)
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down <sup>[29]</sup>
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P4[0]	
21	I/O	I	P4[2]	
22	I/O	I	P2[0]	
23	I/O	I	P2[2]	Driven Shield Output (optional)
24	I/O	I	P2[4]	Driven Shield Output (optional)
25	IOH	I	P0[0]	Driven Shield Output (optional)
26	IOH	I	P0[2]	Driven Shield Output (optional)
27	IOH	I	P0[4]	
28	IOH	I	P0[6]	
29	Power		V <sub>DD</sub>	
30	IOH	I	P0[7]	
31	IOH	I	P0[3]	Integrating input
32	Power		V <sub>SS</sub>	Ground connection <sup>[30]</sup>
CP	Power		V <sub>SS</sub>	Center pad must be connected to ground

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Notes**

25. The center pad (CP) on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
26. 28 GPIOs = 25 pins for capacitive sensing+2 pins for I<sup>2</sup>C + 1 pin for modulator capacitor.
27. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I<sup>2</sup>C bus. Use alternate pins if you encounter issues.
28. Alternate SPI clock.
29. The internal pull down is 5KOhm.
30. All VSS pins should be brought out to one common GND plane.

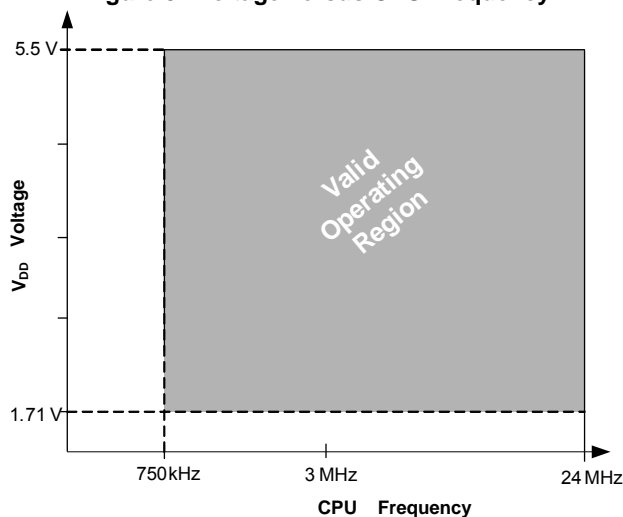
**Figure 6. CY8C20437, CY8C20447/S, CY8C20467/S Device**




## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x37/47/67/S PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at <http://www.cypress.com/psoc>.

**Figure 8. Voltage versus CPU Frequency**



## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 7. Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>STG</sub>	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	-55	+25	+125	°C
V <sub>DD</sub>	Supply voltage relative to V <sub>SS</sub>	—	-0.5	—	+6.0	V
V <sub>IO</sub>	DC input voltage	—	V <sub>SS</sub> - 0.5	—	V <sub>DD</sub> + 0.5	V
V <sub>IOZ</sub>	DC voltage applied to tristate	—	V <sub>SS</sub> - 0.5	—	V <sub>DD</sub> + 0.5	V
I <sub>MIO</sub>	Maximum current into any port pin	—	-25	—	+50	mA
ESD	Electro static discharge voltage	Human body model ESD	2000	—	—	V
LU	Latch up current	In accordance with JESD78 standard	—	—	200	mA

## Operating Temperature

**Table 8. Operating Temperature**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Ambient temperature	—	-40	—	+85	°C
T <sub>C</sub>	Commercial temperature range	—	0	—	70	°C
T <sub>J</sub>	Operational die temperature	The temperature rise from ambient to junction is package specific. See the <a href="#">Thermal Impedances on page 30</a> . The user must limit the power consumption to comply with this requirement.	-40	—	+100	°C

## DC I<sup>2</sup>C Specifications

Table 20 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 20. DC I<sup>2</sup>C Specifications<sup>[50]</sup>**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>ILI2C</sub>	Input low level	$3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	$0.25 \times V_{DD}$	V
		$2.5\text{ V} \leq V_{DD} \leq 3.0\text{ V}$	–	–	$0.3 \times V_{DD}$	V
		$1.71\text{ V} \leq V_{DD} \leq 2.4\text{ V}$	–	–	$0.3 \times V_{DD}$	V
V <sub>IHI2C</sub>	Input high level	$1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$0.65 \times V_{DD}$	–	$V_{DD}^{+}$ $0.7\text{ V}^{[51]}$	V

## Shield Driver DC Specifications

Table 21 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 21. Shield Driver DC Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>Ref</sub>	Reference buffer output	$1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.942	–	1.106	V
V <sub>RefHi</sub>	Reference buffer output	$1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.104	–	1.296	V

## DC IDAC Specifications

Table 22 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 22. DC IDAC Specifications (8-bit IDAC)**

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–1	–	1	LSB	–
IDAC_DNL	Integral nonlinearity	–2	–	2	LSB	–
IDAC_Current	Range = 4x	138	–	169	μA	DAC setting = 127 dec
	Range = 8x	138	–	169	μA	DAC setting = 64 dec

**Table 23. DC IDAC Specifications (7-bit IDAC)**

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–1	–	1	LSB	–
IDAC_DNL	Integral nonlinearity	–2	–	2	LSB	–
IDAC_Current	Range = 4x	137	–	168	μA	DAC setting = 127 dec
	Range = 8x	138	–	169	μA	DAC setting = 64 dec

### Notes

50. Errata: Pull-up resistors on I2C interface cannot be connected to a supply voltage that is more than 0.7 V higher than the CY8C20xx7/S power supply. For more information see item #6 in the "Errata" on page 37.

51. Errata: For more information see item #6 in the "Errata" on page 37.



## AC Programming Specifications

Figure 10. AC Waveform

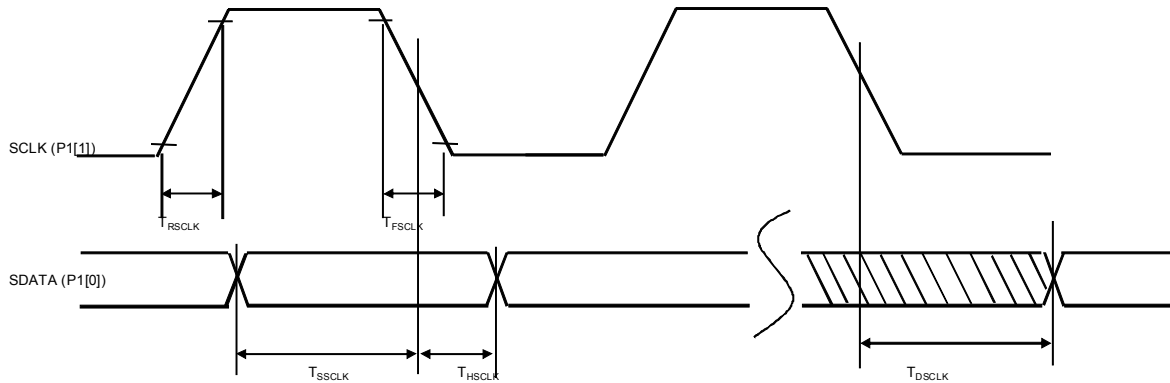


Table 28 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 28. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$t_{RSCLK}$	Rise time of SCLK	—	1	—	20	ns
$t_{FSCLK}$	Fall time of SCLK	—	1	—	20	ns
$t_{SSCLK}$	Data setup time to falling edge of SCLK	—	40	—	—	ns
$t_{HSCLK}$	Data hold time from falling edge of SCLK	—	40	—	—	ns
$F_{SCLK}$	Frequency of SCLK	—	0	—	8	MHz
$t_{ERASEB}$	Flash erase time (block)	—	—	—	18	ms
$t_{WRITE}$	Flash block write time	—	—	—	25	ms
$t_{DSCLK}$	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	—	—	60	ns
$t_{DSCLK3}$	Data out delay from falling edge of SCLK	$3.0 \leq V_{DD} \leq 3.6$	—	—	85	ns
$t_{DSCLK2}$	Data out delay from falling edge of SCLK	$1.71 \leq V_{DD} \leq 3.0$	—	—	130	ns
$t_{XRST3}$	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	—	—	$\mu$ s
$t_{XRES}$	XRES pulse length	—	300	—	—	$\mu$ s
$t_{VDDWAIT}^{[54]}$	$V_{DD}$ stable to wait-and-poll hold off	—	0.1	—	1	ms
$t_{VDDXRES}^{[54]}$	$V_{DD}$ stable to XRES assertion delay	—	14.27	—	—	ms
$t_{POLL}$	SDAT high pulse time	—	0.01	—	200	ms
$t_{ACQ}^{[54]}$	“Key window” time after a $V_{DD}$ ramp acquire event, based on 256 ILO clocks.	—	3.20	—	19.60	ms
$t_{XRESINI}^{[54]}$	“Key window” time after an XRES event, based on 8 ILO clocks	—	98	—	615	$\mu$ s

**Note**

54. Valid from 5 to 50 °C. See the spec, [CY8C20X66](#), [CY8C20X46](#), [CY8C20X36](#), [CY7C643XX](#), [CY7C604XX](#), [CY8CTST2XX](#), [CY8CTMG2XX](#), [CY8C20X67](#), [CY8C20X47](#), [CY8C20X37](#), [Programming Spec](#) for more details.

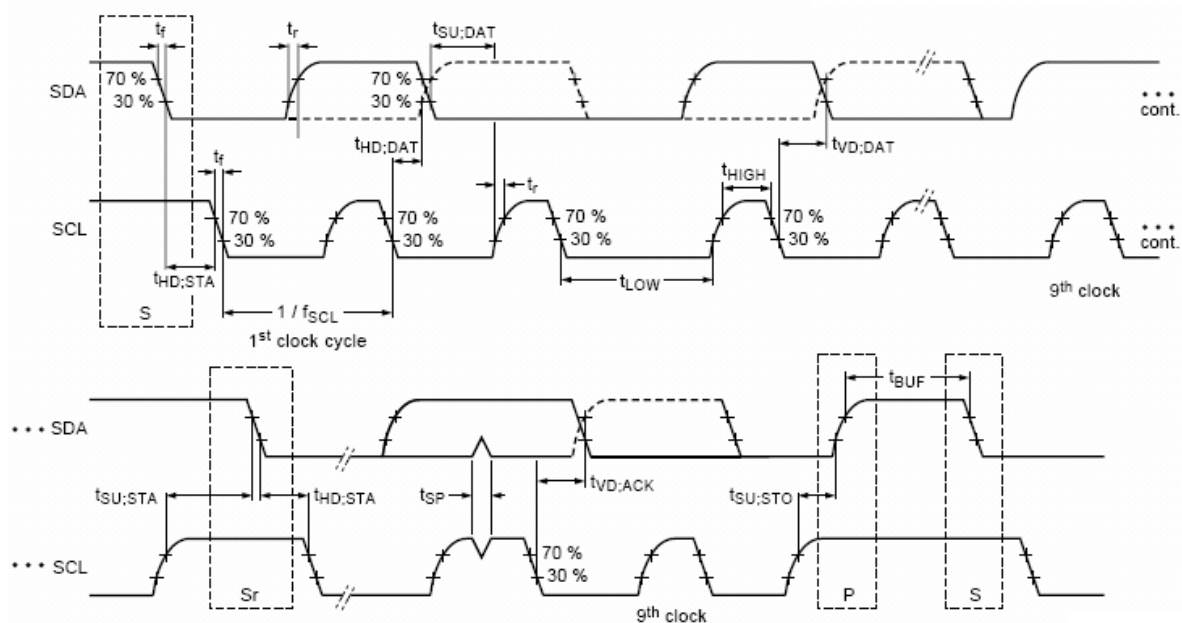
## AC I<sup>2</sup>C Specifications

Table 29 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 29. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins**

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
$f_{SCL}$	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	$\mu$ s
$t_{LOW}$	LOW period of the SCL clock	4.7	–	1.3	–	$\mu$ s
$t_{HIGH}$	HIGH Period of the SCL clock	4.0	–	0.6	–	$\mu$ s
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	–	0.6	–	$\mu$ s
$t_{HD;DAT}^{[55]}$	Data hold time	20	3.45	20	0.90	$\mu$ s
$t_{SU;DAT}$	Data setup time	250	–	100 <sup>[56]</sup>	–	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	–	0.6	–	$\mu$ s
$t_{BUF}$	Bus free time between a STOP and START condition	4.7	–	1.3	–	$\mu$ s
$t_{SP}$	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

**Figure 11. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus**

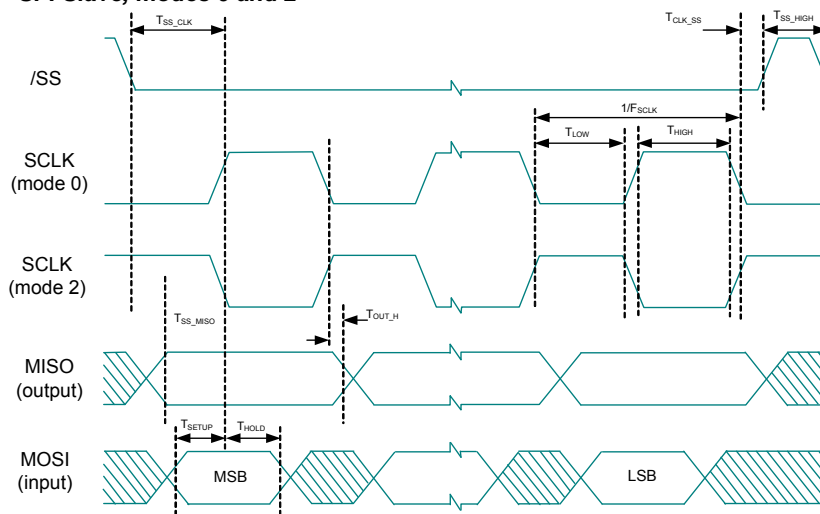
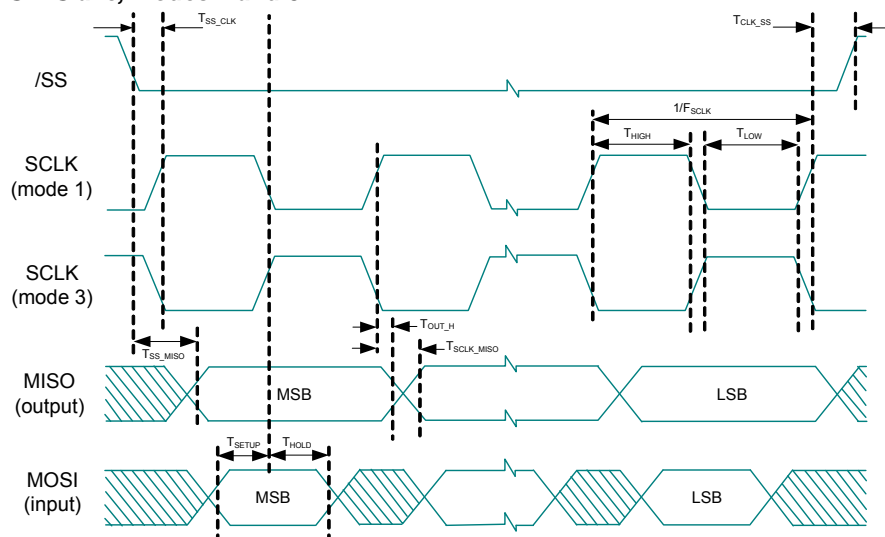


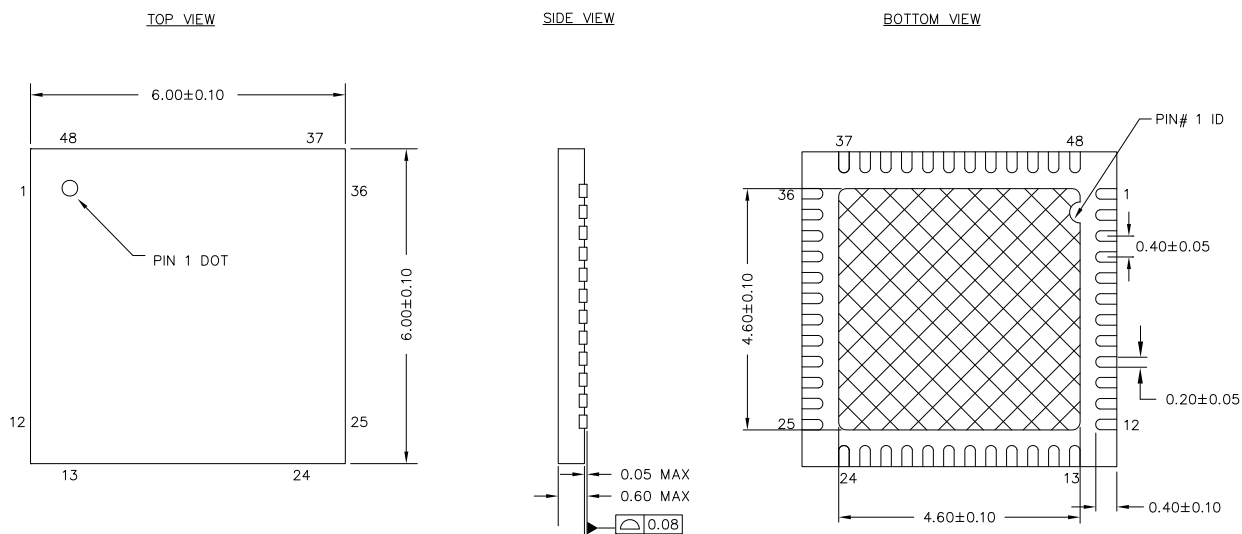
### Notes


55. **Errata:** To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. For more information see item #5 in the "Errata" on page 37.
56. A Fast-Mode I<sup>2</sup>C-bus device can be used in a standard mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU;DAT} \geq 250$  ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$  ns (according to the Standard-Mode I<sup>2</sup>C-bus specification) before the SCL line is released.

**Table 31. SPI Slave AC Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	—	—	—	4	MHz
$t_{LOW}$	SCLK low time	—	42	—	—	ns
$t_{HIGH}$	SCLK high time	—	42	—	—	ns
$t_{SETUP}$	MOSI to SCLK setup time	—	30	—	—	ns
$t_{HOLD}$	SCLK to MOSI hold time	—	50	—	—	ns
$t_{SS\_MISO}$	SS high to MISO valid	—	—	—	153	ns
$t_{SCLK\_MISO}$	SCLK to MISO valid	—	—	—	125	ns
$t_{SS\_HIGH}$	SS high time	—	50	—	—	ns
$t_{SS\_CLK}$	Time from SS low to first SCLK	—	$2/SCLK$	—	—	ns
$t_{CLK\_SS}$	Time from last SCLK to SS high	—	$2/SCLK$	—	—	ns

**Figure 14. SPI Slave Mode 0 and 2**
**SPI Slave, modes 0 and 2**

**Figure 15. SPI Slave Mode 1 and 3**
**SPI Slave, modes 1 and 3**


**Figure 20. 48-Pin (6 x 6 x 0.6 mm) QFN**

**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ± 7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 \*E

**Important Notes**

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at [http://www.amkor.com/products/notes\\_papers/MLFAppNote.pdf](http://www.amkor.com/products/notes_papers/MLFAppNote.pdf).
- Pinned vias for thermal conduction are not required for the low power PSoC device.

## Thermal Impedances

**Table 32. Thermal Impedances per Package**

Package	Typical $\theta_{JA}$ <sup>[57]</sup>
16-pin SOIC	95 °C/W
16-pin QFN	33 °C/W
24-pin QFN <sup>[58]</sup>	21 °C/W
32-pin QFN <sup>[58]</sup>	20 °C/W
48-pin QFN <sup>[58]</sup>	18 °C/W
30-ball WLCSP	54 °C/W

## Capacitance on Crystal Pins

**Table 33. Typical Package Capacitance on Crystal Pins**

Package	Package Capacitance
32-Pin QFN	3.2 pF
48-Pin QFN	3.3 pF

## Solder Reflow Peak Temperature

Table 34 shows the solder reflow temperature limits that must not be exceeded.

**Table 34. Solder Reflow Peak Temperature**

Package	Maximum Peak Temperature ( $T_C$ )	Maximum Time above $T_C - 5$ °C
16-pin SOIC	260 °C	30 seconds
16-pin QFN	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
30-ball WLCSP	260 °C	30 seconds

### Notes

57.  $T_J = T_A + \text{Power} \times \theta_{JA}$ .

58. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

## Development Tool Selection

### Software

#### *PSoC Designer™*

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, in-system programming support, and built-in support for third-party assemblers and C compilers. PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family. PSoC Designer is available free of charge at <http://www.cypress.com/psocdesigner> and includes a free C compiler.

#### *PSoC Designer Software Subsystems*

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

**Assemblers.** The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

#### *PSoC Programmer*

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube in-circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at <http://www.cypress.com/psocprogrammer>.

### Development Kits

All development kits are sold at the [Cypress Online Store](#).

### Evaluation Tools

All evaluation tools are sold at the [Cypress Online Store](#).

#### *CY3210-MiniProg1*

The **CY3210-MiniProg1 kit** allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- 28-pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

#### *CY3210-PSoCEval1*

The **CY3210-PSoCEval1 kit** features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

## Ordering Information

Table 35 lists the CY8C20x37/47/67/S PSoC devices' key package features and ordering codes.

**Table 35. PSoC Device Key Features and Ordering Information**

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	CapSense Sensors	Digital I/O Pins	Analog Inputs <sup>[59]</sup>	XRES Pin	ADC
CY8C20237-24SXI	16-pin SOIC	8 K	1 K	10	13	13	Yes	Yes
CY8C20247S-24SXI	16-pin SOIC	16 K	2 K	10	13	13	Yes	Yes
CY8C20237-24LKXI	16-pin QFN	8 K	1 K	10	13	13	Yes	Yes
CY8C20237-24LKXIT	16-pin QFN (Tape and Reel)	8 K	1 K	10	13	13	Yes	Yes
CY8C20247S-24LKXI	16-pin QFN	16 K	2 K	10	13	13	Yes	Yes
CY8C20247S-24LKXIT	16-pin QFN (Tape and Reel)	16 K	2 K	10	13	13	Yes	Yes
CY8C20337-24LQXI	24-pin QFN	8 K	1 K	16	19	19	Yes	Yes
CY8C20337-24LQXIT	24-pin QFN (Tape and Reel)	8 K	1 K	16	19	19	Yes	Yes
CY8C20347-24LQXI	24-pin QFN	16 K	2 K	16	19	19	Yes	Yes
CY8C20347-24LQXIT	24-pin QFN (Tape and Reel)	16 K	2 K	16	19	19	Yes	Yes
CY8C20347S-24LQXI	24-pin QFN	16 K	2 K	16	19	19	Yes	Yes
CY8C20347S-24LQXIT	24-pin QFN (Tape and Reel)	16 K	2 K	16	19	19	Yes	Yes
CY8C20437-24LQXI	32-pin QFN	8 K	1 K	25	28	28	Yes	Yes
CY8C20437-24LQXIT	32-pin QFN (Tape and Reel)	8 K	1 K	25	28	28	Yes	Yes
CY8C20447-24LQXI	32-pin QFN	16 K	2 K	25	28	28	Yes	Yes
CY8C20447-24LQXIT	32-pin QFN (Tape and Reel)	16 K	2 K	25	28	28	Yes	Yes
CY8C20447S-24LQXI	32-pin QFN	16 K	2 K	25	28	28	Yes	Yes
CY8C20447S-24LQXIT	32-pin QFN (Tape and Reel)	16 K	2 K	25	28	28	Yes	Yes
CY8C20467-24LQXI	32-pin QFN	32 K	2 K	25	28	28	Yes	Yes
CY8C20467-24LQXIT	32-pin QFN (Tape and Reel)	32 K	2 K	25	28	28	Yes	Yes
CY8C20467S-24LQXI	32-pin QFN	32 K	2 K	25	28	28	Yes	Yes
CY8C20467S-24LQXIT	32-pin QFN (Tape and Reel)	32 K	2 K	25	28	28	Yes	Yes
CY8C20637-24LQXI	48-pin QFN	8 K	1 K	31	34	34	Yes	Yes
CY8C20637-24LQXIT	48-pin QFN (Tape and Reel)	8 K	1 K	31	34	34	Yes	Yes
CY8C20647-24LQXI	48-pin QFN	16 K	2 K	31	34	34	Yes	Yes
CY8C20647-24LQXIT	48-pin QFN (Tape and Reel)	16 K	2 K	31	34	34	Yes	Yes
CY8C20647S-24LQXI	48-pin QFN	16 K	2 K	31	34	34	Yes	Yes
CY8C20647S-24LQXIT	48-pin QFN (Tape and Reel)	16 K	2 K	31	34	34	Yes	Yes
CY8C20667-24LQXI	48-pin QFN	32 K	2 K	31	34	34	Yes	Yes
CY8C20667-24LQXIT	48-pin QFN (Tape and Reel)	32 K	2 K	31	34	34	Yes	Yes
CY8C20667S-24LQXI	48-pin QFN	32 K	2 K	31	34	34	Yes	Yes
CY8C20667S-24LQXIT	48-pin QFN (Tape and Reel)	32 K	2 K	31	34	34	Yes	Yes

**Note**

<sup>59</sup>. Dual-function Digital I/O Pins also connect to the common analog mux.

## Acronyms

The following table lists the acronyms that are used in this document.

**Table 36. Acronyms Used in this Document**

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
ESD	electrostatic discharge
FSR	full scale range
GPIO	general purpose input/output
I <sup>2</sup> C	inter-integrated circuit
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
ISSP	in-system serial programming
LCD	liquid crystal display
LDO	low dropout (regulator)
LED	light-emitting diode
LPC	low power comparator
LSB	least-significant bit
LVD	low voltage detect
MCU	micro-controller unit
MIPS	million instructions per second
MISO	master in slave out
MOSI	master out slave in
MSB	most-significant bit
OCD	on-chip debug
PCB	printed circuit board
POR	power on reset
PSRR	power supply rejection ratio
PWRSYS	power system
PSoC	programmable system-on-chip
QFN	quad flat no-lead
SCLK	serial I <sup>2</sup> C clock
SDA	serial I <sup>2</sup> C data
SDATA	serial ISSP data
SOIC	small outline integrated circuit
SPI	serial peripheral interface
SRAM	static random access memory
SS	slave select
USB	universal serial bus
WLCSP	wafer level chip scale package

## Reference Documents

- *Technical reference manual for CY20xx7 devices*
- *In-system Serial Programming (ISSP) protocol for 20xx7*
- *Host Sourced Serial Programming for 20xx7 devices*

## Document Conventions

### Units of Measure

[Table 37](#) lists all the abbreviations used to measure the PSoC devices.

**Table 37. Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
dB	decibel
kHz	kilohertz
ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



## Errata

This section describes the errata for the CY8C20xx7/S family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

### CY8C20xx7/S Qualification Status

Product Status: Production released.

### CY8C20xx7/S Errata Summary

The following Errata items apply to the CY8C20xx7/S datasheet 001-69257.

#### 1. DoubleTimer0 ISR

##### ■Problem Definition

When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0, B0h (PT0\_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

##### ■Parameters Affected

No datasheet parameters are affected.

##### ■Trigger Condition(S)

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

##### ■Scope of Impact

The ISR may be executed twice.

##### ■Workaround

In the ISR, firmware should clear the one-shot bit with a statement such as “`and reg[B0h], FDh`”

##### ■Fix Status

Will not be fixed

##### ■Changes

None

#### 2. Missed GPIO Interrupt

##### ■Problem Definition

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

##### ■Parameters Affected

No datasheet parameters are affected.

##### ■Trigger Condition(S)

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

##### ■Scope of Impact

The GPIO interrupt service routine will not be run.

##### ■Workaround

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt. Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0. Alternatively, the ISR's for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

##### ■Fix Status

Will not be fixed

##### ■Changes

None

### 3. Missed Interrupt During Transition to Sleep

■ **Problem Definition**

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling sleep mode just prior to an interrupt.

■ **Scope of Impact**

The relevant interrupt service routine will not be run.

■ **Workaround**

None.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

### 4. Wakeup from sleep with analog interrupt

■ **Problem Definition**

Device wakes up from sleep when an analog interrupt is trigger

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

■ **Scope of Impact**

Device unexpectedly wakes up from sleep

■ **Workaround**

Disable the analog interrupt before entering sleep and turn it back on upon wake-up.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

## Document History Page

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3276782	DST	06/27/2011	New silicon and document
*A	3327230	DST	07/28/2011	Changed 48-pin dimensions to 6 × 6 × 0.6 mm QFN Updated pins name in <a href="#">Table 3 on page 9</a> and removed USB column and updated dimensions for 48-pin parts in <a href="#">Table 35 on page 33</a> Updated <a href="#">Figure 20 on page 29</a> Removed ICE and Debugger sections. Removed CY3215 Development Kit and CY3280-20x66 UCC sections. Updated <a href="#">Ordering Information</a> .
*B	3403111	YVA	10/12/2011	Moved status from Advance to Preliminary. Updated <a href="#">Ordering Information</a> Removed the row named "48-Pin (6 × 6 mm) QFN (OCD)". Changed all 48-pin ordering code column from CY8C20XXX-24LTxx to CY8C20XXX-24LQxx. Updated 16-pin SOIC and 16-pin QFN package drawings.
*C	3473317	DST	12/23/2011	Updated <a href="#">Features</a> . Updated <a href="#">Pinouts</a> (Removed PSoC in captions of <a href="#">Figure 2</a> , <a href="#">Figure 3</a> , <a href="#">Figure 4</a> , <a href="#">Figure 6</a> , and <a href="#">Figure 7</a> ). Updated <a href="#">DC Chip-Level Specifications</a> under <a href="#">Electrical Specifications</a> (Updated typical value of I <sub>DD24</sub> parameter from 3.32 mA to 2.88 mA, updated typical value of I <sub>DD12</sub> parameter from 1.86 mA to 1.71 mA, updated typical value of I <sub>DD6</sub> parameter from 1.13 mA to 1.16 mA, updated maximum value of I <sub>SB0</sub> parameter from 0.50 µA to 1.1 µA, added I <sub>SB12C</sub> parameter and its details). Updated <a href="#">DC GPIO Specifications</a> under <a href="#">Electrical Specifications</a> (Added the parameters namely V <sub>ILLVT3.3</sub> , V <sub>IHLVT3.3</sub> , V <sub>ILLVT5.5</sub> , V <sub>IHLVT5.5</sub> and their details in <a href="#">Table 10</a> , added the parameters namely V <sub>ILLVT2.5</sub> , V <sub>IHLVT2.5</sub> and their details in <a href="#">Table 11</a> ). Added the following sections namely <a href="#">DC I2C Specifications</a> , <a href="#">Shield Driver DC Specifications</a> , and <a href="#">DC IDAC Specifications</a> under <a href="#">Electrical Specifications</a> . Updated <a href="#">AC Chip-Level Specifications</a> (Added the parameter namely t <sub>JIT_IMO</sub> and its details). Updated <a href="#">Ordering Information</a> (updated <a href="#">Table 35</a> ).
*D	3510277	YVA/DST	02/16/2012	Added CY8C20x37/37S/47/47S/67/67S part numbers and changed title to "1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders" Updated <a href="#">Features</a> . Modified comparator blocks in <a href="#">Logic Block Diagram</a> . Replaced SmartSense with SmartSense auto-tuning. Added CY8C20xx7S part numbers in Pin Definitions. Added footnote for <a href="#">Table 20</a> . Updated <a href="#">Table 21</a> and <a href="#">Table 22</a> and added <a href="#">Table 23</a> . Updated F <sub>32K1</sub> min value. Updated data hold time min values. Updated CY8C206x7 part information in Table "Emulation and Programming Accessories". Updated <a href="#">Ordering Information</a> .
*E	3539259	DST	03/01/2012	Changed Datasheet status from Preliminary to Final. Updated all <a href="#">Pinouts</a> to include Driven Shield Output (optional) information. Updated Min value for V <sub>LPC</sub> <a href="#">Table 15</a> . Updated Offset and Input range in <a href="#">Table 16</a> .

**Document History Page** *(continued)*

<b>Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors</b> <b>Document Number: 001-69257</b>				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*K	4248645	DST	01/16/2014	Updated <a href="#">Pinouts</a> : Updated <a href="#">32-pin QFN (25 Sensing Inputs)[25]</a> : Updated <a href="#">Figure 6</a> .  Updated <a href="#">Packaging Information</a> : spec 001-09116 – Changed revision from *H to *I.
*L	4404150	SLAN	06/10/2014	Updated <a href="#">Pinouts</a> : Updated <a href="#">16-pin SOIC (10 Sensing Inputs)</a> : Updated <a href="#">Table 1</a> : Added Note 6 and referred the same note in description of XRES pin. Updated <a href="#">16-pin QFN (10 Sensing Inputs)[8]</a> : Updated <a href="#">Table 2</a> : Added Note 12 and referred the same note in description of XRES pin. Updated <a href="#">24-pin QFN (16 Sensing Inputs)[14]</a> : Updated <a href="#">Table 3</a> : Added Note 18 and referred the same note in description of XRES pin. Updated <a href="#">30-ball WLCSP (24 Sensing Inputs)</a> : Updated <a href="#">Table 4</a> : Added Note 21 and referred the same note in description of XRES pin. Updated <a href="#">32-pin QFN (25 Sensing Inputs)[25]</a> : Updated <a href="#">Table 5</a> : Added Note 29 and referred the same note in description of XRES pin. Updated <a href="#">48-pin QFN (31 Sensing Inputs)[31]</a> : Updated <a href="#">Table 6</a> : Added Note 35 and referred the same note in description of XRES pin.  Updated <a href="#">Electrical Specifications</a> : Updated <a href="#">DC GPIO Specifications</a> : Updated <a href="#">Table 10</a> : Updated minimum and maximum values of $V_{IH}$ parameter. Updated <a href="#">Table 11</a> : Updated minimum and maximum values of $V_{IH}$ parameter. Updated <a href="#">AC Chip-Level Specifications</a> : Updated <a href="#">Table 24</a> : Removed minimum and maximum values of “ILO untrimmed frequency”.  Updated <a href="#">Packaging Information</a> : spec 001-09116 – Changed revision from *I to *J.  Completing Sunset Review.
*M	4825924	SLAN	07/07/2015	Added the footnote “All VSS pins should be brought out to one common GND plane” in pinout tables ( <a href="#">Table 1</a> through <a href="#">Table 6</a> ). Updated <a href="#">Packaging Information</a> : spec 001-13937 – Changed revision from *E to *F. Updated to new template.
*N	5068999	ARVI	12/31/2015	Updated hyperlink of “Technical Reference Manual” in all instances across the document. Updated <a href="#">PSoC® Functional Overview</a> : Updated <a href="#">Additional System Resources</a> : Updated description. Updated <a href="#">Development Tool Selection</a> : Removed “Accessories (Emulation and Programming)”. Removed “Build a PSoC Emulator into Your Board”.

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