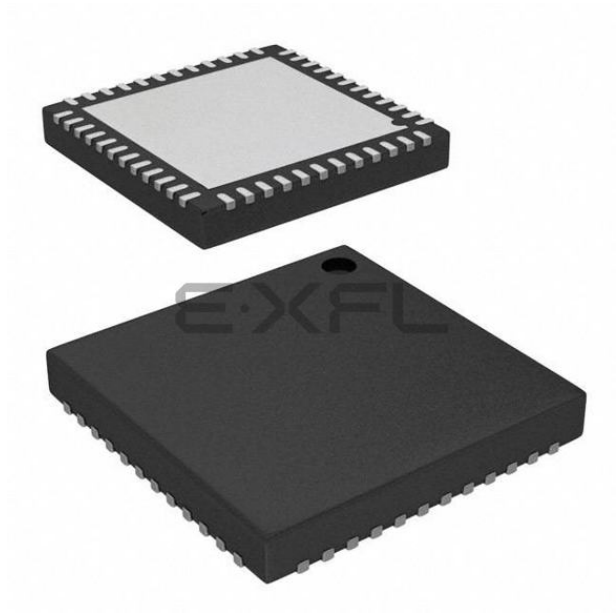

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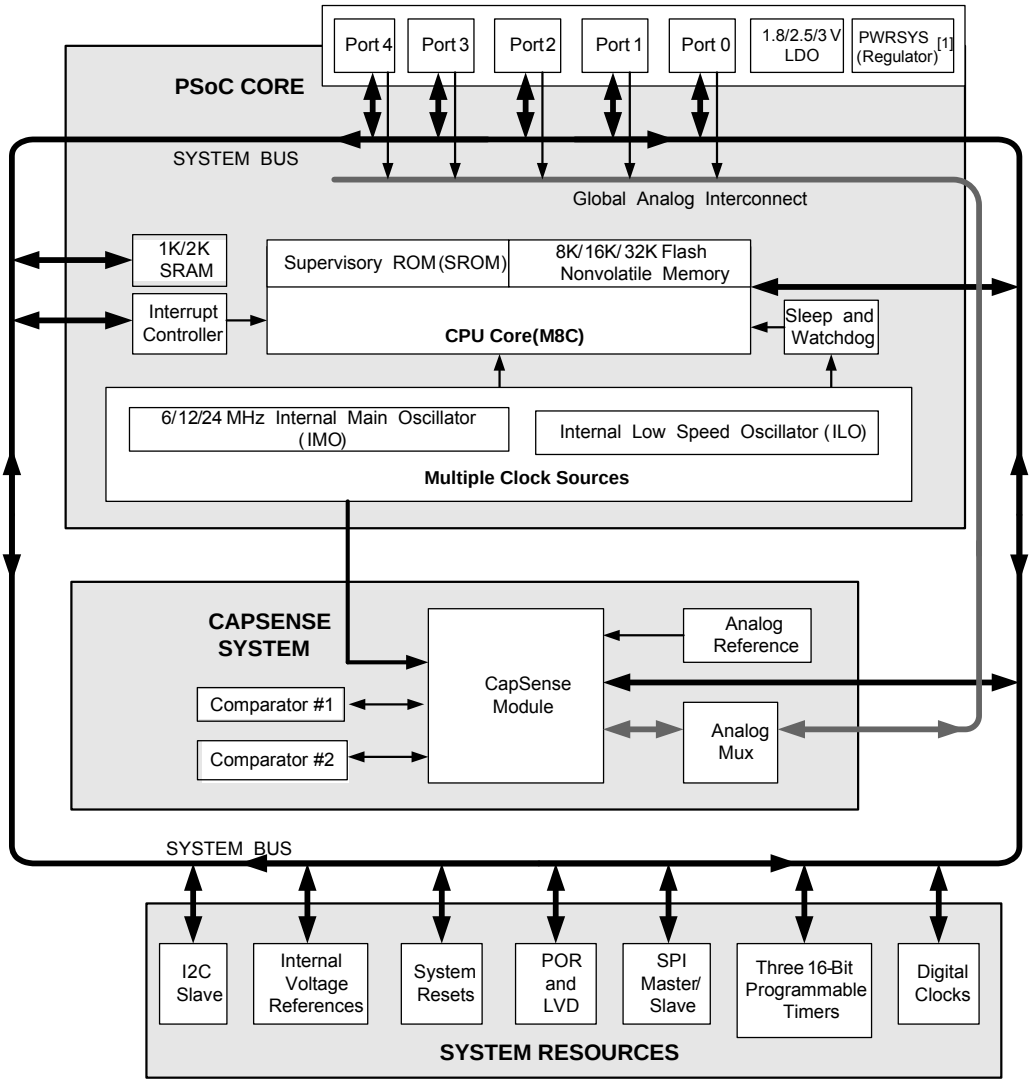
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY8C20xx7/S
RAM Size	2K x 8
Interface	I²C, SPI
Number of I/O	33
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20647-24lqxi

Logic Block Diagram



Note
1. Internal voltage regulator for internal circuitry

Additional System Resources

System resources provide additional capability, such as configurable I^2C slave, SPI master/slave communication interface, three 16-bit programmable timers, various system resets supported by the M8C low voltage detection and power-on reset. The merits of each system resource are listed here:

- The I^2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I^2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I^2C enhanced slave interface appears as a 32-byte RAM buffer to the external I^2C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For more details, refer to the I2CSBUF User Module datasheet.
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20x37/47/67/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

Application Notes/Design Guides

Application notes and design guides are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/gocapsense. Select Application Notes under the Related Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. See “Development Kits” on page 31.

Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

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Pinouts

The CY8C20x37/47/67/S PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

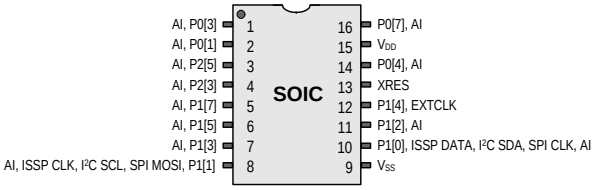
16-pin SOIC (10 Sensing Inputs)

Table 1. Pin Definitions – CY8C20237-24SXI, CY8C20247/S-24SXI [3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[3]	Integrating Input
2	I/O	I	P0[1]	Integrating Input
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P1[7]	I2C SCL, SPI SS
6	I/O	I	P1[5]	I2C SDA, SPI MISO
7	I/O	I	P1[3]	
8	I/O	I	P1[1]	ISSP CLK[4], I2C SCL, SPI MOSI
9	Power		V_{SS}	Ground connection[7]
10	I/O	I	P1[0]	ISSP DATA[4], I2C SDA, SPI CLK[5]
11	I/O	I	P1[2]	Driven Shield Output (optional)
12	I/O	I	P1[4]	Optional external clock (EXTCLK)
13	INPUT		XRES	Active high external reset with internal pull-down[6]
14	I/O	I	P0[4]	
15	Power		V_{DD}	Supply voltage
16	I/O	I	P0[7]	

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 2. CY8C20237-24SXI, CY8C20247/S-24SXI Device



Notes
3. 13 GPIOs = 10 pins for capacitive sensing+2 pins for I^2C + 1 pin for modulator capacitor.
4. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
5. Alternate SPI clock.
6. The internal pull down is 5KOhm.
7. All VSS pins should be brought out to one common GND plane.

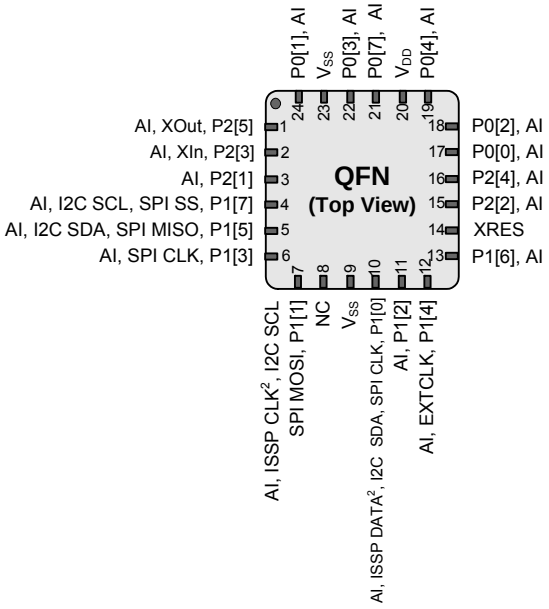
24-pin QFN (16 Sensing Inputs)[14]

Table 3. Pin Definitions – CY8C20337, CY8C20347/S [15]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I^2C SCL, SPI SS
5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[16], I^2C SCL, SPI MOSI
8			NC	No connection
9	Power		V_{SS}	Ground connection[19]
10	IOHR	I	P1[0]	ISSP DATA[16], I^2C SDA, SPI CLK[17]
11	IOHR	I	P1[2]	Driven Shield Output (optional)
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down[18]
15	I/O	I	P2[2]	Driven Shield Output (optional)
16	I/O	I	P2[4]	Driven Shield Output (optional)
17	IOH	I	P0[0]	Driven Shield Output (optional)
18	IOH	I	P0[2]	Driven Shield Output (optional)
19	IOH	I	P0[4]	
20	Power		V_{DD}	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[3]	Integrating input
23	Power		V_{SS}	Ground connection[19]
24	IOH	I	P0[1]	Integrating input
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 4. CY8C20337, CY8C20347/S Device



Notes

14. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. 19 GPIOs = 16 pins for capacitive sensing+2 pins for I^2C + 1 pin for modulator capacitor.
16. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter issues.
17. Alternate SPI clock.
18. The internal pull down is 5KOhm.
19. All VSS pins should be brought out to one common GND plane.

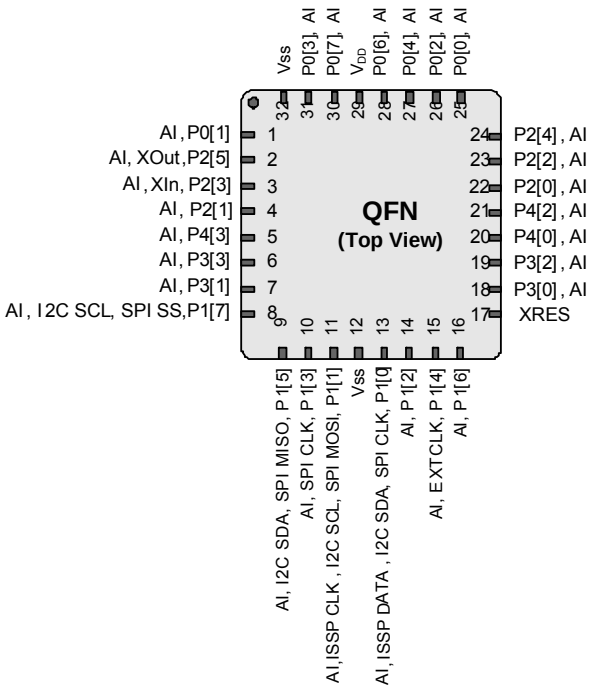
32-pin QFN (25 Sensing Inputs)[25]

Table 5. Pin Definitions – CY8C20437, CY8C20447/S, CY8C20467/S [26]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[5]	Crystal output (XOut)
3	I/O	I	P2[3]	Crystal input (XIn)
4	I/O	I	P2[1]	
5	I/O	I	P4[3]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I^2C SCL, SPI SS
9	IOHR	I	P1[5]	I^2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK[27], I^2C SCL, SPI MOSI.
12	Power		V_{SS}	Ground connection[30]
13	IOHR	I	P1[0]	ISSP DATA[27], I^2C SDA, SPI CLK[28]
14	IOHR	I	P1[2]	Driven Shield Output (optional)
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down[29]
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P4[0]	
21	I/O	I	P4[2]	
22	I/O	I	P2[0]	
23	I/O	I	P2[2]	Driven Shield Output (optional)
24	I/O	I	P2[4]	Driven Shield Output (optional)
25	IOH	I	P0[0]	Driven Shield Output (optional)
26	IOH	I	P0[2]	Driven Shield Output (optional)
27	IOH	I	P0[4]	
28	IOH	I	P0[6]	
29	Power		V_{DD}	
30	IOH	I	P0[7]	
31	IOH	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[30]
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 6. CY8C20437, CY8C20447/S, CY8C20467/S Device



Notes

25. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
26. 28 GPIOs = 25 pins for capacitive sensing+2 pins for I^2C + 1 pin for modulator capacitor.
27. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter issues.
28. Alternate SPI clock.
29. The internal pull down is 5KOhm.
30. All VSS pins should be brought out to one common GND plane.

DC Chip-Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 9. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD} [37, 38, 39]	Supply voltage	See Table 14 on page 17.	1.71	–	5.50	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	2.88	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.71	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.16	1.80	mA
I_{SB0} [40, 41, 42, 43]	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.1	µA
I_{SB1} [40, 41, 42, 43]	Standby current with POR, LVD and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	µA
I_{SBI2C} [40, 41, 42, 43]	Standby current with I^2C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	µA

Notes

37. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
38. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that V_{DD} falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the Technical Reference Manual. In deep sleep/standby sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected and resets the device when V_{DD} goes lower than 1.1 V at edge rates slower than 1 V/ms.
39. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.
40. Errata: When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the “Errata” on page 37.
41. Errata: When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the “Errata” on page 37.
42. Errata: If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the “Errata” on page 37.
43. Errata: Device wakes up from sleep when an analog interrupt is trigger. For more information, see the “Errata” on page 37.

Table 11. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} - 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V_{DD} - 0.40	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} - 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} - 0.50	–	–	V
V_{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V_{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.72	V
V_{IH}	Input high voltage	–	V_{DD} × 0.65	–	V_{DD} + 0.7	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT2.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	V	–	
$V_{IHLVT2.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2		–	V

Table 12. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 pins	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 100 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V

Comparator User Module Electrical Specifications

Table 16 lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40 °C ≤ TA ≤ 85 °C, 1.71 V ≤ V_{DD} ≤ 5.5 V.

Table 16. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset	–	Valid from 0.2 V to 1.5 V	–	2.5	30	mV
Current	–	Average DC current, 50 mV overdrive	–	20	80	µA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range	–	–	0.2		1.5	V

ADC Electrical Specifications

Table 17. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	VREFADC	V
C_{IIN}	Input capacitance	–	–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications on page 21 for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^Resolution/Data Clock)	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^resolution/data clock)	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8, 9, or 10 bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (V_{DD} > 3.0 V)	–	24	–	dB
		PSRR (V_{DD} < 3.0 V)	–	30	–	dB

DC I²C Specifications

Table 20 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. DC I²C Specifications[50]

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{ILI2C}	Input low level	3.1 V ≤ V_{DD} ≤ 5.5 V	–	–	0.25 × V_{DD}	V
		2.5 V ≤ V_{DD} ≤ 3.0 V	–	–	0.3 × V_{DD}	V
		1.71 V ≤ V_{DD} ≤ 2.4 V	–	–	0.3 × V_{DD}	V
V_{IHI2C}	Input high level	1.71 V ≤ V_{DD} ≤ 5.5 V	0.65 × V_{DD}	–	V_{DD} + 0.7 V[51]	V

Shield Driver DC Specifications

Table 21 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. Shield Driver DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{Ref}	Reference buffer output	1.7 V ≤ V_{DD} ≤ 5.5 V	0.942	–	1.106	V
V_{RefHi}	Reference buffer output	1.7 V ≤ V_{DD} ≤ 5.5 V	1.104	–	1.296	V

DC IDAC Specifications

Table 22 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. DC IDAC Specifications (8-bit IDAC)

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–1	–	1	LSB	–
IDAC_DNL	Integral nonlinearity	–2	–	2	LSB	–
IDAC_Current	Range = 4x	138	–	169	µA	DAC setting = 127 dec
	Range = 8x	138	–	169	µA	DAC setting = 64 dec

Table 23. DC IDAC Specifications (7-bit IDAC)

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–1	–	1	LSB	–
IDAC_DNL	Integral nonlinearity	–2	–	2	LSB	–
IDAC_Current	Range = 4x	137	–	168	µA	DAC setting = 127 dec
	Range = 8x	138	–	169	µA	DAC setting = 64 dec

Notes

50. Errata: Pull-up resistors on I2C interface cannot be connected to a supply voltage that is more than 0.7 V higher than the CY8C20xx7/S power supply. For more information see item #6 in the "Errata" on page 37.
51. Errata: For more information see item #6 in the "Errata" on page 37.

AC Chip-Level Specifications

Table 24 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 24. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{IMO24}	IMO frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F_{IMO12}	IMO frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F_{IMO6}	IMO frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F_{CPU}	CPU frequency	–	0.75	–	25.20	MHz
F_{32K1}	ILO frequency	–	15	32	50	kHz
F_{32K_U}	ILO untrimmed frequency	–	–	32	–	kHz
DC_{IMO}	Duty cycle of IMO	–	40	50	60	%
DC_{ILO}	ILO duty cycle	–	40	50	60	%
SR_{POWER_UP}	Power supply slew rate	V_{DD} slew rate during power-up	–	–	250	V/ms
t_{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t_{XRST2}	External reset pulse width after power-up[52]	Applies after part has booted	10	–	–	µs
t_{JIT_IMO}[53]	6 MHz IMO cycle-to-cycle jitter (RMS)	–	–	0.7	6.7	ns
	6 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	–	–	4.3	29.3	ns
	6 MHz IMO period jitter (RMS)	–	–	0.7	3.3	ns
	12 MHz IMO cycle-to-cycle jitter (RMS)	–	–	0.5	5.2	ns
	12 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	–	—	2.3	5.6	ns
	12 MHz IMO period jitter (RMS)	–	–	0.4	2.6	ns
	24 MHz IMO cycle-to-cycle jitter (RMS)	–	–	1.0	8.7	ns
	24 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	–	–	1.4	6.0	ns
	24 MHz IMO period jitter (RMS)	–	–	0.6	4.0	ns

Note
52. The minimum required XRES pulse length is longer when programming the device (see Table 28 on page 23).
53. See the Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

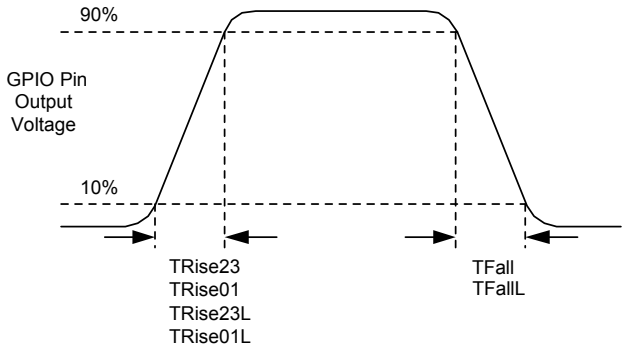
AC General Purpose I/O Specifications

Table 25 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 25. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode Port 0, 1	0 0	– –	6 MHz for 1.71 V <V_{DD} < 2.40 V 12 MHz for 2.40 V < V_{DD}< 5.50 V	MHz MHz
t_{RISE23}	Rise time, strong mode, Cload = 50 pF Ports 2 or 3	V_{DD} = 3.0 to 3.6 V, 10% to 90%	15	–	80	ns
$t_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, Ports 2 or 3	V_{DD} = 1.71 to 3.0 V, 10% to 90%	15	–	80	ns
t_{RISE01}	Rise time, strong mode, Cload = 50 pF Ports 0 or 1	V_{DD} = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled	10	–	50	ns
$t_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1	V_{DD} = 1.71 to 3.0 V, 10% to 90% LDO enabled or disabled	10	–	80	ns
t_{FALL}	Fall time, strong mode, Cload = 50 pF all ports	V_{DD} = 3.0 to 3.6 V, 10% to 90%	10	–	50	ns
t_{FALLL}	Fall time, strong mode low supply, Cload = 50 pF, all ports	V_{DD} = 1.71 to 3.0 V, 10% to 90%	10	–	70	ns

Figure 9. GPIO Timing Diagram



AC Comparator Specifications

Table 26 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 26. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

AC External Clock Specifications

Table 27 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 27. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	µs

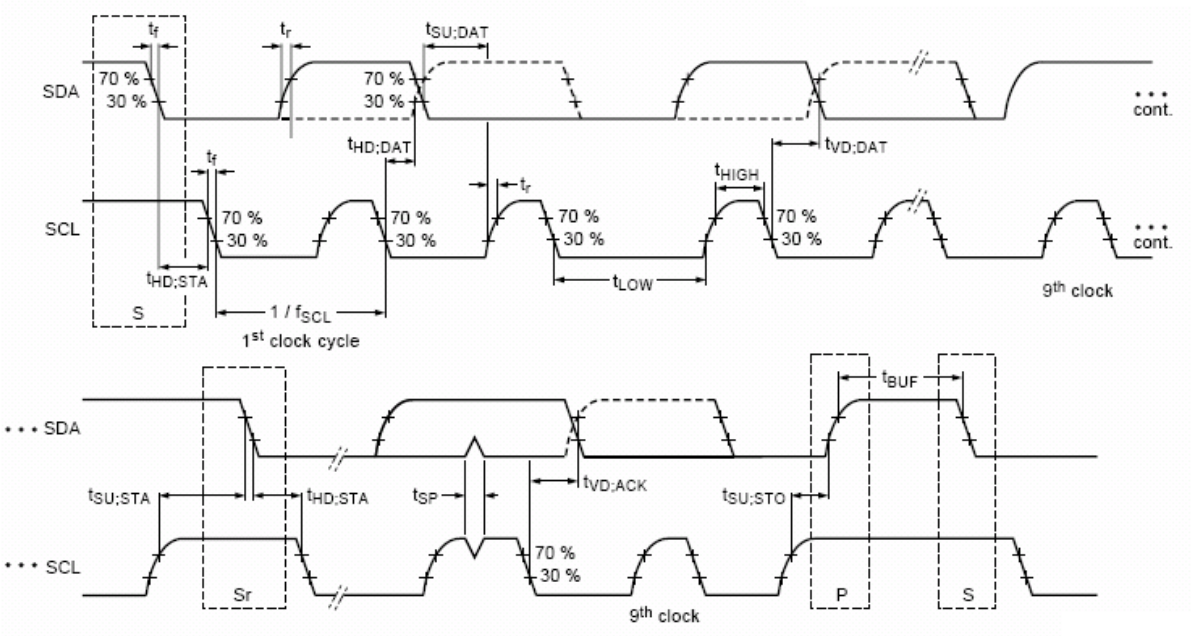
AC I²C Specifications

Table 29 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	µs
t_{HIGH}	HIGH Period of the SCL clock	4.0	–	0.6	–	µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HD;DAT}$[55]	Data hold time	20	3.45	20	0.90	µs
$t_{SU;DAT}$	Data setup time	250	–	100[56]	–	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SP}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 11. Definition for Timing for Fast/Standard Mode on the I²C Bus



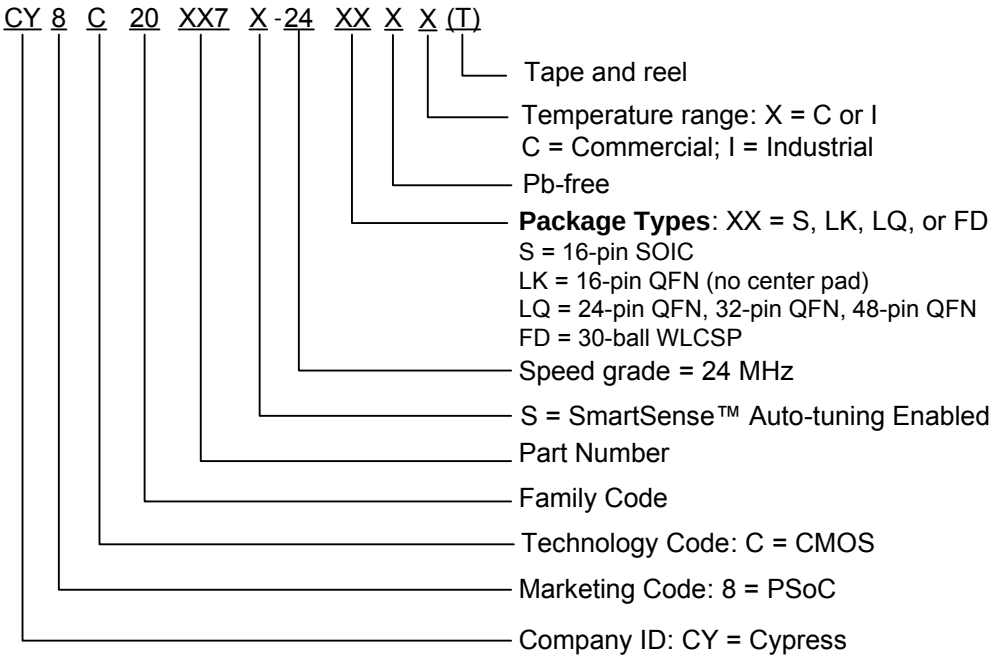
Notes

55. Errata: To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. For more information see item #5 in the "Errata" on page 37.
56. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Table 35. PSoC Device Key Features and Ordering Information *(continued)*

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	CapSense Sensors	Digital I/O Pins	Analog Inputs [59]	XRES Pin	ADC
CY8C20767-24FDXC	30-pin WLCSP	32 K	2 K	24	27	27	Yes	Yes
CY8C20767-24FDXCT	30-pin WLCSP (Tape and Reel)	32 K	2 K	24	27	27	Yes	Yes

Ordering Code Definitions



3. Missed Interrupt During Transition to Sleep

■Problem Definition

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

■Parameters Affected

No datasheet parameters are affected.

■Trigger Condition(S)

Triggered by enabling sleep mode just prior to an interrupt.

■Scope of Impact

The relevant interrupt service routine will not be run.

■Workaround

None.

■Fix Status

Will not be fixed

■Changes

None

4. Wakeup from sleep with analog interrupt

■Problem Definition

Device wakes up from sleep when an analog interrupt is trigger

■Parameters Affected

No datasheet parameters are affected.

■Trigger Condition(S)

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

■Scope of Impact

Device unexpectedly wakes up from sleep

■Workaround

Disable the analog interrupt before entering sleep and turn it back on upon wake-up.

■Fix Status

Will not be fixed

■Changes

None

6. I2C Port Pin Pull-up Supply Voltage

■Problem Definition
Pull-up resistor on I2C interface cannot be connected to a supply voltage that is greater than 0.7 V of CY8C20xx7/S V_{DD}.

■Parameters Affected
None.

■Trigger Condition(S)
This problem occurs only when the I2C master is powered at a higher voltage than CY8C20xx7/S.

■Scope of Impact
This trigger condition will corrupt the I2C communication between the I2C host and the CY8C20xx7/S CapSense controller.

■Workaround
I2C master cannot be powered at a supply voltage that is greater than 0.7 V compared to CY8C20xx7/S supply voltage.

■Fix Status
Will not be fixed

■Changes
None

7. Port1 Pin Voltage

■Problem Definition
Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C20xx7/S V_{DD}.

■Parameters Affected
None.

■Trigger Condition(S)
This problem occurs only when port1 pins are at voltage 0.7 V higher than V_{DD} of CY8C20xx7/S.

■Scope of Impact
This trigger condition will not allow CY8C20xx7/S to drive the output signal on port1 pins, input path is unaffected by this condition.

■Workaround
Port1 should not be connected to a higher voltage than V_{DD} of CY8C20xx7/S.

■Fix Status
Will not be fixed

■Changes
None

Document History Page

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3276782	DST	06/27/2011	New silicon and document
*A	3327230	DST	07/28/2011	Changed 48-pin dimensions to 6 × 6 × 0.6 mm QFN Updated pins name in Table 3 on page 9 and removed USB column and updated dimensions for 48-pin parts in Table 35 on page 33 Updated Figure 20 on page 29 Removed ICE and Debugger sections. Removed CY3215 Development Kit and CY3280-20x66 UCC sections. Updated Ordering Information.
*B	3403111	YVA	10/12/2011	Moved status from Advance to Preliminary. Updated Ordering Information Removed the row named “48-Pin (6 × 6 mm) QFN (OCD)”. Changed all 48-pin ordering code column from CY8C20XXX-24LTxx to CY8C20XXX-24LQxx. Updated 16-pin SOIC and 16-pin QFN package drawings.
*C	3473317	DST	12/23/2011	Updated Features. Updated Pinouts (Removed PSoC in captions of Figure 2, Figure 3, Figure 4, Figure 6, and Figure 7). Updated DC Chip-Level Specifications under Electrical Specifications (Updated typical value of I_{DD24} parameter from 3.32 mA to 2.88 mA, updated typical value of I_{DD12} parameter from 1.86 mA to 1.71 mA, updated typical value of I_{DD6} parameter from 1.13 mA to 1.16 mA, updated maximum value of I_{SB0} parameter from 0.50 µA to 1.1 µA, added I_{SBI2C} parameter and its details). Updated DC GPIO Specifications under Electrical Specifications (Added the parameters namely $V_{ILLVT3.3}$, $V_{IHLVT3.3}$, $V_{ILLVT5.5}$, $V_{IHLVT5.5}$ and their details in Table 10, added the parameters namely $V_{ILLVT2.5}$, $V_{IHLVT2.5}$ and their details in Table 11). Added the following sections namely DC I2C Specifications, Shield Driver DC Specifications, and DC IDAC Specifications under Electrical Specifications. Updated AC Chip-Level Specifications (Added the parameter namely t_{JIT_IMO} and its details). Updated Ordering Information (updated Table 35).
*D	3510277	YVA/DST	02/16/2012	Added CY8C20x37/37S/47/47S/67/67S part numbers and changed title to “1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders” Updated Features. Modified comparator blocks in Logic Block Diagram. Replaced SmartSense with SmartSense auto-tuning. Added CY8C20xx7S part numbers in Pin Definitions. Added footnote for Table 20. Updated Table 21 and Table 22 and added Table 23. Updated F_{32K1} min value. Updated data hold time min values. Updated CY8C206x7 part information in Table “Emulation and Programming Accessories”. Updated Ordering Information.
*E	3539259	DST	03/01/2012	Changed Datasheet status from Preliminary to Final. Updated all Pinouts to include Driven Shield Output (optional) information. Updated Min value for V_{LPC} Table 15. Updated Offset and Input range in Table 16.

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	3645807	DST/BVI	07/03/2012	Updated F_{SCLK} parameter in the Table 31, “SPI Slave AC Specifications,” on page 26 Changed t_{OUT_HIGH} to t_{OUT_H} in Table 30, “SPI Master AC Specifications,” on page 25 Updated Features section, “Programmable pin configurations” bullet: ■ Included the following sub-bullet point - 5 mA source current on port 0 and 1 and 1 mA on port 2,3 and 4 ■ Changed the bullet point “High sink current of 25 mA for each GPIO” to “High sink current of 25 mA for each GPIO. Total 120 mA maximum sink current per chip” ■ Added “QuietZone™ Controller” bullet and updated “Low power CapSense® block with SmartSense™ auto-tuning” bullet. Updated package diagrams 001-13937 to *D and 001-57280 to *C revisions.
*G	3800055	DST	11/23/2012	Changed document title. Part named changed from CY8C20xx7 to CY8C20xx7/S Table 20: Update to VIHI2C to match Item #6 in K2 Si Errata document (001-75370) Updated package diagrams: 51-85068 to *E 001-09116 to *G 001-13937 to *E 001-42168 to *E 001-57280 to *E
*H	3881332	SRLI	02/04/2013	Updated Features: Added Note “Please contact your nearest sales office for additional details.” and referred the same note in “24 Sensing Inputs – 30-pin WLCSP”.
*I	3993458	DST	05/07/2013	Updated Electrical Specifications (Updated DC GPIO Specifications (Updated heading of third column as “Port 0/1 per I/O (max)” for Table 13)). Updated Packaging Information: spec 001-09116 – Changed revision from *G to *H (Figure 17). Added Errata.
*J	4081796	DST	07/31/2013	Added Errata footnotes (Note 40, 41, 42, 43, 44). Updated already existing footnotes (Note 50, 51, 55) as Errata footnotes. Updated Electrical Specifications: Updated DC Chip-Level Specifications: Added Note 40, 41, 42, 43 and referred the same notes in I_{SB0}, I_{SB1}, I_{SBI2C} parameters. Updated DC GPIO Specifications: Added Note 44 and referred the same note in description of $V_{ILLVT3.3}$ parameter in Table 10. Updated DC I2C Specifications: Updated Note 50, 51 referred in Table 20. Updated AC I2C Specifications: Updated Note 55 referred in Table 29. Updated to new template.

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*K	4248645	DST	01/16/2014	Updated Pinouts: Updated 32-pin QFN (25 Sensing Inputs)[25]: Updated Figure 6. Updated Packaging Information: spec 001-09116 – Changed revision from *H to *I.
*L	4404150	SLAN	06/10/2014	Updated Pinouts: Updated 16-pin SOIC (10 Sensing Inputs): Updated Table 1: Added Note 6 and referred the same note in description of XRES pin. Updated 16-pin QFN (10 Sensing Inputs)[8]: Updated Table 2: Added Note 12 and referred the same note in description of XRES pin. Updated 24-pin QFN (16 Sensing Inputs)[14]: Updated Table 3: Added Note 18 and referred the same note in description of XRES pin. Updated 30-ball WLCSP (24 Sensing Inputs): Updated Table 4: Added Note 21 and referred the same note in description of XRES pin. Updated 32-pin QFN (25 Sensing Inputs)[25]: Updated Table 5: Added Note 29 and referred the same note in description of XRES pin. Updated 48-pin QFN (31 Sensing Inputs)[31]: Updated Table 6: Added Note 35 and referred the same note in description of XRES pin. Updated Electrical Specifications: Updated DC GPIO Specifications: Updated Table 10: Updated minimum and maximum values of V_{IH} parameter. Updated Table 11: Updated minimum and maximum values of V_{IH} parameter. Updated AC Chip-Level Specifications: Updated Table 24: Removed minimum and maximum values of “ILO untrimmed frequency”. Updated Packaging Information: spec 001-09116 – Changed revision from *I to *J. Completing Sunset Review.
*M	4825924	SLAN	07/07/2015	Added the footnote “All VSS pins should be brought out to one common GND plane” in pinout tables (Table 1 through Table 6). Updated Packaging Information: spec 001-13937 – Changed revision from *E to *F. Updated to new template.
*N	5068999	ARVI	12/31/2015	Updated hyperlink of “Technical Reference Manual” in all instances across the document. Updated PSoC® Functional Overview: Updated Additional System Resources: Updated description. Updated Development Tool Selection: Removed “Accessories (Emulation and Programming)”. Removed “Build a PSoC Emulator into Your Board”.

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*O	5122184	JFMD	02/02/2016	Updated Features: Removed Note “Please contact your nearest sales office for additional details.” and its reference. Updated Ordering Information: Updated Table 35: Updated part numbers.

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